FLUKE

PRELIMINARY

5700A
CALIBRATOR

Service Manual

P/N 791996
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FLUKE

WARRANTY

John Fluke Mfg. Co., Inc. (Fluke) warrants this instrument to be free from defects in material and workmanship under normal use and service for a period of 1 year from date of shipment. Software is warranted to operate in accordance with its programmed instructions on appropriate Fluke instruments. It is not warranted to be error free. This warranty extends only to the original purchaser and shall not apply to fuses, computer media, batteries or any instrument which, in Fluke's sole opinion, has been subject to misuse, alteration, abuse or abnormal conditions of operation or handling.

Fluke's obligation under this warranty is limited to repair or replacement of an instrument which is returned to an authorized service center within the warranty period and is determined, upon examination by Fluke, to be defective. If Fluke determines that the defect or malfunction has been caused by misuse, alteration, abuse, or abnormal conditions of operation or handling, Fluke will repair the instrument and bill the purchaser for the reasonable cost of repair. If the instrument is not covered by this warranty, Fluke will, if requested by purchaser, submit an estimate of the repair costs before work is started.

To obtain repair service under this warranty purchaser must forward the instrument, (transportation prepaid) and a description of the malfunction to the nearest Fluke Service Center. The instrument shall be repaired at the Service Center or at the factory, at Fluke's option, and returned to purchaser, transportation prepaid. FLUKE ASSUMES NO RISK FOR IN-TRANSIT DAMAGE.

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The purchaser assumes all risk of loss or damage to instruments upon delivery by Fluke to the carrier. If an instrument is damaged in transit, PURCHASER MUST FILE ALL CLAIMS FOR DAMAGE WITH THE CARRIER to obtain compensation. Upon request by purchaser, Fluke will submit an estimate of the cost to repair shipment damage.

Fluke will be happy to answer all questions to enhance the use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX C9090, EVERETT, WA 98206,

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We hereby certify that the Fluke Model 5700A is in compliance with Postal Regulation Vfg. 1046 and is RFI suppressed. The marketing and sale of the equipment was reported to the German Postal Service. The right to retest this equipment to verify compliance with the regulation was given to the German Postal Service.

Bescheinigung des Herstellers/Importeurs

Hiermit wird bescheinigt, daß Fluke Model 5700A in Übereinstimmung mit den Bestimmungen der Amtsblattverfügung Vfg. 1046 funk-entstört ist. Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

John Fluke Mfg. Co., Inc.

INTERFERENCE INFORMATION

This equipment generates and uses radio frequency energy and if not installed and used in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the equipment with respect to the receiver
- Move the equipment away from the receiver
- Plug the equipment into a different outlet so that the computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: How to Identify and Resolve Radio-TV Interference Problems. This booklet is available from the U.S. Government Printing Office, Washington, DC 20402. Stock No. 004-000-00345-4.

OPERATOR SAFETY SUMMARY

WARNING

HIGH VOLTAGE

is used in the operation of this equipment

LETHAL VOLTAGE

MAY BE PRESENT ON THE TERMINALS. OBSERVE ALL SAFETY PRECAUTIONS!

TO AVOID ELECTRICAL SHOCK HAZARD, THE OPERATOR SHOULD NOT ELECTRICALLY CONTACT THE OUTPUT HI OR SENSE HI BINDING POSTS. DURING OPERATION, LETHAL VOLTAGES OF UP TO 1100V AC OR DC MAY BE PRESENT ON THESE TERMINALS.

WHENEVER THE NATURE OF THE OPERATION PERMITS, KEEP ONE HAND AWAY FROM EQUIPMENT TO REDUCE THE HAZARD OF CURRENT FLOWING THROUGH VITAL ORGANS OF THE BODY.

TERMS IN THIS MANUAL

This instrument has been designed and tested in accordance with IEC Publication 348, Safety Requirements for Electronic Measuring Apparatus. This Operator Manual contains information and warnings which have to be followed by the user to ensure safe operation and to retain the instrument in safe condition.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

SYMBOLS MARKED ON EQUIPMENT

ϟ DANGER — High voltage.

⏚ Protective ground (earth) terminal.

⚠ Attention — refer to the manual. This symbol is to indicate that information about usage of a feature is contained in the manual.

POWER SOURCE

The 5700A is intended to operate from a power source that will not apply more than 264V ac rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified on the line voltage selection switch label, and which is identical in type, voltage rating, and current rating.

GROUNDING THE 5700A

The 5700A is a Safety Class I (grounded enclosure) instrument as defined in IEC 348. The enclosure is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired earth grounded receptacle before connecting anything to any of the 5700A terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector appropriate for proper operation of a 5700A in your country.

Use only a power cord that is in good condition.

For detailed information on power cords refer to Figure 2-3 in Section 2.

Refer cord and connector changes to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate the 5700A in an atmosphere of explosive gas.

DO NOT REMOVE COVER

To avoid personal injury, do not remove the 5700A cover. Do not operate the 5700A without the cover properly installed. There are no user-serviceable parts inside the 5700A, so there is no need for the operator to ever remove the cover.

SERVICING SAFETY SUMMARY

PROCEDURES IN THIS MANUAL ARE FOR QUALIFIED SERVICE PERSONNEL ONLY

Also refer to the preceding Operator Safety Summary

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points inside this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

FIRST AID FOR ELECTRIC SHOCK

RESCUE

FREE VICTIM FROM CONTACT WITH LIVE CONDUCTOR QUICKLY. AVOID CONTACT WITH EITHER LIVE CONDUCTOR OR VICTIM'S BODY.

Shut off high voltage at once and ground circuit. If high voltage cannot be turned off quickly, ground circuit.

An ax with a dry wooden handle may be used to cut high voltage line. Use extreme caution to avoid resulting electric flash.

If circuit cannot be broken or grounded, use a dry board, dry clothing, or other nonconductor to free victim.

SYMPTOMS

NEVER ACCEPT ORDINARY AND GENERAL TESTS FOR DEATH.

Symptoms of electric shock may include unconsciousness, failure to breathe, absence of pulse, pallor, and stiffness, as well as severe burns. WHENEVER VICTIM IS NOT BREATHING PROPERLY, GIVE ARTIFICIAL RESPIRATION.

TREATMENT

START ARTIFICIAL RESPIRATION IMMEDIATELY.

Perform artificial respiration at scene of accident, unless victim's or operator's life is endangered. IN THIS CASE ONLY, remove victim to safe location nearby. If new location is more than a few feet away, give artificial respiration while victim is being moved.

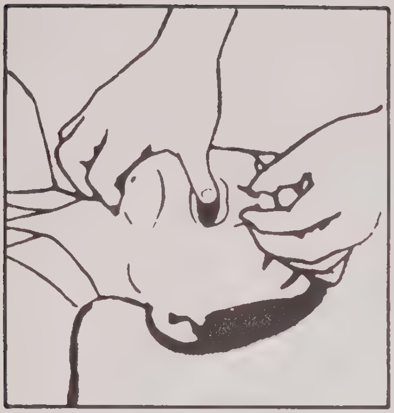
After starting artificial respiration, continue without loss of rhythm for at least FOUR HOURS, or until victim is breathing without help. If you have to change operators while giving artificial respiration, do so without losing rhythm of respiration.

AFTER VICTIM REVIVES

Be prepared to resume artificial respiration, as he may stop breathing again.

When victim is COMPLETELY CONSCIOUS, give him a stimulant (NOT AN ALCOHOLIC DRINK) such as a teaspoonful of aromatic spirits of ammonia in a small glass of water, hot coffee, or hot tea.

Keep victim warm and lying down until he has been conscious for at least fifteen minutes.



POSITION VICTIM

Place victim in face-upward position and kneel close to his ear.

CLEAR THROAT

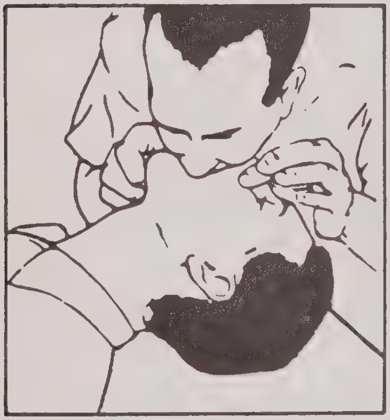
Turn head to one side and quickly wipe out any fluid, mucus, or foreign body from mouth and throat with fingers.

OPEN AIR PASSAGE

Tilt head back and extend neck to open air passage.

LIFT JAW FORWARD

Place thumb in victim's mouth and grasp jaw firmly. Lift jaw forward to pull tongue out of air passage. Do not attempt to hold or depress tongue.



PINCH NOSTRILS CLOSED

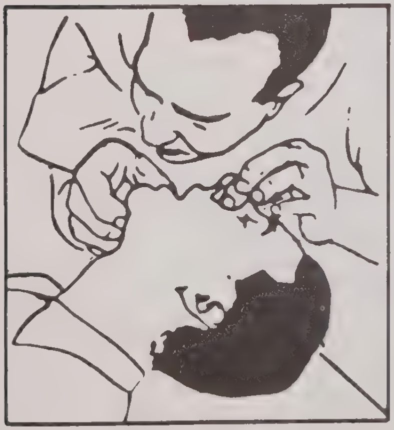
With other hand pinch nostrils closed to prevent air leak.

FORM TIGHT SEAL WITH LIPS

Rescuer's wide-open mouth completely surrounds and seals open mouth of victim. This is not a kissing or puckered position — mouth of rescuer must be wide-open.

BLOW

Exhale firmly into victim's mouth until chest is seen to lift. This can be seen by rescuer without difficulty.



REMOVE MOUTH AND INHALE

During this time, rescuer can hear and feel escape for air from lungs. Readjust position if air does not flow freely in and out of victim's lungs.

Continue at a rate of 12 to 20 times per minute.

Breathing should be normal in rate with only moderate increase in volume, so that rescue breathing can be continued for long periods without fatigue. Do not breathe too forcibly or too large a volume if victim is an infant or small child.

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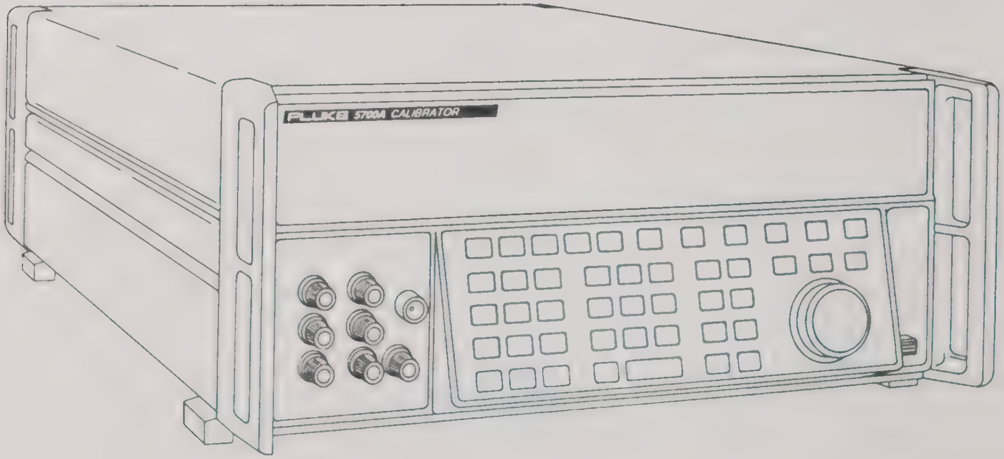
FLUKE 5700A CALIBRATOR

5700A Calibrator

Section 1
Introduction and Specifications

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1-1. INTRODUCTION

The Fluke Model 5700A Calibrator is a precise instrument that calibrates a wide variety of electrical measuring instruments. The 5700A maintains high accuracy over a wide ambient temperature range, allowing it to test instruments wherever they are, rather than only in a temperature-controlled standards laboratory. With a 5700A, you can calibrate precision multimeters that measure ac or dc voltage, ac or dc current, and resistance. Option 5700A-03 Wideband AC Voltage extends this workload to include many rf meters.

Specifications for the 5700A are provided at the end of this section. The 5700A is a fully-programmable precision source of the following:

- DC voltage to 1100V
- AC voltage to 1100V, with output available from 10 Hz to 1.2 MHz
- AC and DC current to 2.2A, with output available from 10 Hz to 10 kHz.
- Resistance in values of $1x10^{n}$ and $1.9x10^{n}$ from short to 100 megohms
- Optional wideband ac voltage from 300 uV to 3.5V (-57 dBm to +24 dBm) 10 Hz to 30 MHz.

The 5700A contains many features that make it an easy-to-use and powerful tool in and out of the standards lab. For a thorough list of these features, refer to the 5700A Operator Manual. The Operator Manual is the primary source of information on all topics relating to operating the instrument in local and remote modes. Descriptions of all the books supplied with the 5700A, including this Service Manual, are provided next.

1-2. HOW TO USE THE MANUAL SET

The 5700A Manual Set provides complete information for the operator and service or maintenance personnel. The set includes the following manuals:

5700A Getting Started Guide	P/N 791962
5700A Operator Manual	P/N 791905
5700A Operator Reference Guide	P/N 813568
5700A Remote Programming Reference Guide	P/N 813550
5700A Service Manual	P/N 791996

Each of the manuals listed above is shipped with every instrument. The two reference guides are packaged inside the 5700A Operator Manual. Order additional copies of the manuals or reference guides separately using the part number provided. For ordering instructions, refer to the Fluke Catalog, or ask a Fluke sales representative.

1-3. 5700A Service Manual

The 5700A Service Manual (this manual) is a maintenance guide for the 5700A. The following topics are included in the 5700A Service Manual:

- Specifications; same as in the Operator Manual (Section 1)
- Theory of operation (Section 2)
- Full verification (recommended every two years) (Section 3)
- Wideband AC (Option 5700-03) flatness calibration (Section 3)
- Maintenance procedures (Section 4)
- Access procedures (Section 4)
- Routine Calibration (Section 3)
- Module-level troubleshooting hints (Section 5)
- Parts lists (Section 6)
- Schematics (Section 7)

1-4. 5700A Getting Started Guide

The 5700A Getting Started Guide provides a step-by-step, hands-on approach to calibrator operation. The guide gives the new user a quick, positive feel for the 5700A and is the best place to start working with the 5700A. The guide also demonstrates both local and remote operation.

1-5. 5700A Operator Manual

The 5700A Operator Manual provides complete information for installing the 5700A and operating the 5700A from the front panel keys and in remote. It also provides a glossary of calibration-related terms as well as general items such as specifications and error code information. The following topics are covered in the 5700A Operator Manual:

- Installation

- Operating controls and features

- Front panel operation

- Remote operation (IEEE-488 bus or serial port remote control)

- Serial port operation (printing, displaying, or transferring data, and setting up for serial port remote control)

- Operator maintenance procedures

- Options and accessories

The 5700A Operator Manual includes two pocket-sized reference booklets; one for front panel operation and one for remote programming.

1-6. 5700A Operator Reference Guide

The 5700A Operator Reference Guide contains a summary of operating instructions from the Operator Manual. This reference guide contains information needed to start up and operate the 5700A. It contains a front and rear feature reference and a softkey menu tree. The guide is included with the 5700A Operator Manual.

1-7. The 5700A Remote Programming Reference Guide

The 5700A Remote Programming Reference Guide contains a summary of remote commands for the 5700A. It also contains information needed to determine system status using the status byte and registers. This reference guide is also included with the 5700A Operator Manual.

1-8. SPECIFICATIONS

The following tables provide specifications for the 5700A, including operation with the Wideband AC Module (Option 5700A-03) and the 5725A Amplifier.

Specifications are valid after allowing a warm-up period of 30 minutes, or twice the time the 5700A has been turned off. For example, if the 5700A has been turned off for five minutes, the warm-up period is ten minutes.

To simplify evaluation of how the 5700A covers your calibration workload, use the 5700A Absolute Uncertainty specifications. Absolute uncertainty includes stability, temperature coefficient, linearity, line and load regulation, and the traceability to external standards. You do not need to add anything to absolute uncertainty to determine the ratios between 5700A uncertainties and the uncertainties of your calibration workload.

Relative Uncertainty specifications are provided for enhanced accuracy applications. These specifications apply when range constants are adjusted (see "Range Calibration"). To calculate absolute uncertainty, you must combine the uncertainties of your external standards and techniques with relative uncertainty.

Secondary Performance Specifications and Operating Characteristics are included in uncertainty specifications. They are provided for special calibration requirements such as stability or linearity testing.

DC Voltage

Range	Resolution	Absolute Uncertainty ±5°C from calibration temperature			
		24 Hours	90 Days	180 Days	1 Year
		±(ppm output + μV)			
220 mV	10 nV	6.5 + .75	7 + .75	8 + .75	9 + .8
2.2V	100 nV	3.5 + 1.2	6 + 1.2	7 + 1.2	8 + 1.2
11V	1 μV	3.5 + 3	5 + 4	7 + 4	8 + 4
22V	1 μV	3.5 + 6	5 + 8	7 + 8	8 + 8
220V	10 μV	5 + 100	6 + 100	8 + 100	9 + 100
1100V	100 μV	7 + 600	8 + 600	10 + 600	11 + 600

Relative Uncertainty ±1°C	
24 Hours	90 Days
±(ppm output + μV)	
2.5 + .5	4 + .5
2.5 + 1.2	4 + 1.2
1.5 + 3	3.5 + 4
1.5 + 6	3.5 + 8
2.5 + 100	4 + 100
3 + 600	4.5 + 600

Secondary Performance Specifications and Operating Characteristics

Included in Uncertainty Specifications

Range	Stability ±1°C	Temperature Coefficient [Note]		Linearity ±1°C	Noise	
					Bandwidth 0.1-10 Hz	Bandwidth 10-10 kHz
	24 Hours	10°-40°C	0°-10°C and 40°-50°C		pk-pk	RMS
	±(ppm output + μV)	±(ppm output + μV)/°C		±(ppm output + μV)		μV
220 mV	.3 + .3	.4 + .1	1.5 + .5	1 + .2	.15 + .1	5
2.2V	.3 + 1	.3 + .1	1.5 + 2	1 + .6	.15 + .4	15
11V	.3 + 2.5	.15 + .2	1 + 1.5	.3 + 2	.15 + 2	50
22V	.4 + 5	.2 + .4	1.5 + 3	.3 + 4	.15 + 4	50
220V	.5 + 40	.3 + 5	1.5 + 40	1 + 40	.15 + 60	150
1100V	.5 + 200	.5 + 10	3 + 200	1 + 200	.15 + 300	500

Note: Temperature coefficient is an adder to uncertainty specifications that does *not* apply unless operating more than ± 5°C from calibration temperature.

Minimum output: 0V for all ranges, except 100V for 1100V range

Maximum load: 50 mA for 2.2V through 220V ranges; 20 mA for 1100V range; 50Ω output impedance on 220 mV range; all ranges <1000 pF, >25Ω

Load regulation: <0.2 ppm + 0.2 μV change, full load to no load

Line regulation: <0.1 ppm change, ±10% of selected nominal line

Settling time: 3 seconds to full accuracy; +1 second for range or polarity change; +1 second for 1100V range

Overshoot: <5%

Common mode rejection: 140 dB, DC to 400 Hz

Remote sensing: Available 0V to ±1100V, on 2.2V through 1100V ranges

AC Voltage

Range	Resolution	Frequency	Absolute Uncertainty ±5°C from calibration temperature				Relative Uncertainty ±1°C	
			24 Hours	90 Days	180 Days	1 Year	24 Hours	90 Days
		Hz	±(ppm output + μV)				±(ppm output + μV)	
2.2 mV	1 nV	10-20	500 + 5	550 + 5	600 + 5	600 + 5	500 + 5	550 + 5
		20-40	200 + 5	220 + 5	230 + 5	240 + 5	200 + 5	220 + 5
		40-20k	100 + 5	110 + 5	120 + 5	120 + 5	60 + 5	65 + 5
		20k-50k	340 + 5	370 + 5	390 + 5	410 + 5	100 + 5	110 + 5
		50k-100k	800 + 8	900 + 8	950 + 8	950 + 8	220 + 8	240 + 8
		100k-300k	.11% + 15	.12% + 15	.13% + 15	.13% + 15	400 + 15	440 + 15
		300k-500k	.15% + 30	.17% + 30	.17% + 30	.18% + 30	.10% + 30	.11% + 30
		500k-1M	.30% + 30	.33% + 30	.35% + 30	.36% + 30	.3% + 30	.33% + 30
22 mV	10 nV	10-20	500 + 6	550 + 6	600 + 6	600 + 6	500 + 6	550 + 6
		20-40	200 + 6	220 + 6	230 + 6	240 + 6	200 + 6	220 + 6
		40-20k	100 + 6	110 + 6	120 + 6	120 + 6	60 + 6	65 + 6
		20k-50k	340 + 6	370 + 6	390 + 6	410 + 6	100 + 6	110 + 6
		50k-100k	800 + 8	900 + 8	950 + 8	950 + 8	220 + 8	240 + 8
		100k-300k	.11% + 15	.12% + 15	.13% + 15	.13% + 15	400 + 15	440 + 15
		300k-500k	.15% + 30	.17% + 30	.17% + 30	.18% + 30	.10% + 30	.11% + 30
		500k-1M	.30% + 30	.33% + 30	.35% + 30	.36% + 30	.3% + 30	.33% + 30
220 mV	100 nV	10-20	500 + 16	550 + 16	600 + 16	600 + 16	500 + 16	550 + 16
		20-40	200 + 10	220 + 10	230 + 10	240 + 10	200 + 10	220 + 10
		40-20k	95 + 10	100 + 10	110 + 10	110 + 10	60 + 10	65 + 10
		20k-50k	300 + 10	330 + 10	350 + 10	360 + 10	100 + 10	110 + 10
		50k-100k	750 + 30	800 + 30	850 + 30	900 + 30	220 + 30	240 + 30
		100k-300k	940 + 30	.1% + 30	.11% + 30	.11% + 30	400 + 30	440 + 30
		300k-500k	.15% + 40	.17% + 40	.17% + 40	.18% + 40	.1% + 40	.11% + 40
		500k-1M	.30% + 100	.33% + 100	.35% + 100	.36% + 100	.3% + 100	.33% + 100
2.2V	1 μV	10-20	500 + 100	550 + 100	600 + 100	600 + 100	500 + 100	550 + 100
		20-40	150 + 30	170 + 30	170 + 30	180 + 30	150 + 30	170 + 30
		40-20k	70 + 7	75 + 7	80 + 7	85 + 7	40 + 7	45 + 7
		20k-50k	120 + 20	130 + 20	140 + 20	140 + 20	100 + 20	110 + 20
		50k-100k	230 + 80	250 + 80	270 + 80	280 + 80	200 + 80	220 + 80
		100k-300k	400 + 150	440 + 150	470 + 150	480 + 150	400 + 150	440 + 150
		300k-500k	.10% + 400	.11% + 400	.12% + 400	.12% + 400	.1% + 400	.11% + 400
		500k-1M	.20% + 1 mV	.22% + 1 mV	.23% + 1 mV	.24% + 1 mV	.2% + 1 mV	.22% + 1 mV
22V	10 μV	10-20	500 + 1 mV	550 + 1 mV	600 + 1 mV	600 + 1 mV	500 + 1 mV	550 + 1 mV
		20-40	150 + 300	170 + 300	170 + 300	180 + 300	150 + 300	170 + 300
		40-20k	70 + 70	75 + 70	80 + 70	85 + 70	40 + 70	45 + 70
		20k-50k	120 + 200	130 + 200	140 + 200	140 + 200	100 + 200	110 + 200
		50k-100k	230 + 400	250 + 400	270 + 400	280 + 400	200 + 400	220 + 400
		100k-300k	500 + 1.7 mV	550 + 1.7 mV	550 + 1.7 mV	600 + 1.7 mV	500 + 1.7 mV	550 + 1.7 mV
		300k-500k	.12% + 5 mV	.13% + 5 mV	.13% + 5 mV	.14% + 5 mV	.12% + 5 mV	.13% + 5 mV
		500k-1M	.26% + 9 mV	.28% + 9 mV	.29% + 9 mV	.30% + 9 mV	.26% + 9 mV	.28% + 9 mV
			±(ppm output + mV)				±(ppm output + mV)	
220V	100 μV	10-20	500 + 10	550 + 10	600 + 10	600 + 10	500 + 10	550 + 10
		20-40	150 + 3	170 + 3	170 + 3	180 + 3	150 + 3	170 + 3
		40-20k	75 + 1	80 + 1	85 + 1	90 + 1	45 + 1	50 + 1
		20k-50k	200 + 4	220 + 4	240 + 4	250 + 4	100 + 1	110 + 1
		50k-100k	500 + 10	550 + 10	600 + 10	600 + 10	300 + 10	330 + 10
		100k-300k	.15% + 110	.15% + 110	.16% + 110	.16% + 110	.15% + 110	.15% + 100
		300k-500k	.50% + 110	.52% + 110	.53% + 110	.54% + 110	.50% + 110	.52% + 110
		500k-1M	1.20% + 220	1.25% + 220	1.25% + 220	1.30% + 220	1.20% + 220	1.20% + 220
1100V	1 mV	50-1k	75 + 4	80 + 4	85 + 4	90 + 4	50 + 4	55 + 4
5725A Amplifier:								
1100V	1 mV	40-1k	75 + 4	80 + 4	85 + 4	90 + 4	50 + 4	55 + 4
		1k-20k	105 + 6	125 + 6	135 + 6	165 + 6	85 + 6	105 + 6
		20k-30k	230 + 11	360 + 11	440 + 11	600 + 11	160 + 11	320 + 11
750V		30k-50k	230 + 11	360 + 11	440 + 11	600 + 11	160 + 11	320 + 11
		50k-100k	600 + 45	.13% + 45	.16% + 45	.23% + 45	380 + 45	.12% + 45

AC Voltage (continued)

Secondary Performance Specifications and Operating Characteristics

Included in Uncertainty Specifications

Range	Frequency	Stability ± 1°C 24 Hours	Temperature Coefficient 10°-40°C	Temperature Coefficient 0°-10°C and 40°-50°C	Output Impedance	Maximum Distortion Bandwidth 10 Hz-10 MHz
	Hz	± µV	± µV/°C		Ω	± (% output + µV)
2.2 mV	10-20	5	.05	.05	50	.05 + 10
	20-40	5	.05	.05		.035 + 10
	40-20k	2	.05	.05		.035 + 10
	20k-50k	2	.1	.1		.035 + 10
	50k-100k	3	.2	.2		.035 + 10
	100k-300k	3	.3	.3		.3 + 30
	300k-500k	5	.4	.4		.3 + 30
	500k-1M	5	.5	.5		1 + 30
22 mV	10-20	5	.2	.3	50	.05 + 11
	20-40	5	.2	.3		.035 + 11
	40-20k	2	.2	.3		.035 + 11
	20k-50k	2	.4	.5		.035 + 11
	50k-100k	3	.5	.5		.035 + 11
	100k-300k	5	.6	.6		.3 + 30
	300k-500k	10	1	1		.3 + 30
	500k-1M	15	1	1		1 + 30
		± (ppm output + µV)	± (ppm output + µV)/°C			
220 mV	10-20	150 + 20	2 + 1	2 + 1	50	.05 + 16
	20-40	80 + 15	2 + 1	2 + 1		.035 + 16
	40-20k	12 + 2	2 + 1	2 + 1		.035 + 16
	20k-50k	10 + 2	15 + 2	15 + 2		.035 + 16
	50k-100k	10 + 2	15 + 4	15 + 4		.035 + 16
	100k-300k	20 + 4	80 + 5	80 + 5		.3 + 30
	300k-500k	100 + 10	80 + 5	80 + 5		.3 + 30
	500k-1M	200 + 20	80 + 5	80 + 5		1 + 30
					Load Regulation ± (ppm output + µV)	
2.2V	10-20	150 + 20	50 + 10	50 + 10	10 + 2	.05 + 80
	20-40	80 + 15	15 + 5	15 + 5	10 + 2	.035 + 80
	40-20k	12 + 4	2 + 1	5 + 2	10 + 4	.035 + 80
	20k-50k	15 + 5	10 + 2	15 + 4	30 + 10	.035 + 80
	50k-100k	15 + 5	10 + 4	20 + 4	120 + 16	.035 + 80
	100k-300k	30 + 10	80 + 15	80 + 15	300 ppm	.3 + 110
	300k-500k	70 + 20	80 + 40	80 + 40	600 ppm	.3 + 110
	500k-1M	150 + 50	80 + 100	80 + 100	.12%	1 + 110
22V	10-20	150 + 20	50 + 100	50 + 100	10 + 20	.05 + 700
	20-40	80 + 15	15 + 30	15 + 40	10 + 20	.035 + 700
	40-20k	12 + 8	2 + 10	4 + 15	10 + 30	.035 + 700
	20k-50k	15 + 10	10 + 20	20 + 20	30 + 50	.035 + 700
	50k-100k	15 + 10	10 + 40	20 + 40	80 + 80	.035 + 700
	100k-300k	30 + 15	80 + 150	80 + 150	100 + 700	.3 + 800
	300k-500k	70 + 100	80 + 300	80 + 300	200 + 1.1 mV	.3 + 800
	500k-1M	150 + 100	80 + 500	80 + 500	600 + 3.0 mV	2 + 800
220V	10-20	150 + 200	50 + 1 mV	50 + 1 mV	10 + .2 mV	.05 + 10 mV
	20-40	80 + 150	15 + 300	15 + 300	10 + .2 mV	.05 + 10 mV
	40-20k	12 + 80	2 + 80	4 + 80	10 + .3 mV	.05 + 10 mV
	20k-50k	15 + 100	10 + 100	20 + 100	30 + .6 mV	.05 + 10 mV
	50k-100k	15 + 100	10 + 500	20 + 500	80 + 3 mV	.1 + 13 mV
	100k-300k	30 + 400	80 + 600	80 + 600	250 + 25 mV	1.5 + 50 mV
	300k-500k	100 + 10 mV	80 + 800	80 + 800	500 + 50 mV	1.5 + 50 mV
	500k-1M	200 + 20 mV	80 + 1 mV	80 + 1 mV	1000 + 110 mV	3.5 + 100 mV
		± (ppm output + mV)	± (ppm output)/°C			± (% output)
1100V	50-1k	20 + .5	2	5	10 + 1	.07

AC Voltage (continued)

Secondary Performance and Operating Characteristics (continued)

Included in Uncertainty Specifications

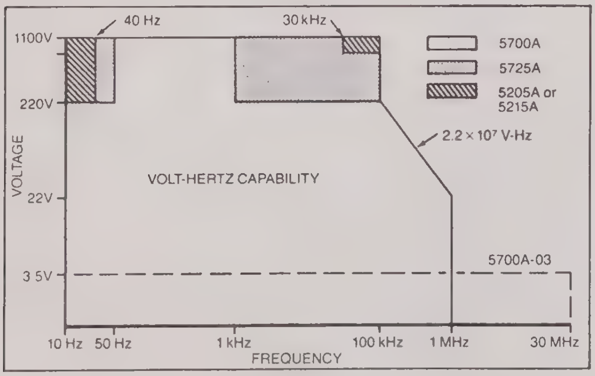
5725A Amplifier:

Range	Frequency	Stability ±1°C 24 Hours	Temperature Coefficient		Load Regulation [Note 2]	Distortion Bandwidth 10 Hz-10 MHz	
			10°-40°C	0°-10°C and 40°-50°C			
	Hz	±(ppm output + mV)	±(ppm output)/°C		±(ppm output + mV)	±(% output)	
						150 pF	1000 pF
1100V	40-1k	10 + .5	5	5	10 + 1	.07	.07
	1k-20k	15 + 2	5	5	90 + 6	.10	.15
	20k-50k	40 + 2	10	10	275 + 11	.30	.30
	50k-100k	130 + 2	30	30	500 + 30	.30	.30

Voltage Range	Maximum Current Limits		Load Limits
2.2V [Note 1] 22V 220V	50 mA, 0°C-40°C 20 mA, 40°C-50°C		>50Ω, 1000 pF
1100V	6 mA		600 pF
5725A Amplifier:			1000 pF [Note 2]
1100V	40 Hz-5 kHz	50 mA	300 pF
	5 kHz-30 kHz	70 mA	
	30 kHz-100 kHz	70 mA [Note 3]	150 pF

Notes:

1. 2.2V Range, 100 kHz-1.2 MHz only: uncertainty specifications cover loads to 10 mA or 1000 pF. For higher loads, load regulation is added
2. The 5725A will drive up to 1000 pF of load capacitance. Uncertainty specifications include loads to 300 pF and 150 pF as shown under "Load Limits." For capacitances up to the maximum of 1000 pF, add "Load Regulation."
3. Applies from 0°C to 40°C.



Output display formats: Voltage or dBm, dBm reference 600Ω.

Minimum output: 10% on each range

External sense: Selectable for 2.2V, 22V, 220V, and 1100V ranges; 5700A <100 kHz, 5725A <30 kHz

Settling time to full accuracy:

Frequency (Hz)	Settling time (seconds)
<120	7
120-120k	5
>120k	2

+1 second for amplitude or frequency range change; +2 seconds for 5700A 1100V range; +4 seconds for 5725A 1100V range

Overshoot: <10%

Common mode rejection: 140 dB, DC to 400 Hz

Frequency:
Range: 10 Hz to 1.1999 MHz
Uncertainty: ±0.01%
Resolution: 4½ digits

Phase lock: Selectable rear panel BNC input
Phase uncertainty (except 1100V range):
>30 Hz: ±(1° + 0.05°/kHz), <30 Hz: ±3°
Input voltage: 1V to 10V rms sine wave
Frequency range: 10 Hz to 1.1999 MHz
Lock range: ±2% of frequency
Lock-in time: Larger of 10/frequency or 10 msec

Phase reference: Selectable, rear panel BNC output
Range: ±180°
Phase Uncertainty (except 1100V range):
±1° at quadrature points (0°, ±90°, ±180°) elsewhere ±2°
Stability: ±0.1°
Resolution: 1°
Output level: 2.5V rms ±0.2V
Frequency range: 50 Hz to 1 kHz, useable 10 Hz to 1.1999 MHz

Resistance

Nominal Value	Absolute Uncertainty of Characterized Value ± 5°C from calibration temperature [Note 1]			
	24 Hours	90 Days	180 Days	1 Year
Ω	± ppm			
0	50 μΩ	50 μΩ	50 μΩ	50 μΩ
1	85	95	100	110
1.9	85	95	100	110
10	26	28	30	33
19	24	26	28	31
100	15	17	18	20
190	15	17	18	20
1k	11	12	13	15
1.9k	11	12	13	15
10k	9	11	12	14
19k	9	11	12	14
100k	11	13	14	16
190k	11	13	14	16
1M	16	18	20	23
1.9M	17	19	21	24
10M	33	37	40	46
19M	43	47	50	55
100M	110	120	125	130

Relative Uncertainty ± 1°C	
24 Hours	90 Days
± ppm	
50 μΩ	50 μΩ
32	40
25	33
5	8
4	7
2	4
2	4
2	3.5
2	3.5
2	3.5
2	3.5
2	3.5
2	3.5
2.5	5
3.5	6
10	14
20	24
50	60

Secondary Performance Specifications and Operating Characteristics

Included in Uncertainty Specifications

Nominal Value	Stability ± 1°C 24 Hours	Temperature Coefficient [Note 2]		Full Spec Load Range [Note 3]	Maximum Peak Current	Maximum Difference of Characterized to Nominal Value	Two-Wire Adder active compensation [Note 4] Lead Resistance	
		10°-40°C	0°-10°C and 40°-50°C				0.1Ω	1Ω
Ω	± ppm	± ppm/°C		mA	mA	± ppm	± mΩ	
0	—	—	—	8-500	500	—	2	4
1	32	4	5	8-100	700	500	2	4
1.9	25	6	7	8-100	500	500	2	4
10	5	2	3	8-11	220	300	2	4
19	4	2	3	8-11	160	300	2	4
100	2	2	3	8-11	70	150	2	4
190	2	2	3	8-11	50	150	2	4
1k	2	2	3	1-2	22	150	10	15
1.9k	2	2	3	1-1.5	16	150	10	15
10k	2	2	3	100-500 μA	7	150	50	60
19k	2	2	3	50-250 μA	5	150	100	120
100k	2	2	3	10-100 μA	1	150		
190k	2	2	3	5-50 μA	500 μA	150		
1M	2.5	2.5	6	5-20 μA	100 μA	200		
1.9M	3.5	3	10	2.5-10 μA	50 μA	200		
10M	10	5	20	.5-2 μA	10 μA	300		
19M	20	8	40	.25-1 μA	5 μA	300		
100M	50	12	100	50-200 nA	1 μA	500		

Notes:

1. Specifications apply to displayed value. 4-wire connections, except 100 MΩ, <80% RH to 30°C, <70% RH to 40°C, <60% RH to 50°C

2. Temperature coefficient is an adder to uncertainty specifications that does *not* apply unless operated more than 5°C from calibration temperature, or calibrated outside the range 19°C to 24°C. Two examples:
a) Calibrate at 20°C: Temperature coefficient adder is not required unless operated below 15°C or above 25°C.
b) Calibrate at 26°C: Add 2°C temperature coefficient adder. Additional temperature coefficient adder is *not* required unless operated below 21°C or above 31°C.

3. Refer to current derating factors table for loads outside of this range.

4. Active two-wire compensation may be selected for values less than 100 kΩ, with either the front panel *or the meter input terminals* as reference plane. Active compensation is limited to 11 mA load, and to 2V burden.

Current Derating Factors

	Value of Derating Factor K for Over or Under Current		
Nominal Value Ω	**Two-Wire Comp** $I<I_L$ **(Note 1)**	**Four-Wire** $I<I_L$ **(Note 1)**	**Four-Wire** $I_U<I<I_{MAX}$ **(Note 2)**
SHORT	4.4	300	—
1	4.4	300	4×10^{-5}
1.9	4.4	160	1.5×10^{-4}
10	4.4	30	1.6×10^{-3}
19	4.4	16	3×10^{-3}
100	4.4	3.5	1×10^{-2}
190	4.4	1.8	1.9×10^{-2}
1k	4.4	0.4	0.1
1.9k	4.4	0.21	0.19
10k	5000	50	2.0
19k	5000	26	3.8
100k	—	7.5	2×10^{-5}
190k	—	4.0	3.8×10^{-5}
1M	—	1.0	1.5×10^{-4}
1.9M	—	0.53	2.9×10^{-4}
10M	—	0.2	1×10^{-3}
19M	—	0.53	1.9×10^{-3}
100M	—	0.1	—

Notes:

1. For $I<I_L$, errors occur due to thermally generated voltages within the 5700A. Use the following equation to determine the error, and add this error to the corresponding UNCERTAINTY or STABILITY specification.

   Error $= K(I_L - I)/(I_L \times I)$

   Where: Error is in mΩ for all TWO-WIRE COMP values and FOUR-WIRE SHORT, and in ppm for the remaining FOUR-WIRE values.
   K is the constant from the above table;
   I and I_L are expressed in mA for SHORT to 1.9 kΩ;
   I and I_L are expressed in µA for 10 kΩ to 100 MΩ

2. For $I_U<I<I_{MAX}$ errors occur due to self-heating of the resistors in the 5700A. Use the following equation to determine the error in ppm, and add this error to the corresponding UNCERTAINTY or STABILITY specification.

   Error in ppm $= K(I^2 - I_U^2)$

   Where: K is the constant from the above table;
   I and I_U are expressed in mA for SHORT to 19 kΩ;
   I and I_U are expressed in µA for 100 kΩ to 100 MΩ

DC Current

Range	Resolution	Absolute Uncertainty ±5°C from calibration temperature			
		24 Hours	90 Days	180 Days	1 Year
	nA	±(ppm output + nA)			
220 μA	.1	45 + 10	50 + 10	55 + 10	60 + 10
2.2 mA	1	45 + 10	50 + 10	55 + 10	60 + 10
22 mA	10	45 + 100	50 + 100	55 + 100	60 + 100
	μA	±(ppm output + μA)			
220 mA	.1	55 + 1	60 + 1	65 + 1	70 + 1
2.2A [Note 1]	1	75 + 30	80 + 30	90 + 30	95 + 30
5725A Amplifier:					
11A	10	330 + 470	340 + 480	350 + 480	360 + 480

Relative Uncertainty ±1°C	
24 Hours	90 Days
±(ppm output + nA)	
24 + 2	26 + 2
24 + 2	26 + 2
24 + 20	26 + 20
±(ppm output + μA)	
26 + .2	30 + .2
40 + 6	45 + 6
100 + 130	110 + 130

Secondary Performance Specifications and Operating Characteristics
Included in Uncertainty Specifications

Range	Stability ±1°C 24 Hours	Temperature Coefficient [Note 2]		Compliance Limits	Burden Voltage Adder [Note 3]	Maximum Load For Full Accuracy [Note 4]	Noise	
		10°-40°C	0°-10°C and 40°-50°C				Bandwidth 0.1-10 Hz pk-pk	Bandwidth 10-10 kHz RMS
	±(ppm output + nA)	±(ppm output + nA)/°C		V	±nA/V	Ω	ppm output + nA	nA
220 μA	5 + 1	1 + .40	3 + 1	10	.2	20k	6 + .9	10
2.2 mA	5 + 5	1 + 2	3 + 10	10	.2	2k	6 + 5	10
22 mA	5 + 50	1 + 20	3 + 100	10	10	200	6 + 50	50
220 mA	8 + 300	1 + 200	3 + 1 μA	10	100	20	9 + 300	500
2.2A	9 + 700	1 + 2.5 μA	3 + 10 μA	3 [Note 5]	2 μA	2	12 + 1.5 μA	20 μA
5725A:	±(ppm output + μA)	±(ppm output + μA)/°C					ppm output + μA	μA
11A	25 + 100	20 + 75	30 + 120	4	0	4	15 + 70	175

Notes:

Maximum output from 5700A terminals is 2.2A. Uncertainty specifications for 220 μA and 2.2 mA ranges are increased by 1.3 × when supplied through 5725A terminals. Specifications are otherwise identical for all output locations.

1. Add to uncertainty specifications:
   ± 200 × I^2 ppm for >100 mA on 220 mA range
   ± 10 × I^2 ppm for >1A on 2.2A range
2. Temperature coefficient is an adder to uncertainty specifications. It does *not* apply unless operating more than ± 5°C from calibration temperature.
3. Burden voltage adder is an adder to uncertainty specifications that does *not* apply unless burden voltage is greater than 0.5V.
4. For higher loads, multiply uncertainty specification by:

$$1 + \frac{0.1 \times \text{actual load}}{\text{maximum load for full accuracy}}$$

5. 5700A compliance limit is 2V for outputs from 1A to 2.2A. 5725A Amplifier may be used in range-lock mode down to 0A.

Minimum output: 0 for all ranges, including 5725A.

Settling time to full accuracy: 1 second for μA and mA ranges; 3 seconds for 2.2A range; 6 seconds for 11A range; + 1 second for range or polarity change

Overshoot: <5%

AC Current

Range	Resolution	Frequency	Absolute Uncertainty ±5°C from calibration temperature				Relative Uncertainty ±1°C	
			24 Hours	90 Days	180 Days	1 Year	24 Hours	90 Days
		Hz	±(ppm output + nA)				±(ppm output + nA)	
220 μA	1 nA	10-20	650 + 30	700 + 30	750 + 30	800 + 30	450 + 30	500 + 30
		20-40	350 + 25	380 + 25	410 + 25	420 + 25	270 + 25	300 + 25
		40-1k	120 + 20	140 + 20	150 + 20	160 + 20	110 + 20	120 + 20
		1k-5k	500 + 50	600 + 50	650 + 50	700 + 50	450 + 50	500 + 50
		5k-10k	.15% + 100	.16% + 100	.17% + 100	.18% + 100	.14% + 100	.15% + 100
2.2 mA	10 nA	10-20	650 + 50	700 + 50	750 + 50	800 + 50	450 + 50	500 + 50
		20-40	350 + 40	380 + 40	410 + 40	420 + 40	270 + 40	300 + 40
		40-1k	120 + 40	140 + 40	150 + 40	160 + 40	110 + 40	120 + 40
		1k-5k	500 + 500	600 + 500	650 + 500	700 + 500	450 + 500	500 + 500
		5k-10k	.15% + 1 μA	.16% + 1 μA	.17% + 1 μA	.18% + 1 μA	.14% + 1 μA	.15% + 1 μA
22 mA	100 nA	10-20	650 + 500	700 + 500	750 + 500	800 + 500	450 + 500	500 + 500
		20-40	350 + 400	380 + 400	410 + 400	420 + 400	270 + 400	300 + 400
		40-1k	120 + 400	140 + 400	150 + 400	160 + 400	110 + 400	120 + 400
		1k-5k	500 + 5 μA	600 + 5 μA	650 + 5 μA	700 + 5 μA	450 + 5 μA	500 + 5 μA
		5k-10k	.15% + 10 μA	.16% + 10 μA	.17% + 10 μA	.18% + 10 μA	.14% + 10 μA	.15% + 10 μA
		Hz	+(ppm output + μA)				+(ppm output + μA)	
220 mA	1 μA	10-20	650 + 5	700 + 5	750 + 5	800 + 5	450 + 5	500 + 5
		20-40	350 + 4	380 + 4	410 + 4	420 + 4	280 + 4	300 + 4
		40-1k	120 + 4	150 + 4	170 + 4	180 + 4	110 + 4	130 + 4
		1k-5k	500 + 50	600 + 50	650 + 50	700 + 50	450 + 50	500 + 50
		5k-10k	.15% + 100	.16% + 100	.17% + 100	.18% + 100	.14% + 100	.15% + 100
2.2A	10 μA	40-1k	600 + 40	650 + 40	700 + 40	750 + 40	600 + 40	650 + 40
		1k-5k	700 + 100	750 + 100	800 + 100	850 + 100	650 + 100	750 + 100
		5k-10k	.80% + 200	.90% + 200	.95% + 200	1.0% + 200	.75% + 200	.85% + 200
5725A Amplifier:								
11A	100 μA	40-1k	370 + 170	400 + 170	440 + 170	460 + 170	300 + 170	330 + 170
		1k-5k	800 + 380	850 + 380	900 + 380	950 + 380	700 + 380	800 + 380
		5k-10k	.3% + 750	.33% + 750	.35% + 750	.36% + 750	.28% + 750	.32% + 750

AC Current (continued)

Secondary Performance Specifications and Operating Characteristics

Included in Uncertainty Specifications

Range	Frequency	Stability ±1°C 24 Hours	Temperature Coefficient [Note 1]		Compliance Limits	Maximum Resistive Load For Full Accuracy [Note 2]	Noise and Distortion Bandwidth 10 Hz-50 kHz <0.5V Burden
			10°-40°C	0°-10°C and 40°-50°C			
	Hz	±(ppm output + nA)	±(ppm output + nA)/µC		V rms	Ω	±(% output + µA)
220 µA	10-20	150 + 5	50 + 5	50 + 5	7	2k	.05 + .1
	20-40	80 + 5	20 + 5	20 + 5			.05 + .1
	40-1k	30 + 3	4 + .5	10 + .5			.05 + .1
	1k-5k	50 + 20	10 + 1	20 + 1			.25 + .5
	5k-10k	400 + 100	20 + 100	20 + 100			.5 + 1
2.2 mA	10-20	150 + 5	50 + 5	50 + 5	7	500	.05 + .1
	20-40	80 + 5	20 + 4	20 + 4			.05 + .1
	40-1k	30 + 3	4 + 1	10 + 2			.05 + .1
	1k-5k	50 + 20	10 + 100	20 + 100			.25 + .5
	5k-10k	400 + 100	50 + 400	50 + 400			.5 + 1
22 mA	10-20	150 + 50	50 + 10	50 + 10	7	150	.05 + .1
	20-40	80 + 50	20 + 10	20 + 10			.05 + .1
	40-1k	30 + 30	4 + 10	10 + 20			.05 + .1
	1k-5k	50 + 500	10 + 500	20 + 400			.25 + .5
	5k-10k	400 + 1 µA	50 + 1 µA	50 + 1 µA			.5 + 1
	Hz	±(ppm output + µA)	±(ppm output + µA)/°C				
220 mA	10-20	150 + .5	50 + .05	50 + .05	7	15	.05 + 10
	20-40	80 + .5	20 + .05	20 + .05			.05 + 10
	40-1k	30 + .3	4 + .1	10 + .1			.05 + 10
	1k-5k	50 + 3	10 + 2	20 + 2			.25 + 50
	5k-10k	400 + 5	50 + 5	50 + 5			.5 + 100
2.2A	40-1k	50 + 5	4 + 1	10 + 1	2 [Note 3]	2	.5 + 100
	1k-5k	80 + 20	10 + 5	20 + 5			.3 + 500
	5k-10k	800 + 50	50 + 10	50 + 10			1 + 1 mA
5725A Amplifier:							±(% output)
11A	40-1k	75 + 100	20 + 75	30 + 75	3	3	[Note 4] .05
	1k-5k	100 + 150	40 + 75	50 + 75			.12
	5k-10k	200 + 300	100 + 75	100 + 75			.5

Notes:

Maximum output from 5700A terminals is 2.2A. Uncertainty specifications for 220 µA and 2.2 mA ranges are increased by 1.3× when supplied through 5725A terminals. Specifications are otherwise identical for all output locations.

1. Temperature coefficient is an adder to uncertainty specifications that does *not* apply unless operating more than ±5°C from calibration temperature.
2. For larger resistive loads multiply uncertainty specifications by:

$$\left(\frac{\text{actual load}}{\text{maximum load for full accuracy}}\right)^2$$

3. 1.5V compliance limit above 1A. 5725A Amplifier may be used in range-lock mode down to 1A.
4. For resistive loads within rated compliance voltage limits.

Minimum output: 9 µA for 220 µA range, 10% on all other ranges. 1A minimum for 5725A.

Inductive load limits: 400 µH (5700A or 5725A). 20 µH for 5700A output >1A.

Power factors: 5700A, 0.9 to 1; 5725A, 0.1 to 1. Subject to compliance voltage limits.

Frequency uncertainty: ±0.01%

Settling time to full accuracy: 5 seconds for 5700A ranges; 6 seconds for 5725A 11A range; +1 second for amplitude or frequency range

Overshoot: <10%

Wideband AC Voltage (Option -03)

Specifications apply to the end of the cable and 50Ω termination used for calibration:

Range		Resolution	Absolute Uncertainty ±5°C from calibration temperature 30 Hz-500 kHz			
Volts	**dBm**		**24 Hours**	**90 Days**	**180 Days**	**1 Year**
			±(% output + µV)			
1.1 mV	−46	10 nV	.4 + .4	.5 + .4	.6 + .4	.8 + 2
3 mV	−37	10 nV	.4 + 1	.45 + 1	.5 + 1	.7 + 3
11 mV	−26	100 nV	.2 + 4	.35 + 4	.5 + 4	.7 + 8
33 mV	−17	100 nV	.2 + 10	.3 + 10	.45 + 10	.6 + 16
110 mV	−6.2	1 µV	.2 + 40	.3 + 40	.45 + 40	.6 + 40
330 mV	+3.4	1 µV	.2 + 100	.25 + 100	.35 + 100	.5 + 100
1.1V	+14	10 µV	.2 + 400	.25 + 400	.35 + 400	.5 + 400
3.5V	+24	10 µV	.15 + 500	.2 + 500	.3 + 500	.4 + 500

Frequency	Frequency Resolution	Amplitude Flatness, 1 kHz Reference			Temperature Coefficient	Settling Time To Full Accuracy	Harmonic Distortion
		Voltage Range					
		1.1 mV	**3 mV**	**>3 mV**			
Hz	**Hz**	**±%**			**±ppm/°C**	**Seconds**	**dB**
10-30	.01	.3	.3	.3	100	7	−40
30-120	.01	.1	.1	.1	100	7	−40
120-1.2k	.1	.1	.1	.1	100	5	−40
1.2k-12k	1	.1	.1	.1	100	5	−40
12k-120k	10	.1	.1	.1	100	5	−40
120k-1.2M	100	.2 + 3 µV	.1 + 3 µV	.1 + 3 µV	100	5	−40
1.2M-2M	100k	.2 + 3 µV	.1 + 3 µV	.1 + 3 µV	100	0.5	−40
2M-10M	100k	.4 + 3 µV	.3 + 3 µV	.2 + 3 µV	100	0.5	−40
10M-20M	1M	.6 + 3 µV	.5 + 3 µV	.4 + 3 µV	150	0.5	−34
20M-30M	1M	1.5 + 15 µV	1.5 + 3 µV	1 + 3 µV	300	0.5	−34

Additional Operating Information:

dBm reference = 50Ω

Range boundaries are at voltage points, dBm levels are approximate.

$$\text{dBm} = 10 \log \left(\frac{\text{Power}}{1\text{ mW}} \right),$$

0.22361V across 50Ω = 1 mW or 0 dBm

Minimum output: 300 µV (−57 dBm)

Frequency uncertainty: ±0.01%

Overload protection: A short circuit on the wideband output will not result in damage. After settling time, normal operation is restored upon removal.

General Specifications:

Warm-up time: 2 × the time since last warmed up, to a maximum of 30 minutes.

System installation: Rear output configuration and rack-mount kit available.

Standard interfaces: IEEE-488, RS-232, 5725A, 5205A or 5215A, 5220A, phase lock in (BNC), phase reference out (BNC).

Temperature performance: Operating: 0°C to 50°C. Calibration: 15°C to 35°C. Storage: −40°C to 75°C

Relative humidity: Operating: <80% to 30°C, <70% to 40°C, <40% to 50°C. Storage: <95%, non-condensing

Safety: Designed to comply with UL1244 (1987); IEC 348-1978; IEC 66E (CO) 4; CSA 556B.

Guard isolation: 20 volts

EMI/RFI: Designed to comply with FCC Rules Part 15, Subpart J, Class B; VDE 0871, Class B.

Reliability: MIL-T-28800D, para. 3.13.3.

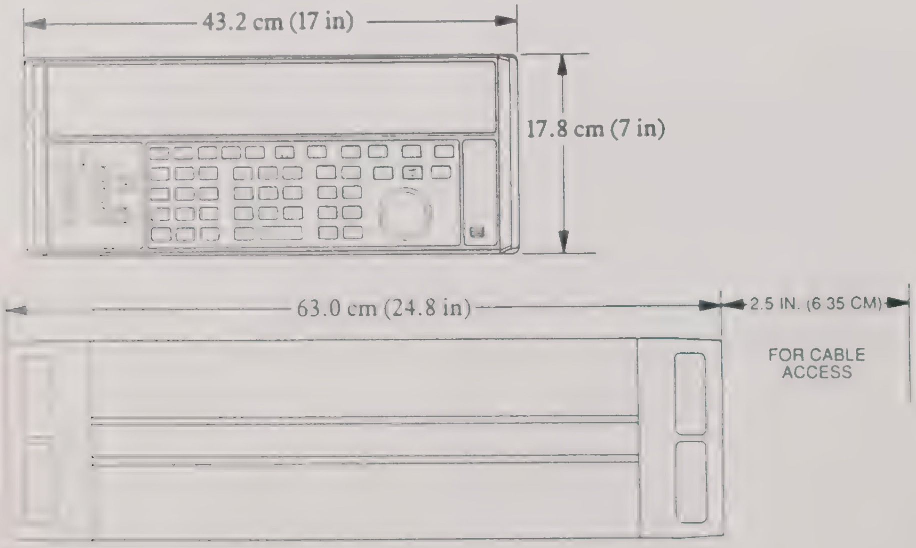
Line Power: 47 to 63 Hz; ±10% allowed about selectable nominal line voltage: 100V, 110V, 115V, 120V, 200V, 220V, 230V, 240V. Maximum power: 5700A, 300VA; 5725A, 750VA.

Size:

5700A: Height 17.8 cm (7 in), standard rack increment, plus 1.5 cm (0.6 in) for feet; Width 43.2 cm (17 in), standard rack width; Depth 63.0 cm (24.8 in), overall; 57.8 cm (22.7 in), rack depth.

5725A: Height 13.3 cm (5.25 in); Width and depth same as 5700A. Both units project 5.1 cm (2 in) from rack front

Weight: 5700A: 27kg (62 lbs); 5725A: 32kg (70 lbs).



Section 2
Theory of Operation

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2-1. INTRODUCTION

This section provides theory of operation in a top-down format. The calibrator is first broadly defined in terms of digital functions (relating to the Digital Motherboard assembly) and analog functions (relating to the Analog Motherboard assembly). The interrelationship of these two areas is then explored in discussions of each output function. Finally, this overall picture is rounded out with a discussion of system interconnections.

Most of this section is devoted to detailed circuit descriptions, first of in the digital (unguarded) section, then in the analog (guarded) section.

2-2. CALIBRATOR OVERVIEW

Figures 2-1, 2-2, and 2-3 comprise the block diagram of the 5700A. These figures are presented further on in the Analog Section Overview and the Digital Section Overview.

The 5700A is configured internally as an automated calibration system with process controls and consistent procedures. Internal microprocessors control all functions and monitor performance, using a switching matrix to route signals between modules. Complete automatic internal diagnostics, both analog and digital, confirm operational integrity.

The heart of the measurement system is a 5-1/2 digit adc (analog-to-digital converter), which is used in a differential mode with the 5700A dac. (The dac is described next under "Internal References.")

2-3. Internal References

The major references that form the basis of the 5700A's accuracy are the hybrid reference amplifiers, patented Fluke solid-state thermal rms sensors, an extremely linear dac, and two internal precision resistors.

2-4. HYBRID REFERENCE AMPLIFIERS

A precision source can only be as accurate as its internal references, so the dc voltage reference for the 5700A was chosen with extreme care. Years of data collection have proven the ovenized reference amplifier to be the best reference device available for modern, ultra-stable voltage standards.

In a microprocessor-controlled precision instrument such as the 5700A, the important characteristics of its dc voltage references are not the accuracy of the value of the references, but rather their freedom from drift and hysteresis. (Hysteresis is the condition of stabilizing at a different value after being turned off then on again.) The 5700A hybrid reference amplifiers excel in both freedom from drift and absence of hysteresis.

2-5. FLUKE THERMAL SENSOR (FTS)

Thermal rms sensors, or ac converters, convert ac voltage to dc voltage with great accuracy. These devices sense true rms voltage by measuring the heat generated by a voltage through a known resistance.

Conventional thermal voltage converters suffer from two main sources of error. First, they exhibit frequency response errors caused by component reactance. Second, they have a poor signal-to-noise ratio because they operate at the millivolt level. The FTS has a full-scale input and output of 2V and a flat frequency response.

After initial functional verification of the Fluke Thermal Sensors, their characteristics only change by less than 1/10th of the allowed ac/dc error per year. External calibration of the ac voltage function of the 5700A consists of verifying that the 5700A meets its specifications.

2-6. DIGITAL-TO-ANALOG CONVERTER (DAC)

A patented 26-bit dac is used in the calibrator as a programmable voltage divider. The dac is a pulse-width modulated (pwm) type with linearity better than 1 ppm (part-per-million) from 1/10th scale to full scale.

2-7. DIGITAL SECTION OVERVIEW

The unguarded Digital Section contains the CPU assembly (A20), Digital Power Supply assembly (A19), Front Panel assembly (A2), Keyboard assembly (A1), and the unguarded portion of the Rear Panel assembly (A21). Figure 2-1 is a block diagram of the digital section of the 5700A.

Power for the digital assemblies and the cooling fans is supplied by the Digital Power Supply assembly.

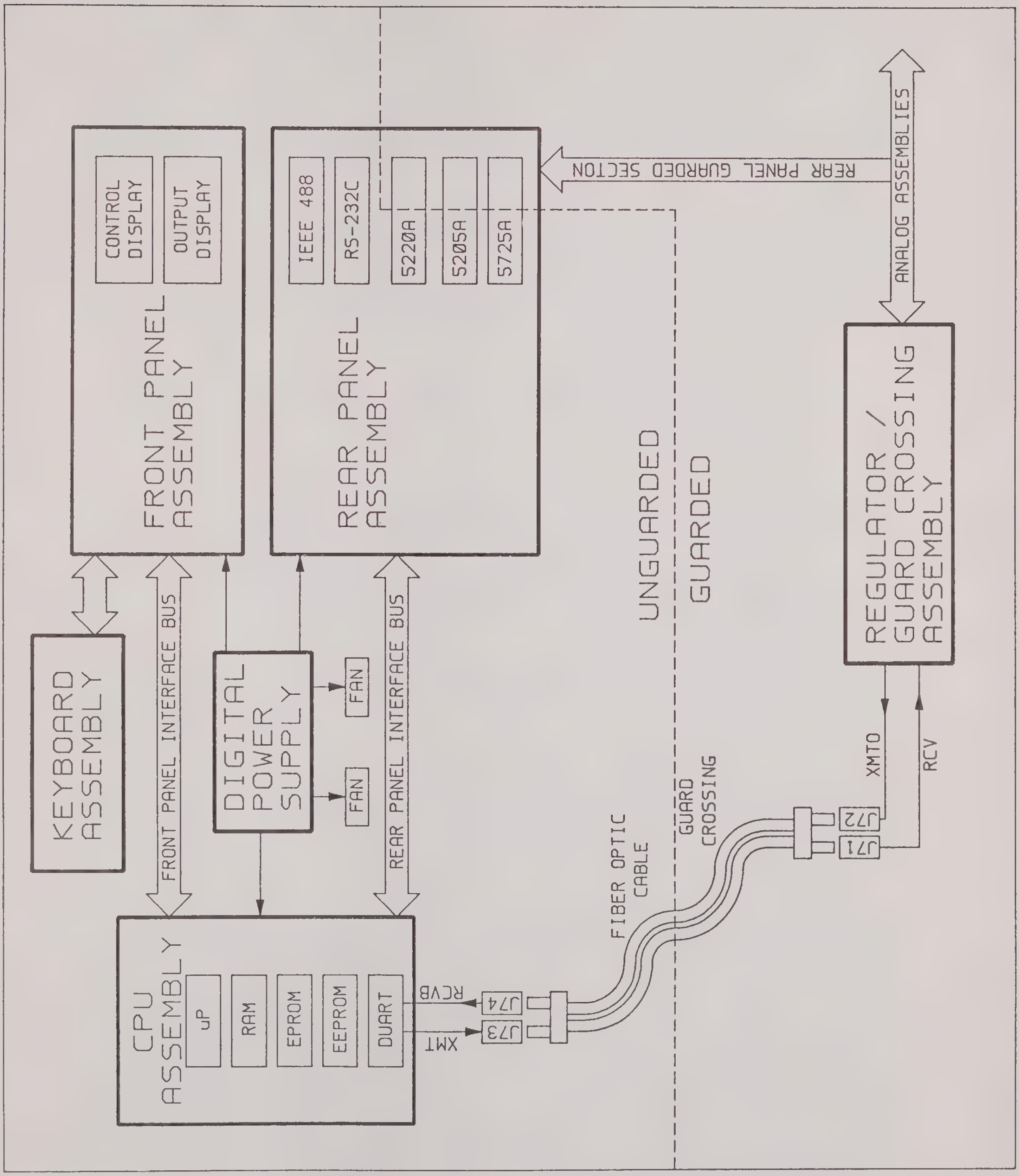

KEYBOARD ASSEMBLY
FRONT PANEL ASSEMBLY
CONTROL DISPLAY
OUTPUT DISPLAY
FRONT PANEL INTERFACE BUS
DIGITAL POWER SUPPLY
FAN
FAN
REAR PANEL ASSEMBLY
IEEE 488
RS-232C
5220A
5205A
5725A
REAR PANEL INTERFACE BUS
REAR PANEL GUARDED SECTION
ANALOG ASSEMBLIES
CPU ASSEMBLY
uP
RAM
EPROM
EEPROM
DUART
RCVB
XMT
J74
J73
FIBER OPTIC CABLE
GUARD CROSSING
UNGUARDED
GUARDED
J72
J71
XMTO
RCV
REGULATOR / GUARD CROSSING ASSEMBLY

Figure 2-1. Digital Section Block Diagram

The CPU (central processing unit) assembly is a single-board computer based on the 68HC000 microprocessor. It controls local and remote interfaces, as well as serial communications over a fiber-optic link to the crossing portion of the Regulator/Guard Crossing assembly (A17). The guard crossing controls the guarded analog circuitry.

A Keyboard assembly provides the user with front-panel control of the 5700A. It contains four LED's, a rotary edit knob, and a forty-five key keypad. It connects to the Front Panel assembly via a cable.

The Front Panel assembly provides information to the user on an Output Display and a Control Display. The Front Panel also contains circuitry that scans the the keyboard and encodes key data for the CPU.

The Rear Panel assembly includes digital interfaces for the following:

- IEEE-488 bus connection
- RS-232-C DTE serial port
- Four auxiliary amplifiers: the 5725A, 5205A, 5215A, and 5220A

2-8. ANALOG SECTION OVERVIEW

The guarded analog section of the 5700A contains the following assemblies:

- Wideband Output (A5) (Part of Option -03)
- Wideband Oscillator (A6) (Part of Option -03)
- Current/Hi-Res (A7)
- Switch Matrix (A8)
- Ohms Cal (A9)
- Ohms (A10)
- DAC (A11)
- Oscillator Control (A12)
- Oscillator Output (A13)
- High Voltage Control (A14)
- High Voltage/High Current (A15)
- Power Amplifier (A16)
- Regulator/Guard Crossing (A17)
- Filter/PA Supply (A18)

These analog assemblies are interfaced to the Analog Motherboard assembly (A3). The guarded digital bus generated by the guard crossing portion of the Regulator/Guard Crossing assembly controls all analog assemblies except the Filter/PA Supply. The Guard Crossing interfaces with the unguarded CPU assembly via a fiber-optic link. The Transformer assembly, along with the filter portion of the Filter/PA Supply assembly and the regulator portion of the Regulator/Guard Crossing assembly, create the system power supply for all the analog assemblies. The Power Amplifier Supply portion of the Filter/PA Supply assembly provides the high voltage power supplies required by the Power Amplifier assembly. The amplitudes of these high voltage supplies are controlled by circuitry contained on the Power Amplifier assembly.

Figures 2-2 and 2-3 are block diagrams for the analog section of the 5700A.

2-9. FUNCTIONAL DESCRIPTION PRESENTED BY OUTPUT FUNCTION

This part of the theory section presents 5700A operation from the perspective of each output function. It describes which assemblies come into play, and how they interact. It does not provide a detailed circuit description. Refer to the individual assembly theories further on in this section for detailed circuit descriptions.

2-10. DC Voltage Functional Description

The DAC assembly (A11) provides a stable dc voltage and is the basic building block of the 5700A. DC voltages are generated in six ranges:

- 220 mV
- 2.2V
- 11V
- 22V
- 220V
- 1100V

The 11V and 22V ranges are generated by the DAC assembly, with its output, DAC OUT HI and DAC SENSE HI routed to the Switch Matrix assembly, where relays connect it to INT OUT HI and INT SENSE HI. Lines INT OUT HI and INT SENSE HI connect to the 5700A binding posts by relays on the Analog Motherboard assembly (A3).

The 2.2V range is created on the Switch Matrix assembly by resistively dividing by five the 11V range from the DAC assembly. Relays on the Switch Matrix and Analog Motherboard route the 2.2V range output to the 5700A binding posts.

The 220 mV range is an extension of the 2.2V range. The Switch Matrix assembly resistively divides by ten the 2.2V range to create the 220 mV range. Relays on the Switch Matrix and Analog Motherboard route the 220 mV range output to the front panel binding posts.

The 220V range is generated by the DAC and Power Amplifier assemblies. The the Power Amplifier amplifies the 11V range of the DAC assembly by a gain of -20 to create the 220V range. The output of the Power Amplifier is routed to the High Voltage Control assembly (A14), where a relay connects it to PA OUT DC. Line PA OUT DC is routed to the binding posts via relays on the Switch Matrix and Analog Motherboard.

The 1100V range is generated by the High Voltage/High Current assembly (A15) operating in conjunction with the Power Amplifier assembly and the High Voltage Control assembly. The 11V range of the DAC assembly is routed to the High Voltage/High Current assembly which amplifies by a gain of -100 to create the 1100V range. Basically the high voltage output is obtained by rectifying and filtering a high voltage ac signal generated by the High Voltage Control assembly operating in conjunction with the Power Amplifier assembly.

2-11. AC Voltage Functional Description

The Oscillator Output assembly (A13) is the ac signal source for the 5700A. The Oscillator Control assembly (A12), controls the amplitude of this ac signal by comparing it with the accurate dc voltage from the DAC assembly and making amplitude corrections via the OSC CONT line. The frequency of oscillation is phase locked to either the high resolution oscillator on the Current/Hi-Res (A7) assembly or an external signal connected to the PHASE LOCK IN connector on the rear panel. AC voltages are generated in the following ranges:

- 2.2 mV
- 22 mV
- 220 mV
- 2.2V
- 11V
- 22V
- 220V
- 1100V

The 2.2V and 22V ranges are generated by the Oscillator Output assembly and routed to the 5700A binding posts via relays on the Switch Matrix (A8) and Analog Motherboard assemblies.

The 220 mV range is generated on the Switch Matrix assembly, which resistively divides by ten the 2.2V range of the Oscillator Output assembly. Relays on the Switch Matrix and Analog Motherboard route the 220 mV range to the 5700A binding posts.

The 2.2 mV and 22 mV ranges are generated on the Switch Matrix assembly. In this mode, the Switch Matrix resistively divides the 2.2V range or the 22V range by 1000 to create the 2.2 mV and 22 mV ranges respectively. Relays on the Switch Matrix and Analog Motherboard route these ranges to the 5700A binding posts.

The 220V range is generated on the Power Amplifier assembly. In this mode, the Power Amplifier is set for a nominal gain of -10 to amplify the 22V range from the Oscillator Output to the 220V range. The 220V ac range from the Power Amplifier is routed to the 5700A binding posts by relays on the High Voltage Control assembly and the Analog Motherboard.

The 1100V range is generated by the High Voltage Control assembly operating in conjunction with the Power Amplifier assembly. In this mode, the 22V range from the Oscillator Output is amplified by the Power Amplifier and High Voltage Control assemblies, which create an amplifier with a nominal gain of -100. Relays on the High Voltage Control and Analog Motherboard assemblies route the 1100V ac range to the 5700A binding posts.

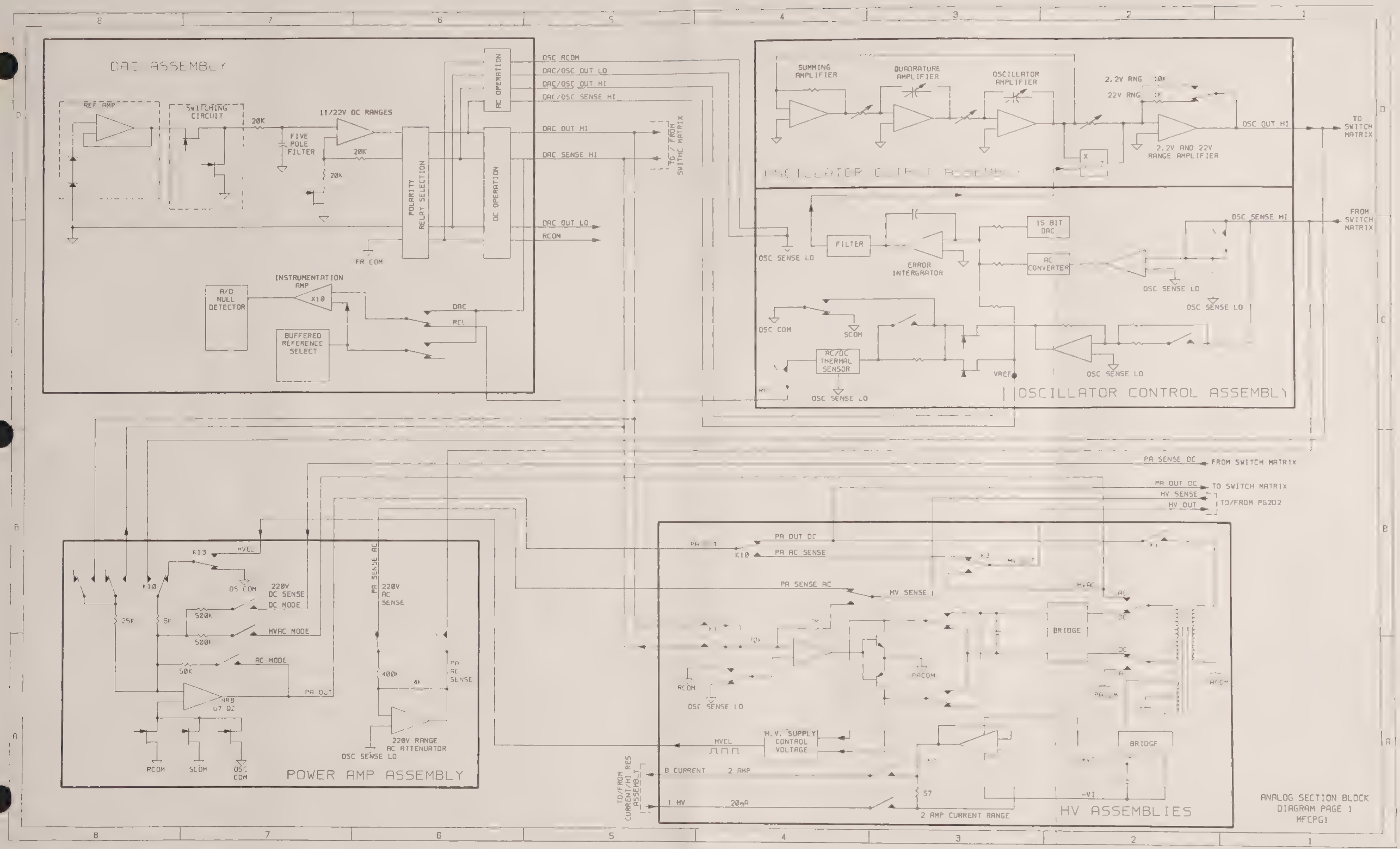
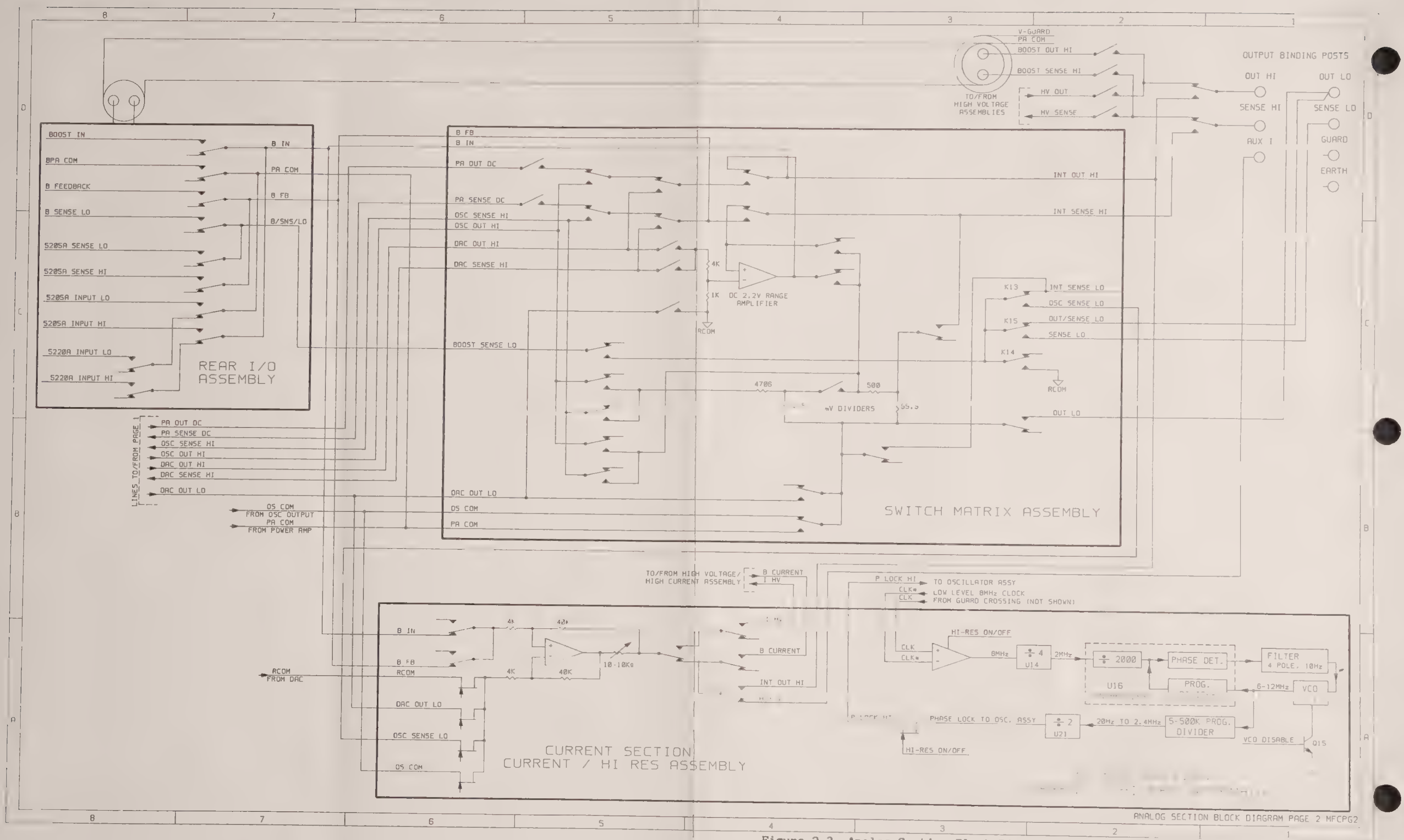

DAC ASSEMBLY
REF AMP
SWITCHING CIRCUIT
20K
FIVE POLE FILTER
11/22V DC RANGES
20K
20k
POLARITY RELAY SELECTION
AC OPERATION
DC OPERATION
FR COM
OSC RCOM
DAC/OSC OUT LO
DAC/OSC OUT HI
DAC/OSC SENSE HI
DAC OUT HI
DAC SENSE HI
TO / FROM SWITHC MATRIX
DAC OUT LO
RCOM
INSTRUMENTATION AMP
X10
A/D NULL DETECTOR
BUFFERED REFERENCE SELECT
DAC
RCL
SUMMING AMPLIFIER
QUADRATURE AMPLIFIER
OSCILLATOR AMPLIFIER
2.2V RNG
22V RNG
2.2V AND 22V RANGE AMPLIFIER
OSC OUT HI
TO SWITCH MATRIX
X
OSCILLATOR OUTPUT ASSEMBLY
OSC SENSE HI
FROM SWITCH MATRIX
15 BIT DAC
FILTER
ERROR INTERGRATOR
OSC SENSE LO
AC CONVERTER
OSC SENSE LO
OSC SENSE LO
OSC COM
SCOM
AC/DC THERMAL SENSOR
VREF
OSC SENSE LO
OSC SENSE LO
OSCILLATOR CONTROL ASSEMBLY
PA SENSE DC
FROM SWITCH MATRIX
PA OUT DC
TO SWITCH MATRIX
HV SENSE
HV OUT
TO/FROM PG2D2
K13
HVCL
K10
OS COM
220V DC SENSE
DC MODE
500k
500k
HVAC MODE
25K
5K
50K
AC MODE
PA OUT
HRB U7 Q2
PA SENSE AC
220V AC SENSE
400Ω
4k
PA AC SENSE
220V RANGE AC ATTENUATOR
OSC SENSE LO
RCOM
SCOM
OSC COM
POWER AMP ASSEMBLY
PA OUT DC
K10
PA AC SENSE
PA SENSE AC
HV SENSE
HVAC
AC
DC
BRIDGE
DC
RCOM
OSC SENSE LO
PACOM
PACOM
H.V. SUPPLY CONTROL VOLTAGE
HVCL
BRIDGE
TO/FROM CURRENT/HI RES ASSEMBLY
B CURRENT
2 AMP
I HV
20mA
S7
-VI
2 AMP CURRENT RANGE
HV ASSEMBLIES
ANALOG SECTION BLOCK DIAGRAM PAGE 1 MFCPG1
8
7
6
5
4
3
2
1
D
C
B
A

Figure 2-2. Analog Section Block Diagram, Part 1



BOOST IN
BPA COM
B FEEDBACK
B SENSE LO
5205A SENSE LO
5205A SENSE HI
5205A INPUT LO
5205A INPUT HI
5220A INPUT LO
5220A INPUT HI
B IN
PA COM
B FB
B/SNS/LO
REAR I/O ASSEMBLY
LINES TO/FROM PAGE 1
PA OUT DC
PA SENSE DC
OSC SENSE HI
OSC OUT HI
DAC OUT HI
DAC SENSE HI
DAC OUT LO
OS COM
FROM OSC OUTPUT
PA COM
FROM POWER AMP
B FB
B IN
PA OUT DC
PA SENSE DC
OSC SENSE HI
OSC OUT HI
DAC OUT HI
DAC SENSE HI
4K
1K
DC 2.2V RANGE AMPLIFIER
RCOM
BOOST SENSE LO
4706
500
mV DIVIDERS
55.5
DAC OUT LO
OS COM
PA COM
SWITCH MATRIX ASSEMBLY
K13
K15
K14
INT SENSE LO
OSC SENSE LO
OUT/SENSE LO
SENSE LO
RCOM
OUT LO
INT OUT HI
INT SENSE HI
V-GUARD
PA COM
BOOST OUT HI
BOOST SENSE HI
HV OUT
HV SENSE
TO/FROM HIGH VOLTAGE ASSEMBLIES
OUTPUT BINDING POSTS
OUT HI
OUT LO
SENSE HI
SENSE LO
AUX I
GUARD
EARTH
TO/FROM HIGH VOLTAGE/ HIGH CURRENT ASSEMBLY
B CURRENT
I HV
P LOCK HI
TO OSCILLATOR ASSY
CLK*
CLK
LOW LEVEL 8MHz CLOCK FROM GUARD CROSSING (NOT SHOWN)
B IN
B FB
RCOM
4K
40K
4K
40K
10-10KΩ
RCOM FROM DAC
DAC OUT LO
OSC SENSE LO
OS COM
B CURRENT
INT OUT HI
HI-RES ON/OFF
CLK
CLK*
8MHz
÷ 4
U14
2MHz
÷ 2000
U16
PHASE DET.
PROG.
FILTER 4 POLE, 10Hz
6-12MHz
VCO
PHASE LOCK TO OSC. ASSY
÷ 2
U21
20Hz TO 2.4MHz
5-500K PROG. DIVIDER
VCO DISABLE
Q15
HI-RES ON/OFF
CURRENT SECTION
CURRENT / HI RES ASSEMBLY
ANALOG SECTION BLOCK DIAGRAM PAGE 2 MFCPG2
8
7
6
5
4
3
2
1
D
C
B
A

Figure 2-3. Analog Section Block Diagram, Part 2

2-12. Wideband AC V Functional Description (Option -03)

The Wideband AC Voltage module (Option -03) consists of the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5). There are two wideband frequency ranges:

- 10 Hz to 1.1 MHz
- 1.2 MHz to 30 MHz

During operation between 10 Hz and 1.1 MHz, output from the Oscillator Output assembly is routed to the Wideband Output assembly where it is amplified and attenuated to achieve the specified amplitude range. The output is connected to the 5700A front panel WIDEBAND connector. Operation between 1.2 MHz and 30 MHz works the same way, except the input to the Wideband Output assembly is the ac signal from the Wideband Oscillator assembly.

2-13. DC Current Functional Description

DC current is generated in five ranges:

- 20 uA - 220 uA
- 220 uA - 2.2 mA
- 2.2 mA - 22 mA
- 22 mA - 220 mA
- 2.2A

All current ranges except 2.2A are generated by the current portion of the Current/Hi-Res assembly. These currents are created by connecting the output of the DAC assembly, set to the 22V range, to the input of the Current assembly. The Current assembly uses this dc voltage to create the output current. The current output can be connected to the AUX CURRENT OUTPUT binding post by relays on the Current assembly, to the OUTPUT HI binding post by relays on the Current, Switch Matrix, and Analog Motherboard assemblies, or to the 5725A via the B-CUR line by relays on the Analog Motherboard assembly and Rear Panel assembly.

The 2.2A range is an extension of the 22 mA range. The 22 mA range output from the Current assembly is amplified by a gain of 100 by the High Voltage/High Current assembly operating in conjunction with the Power Amp assembly and the High Voltage Control assembly. The 2.2A current range is routed back to the Current assembly where it is connected to either the AUX CURRENT OUTPUT binding post, the OUTPUT HI binding post, or the 5725A in the same manner as the lower current ranges.

2-14. AC Current Functional Description

AC current is created in the same manner as dc current, except the input to the Current assembly is the ac voltage from the Oscillator Output assembly set to the 22V range. The switching between ac and dc is carried out on the Switch Matrix, Oscillator Control, Oscillator Output, and DAC assemblies.

2-15. Ohms Functional Description

Two assemblies function as one to supply the fixed values of resistance:

- Ohms Main assembly (A10)
- Ohms Cal assembly (A9)

All of the resistance values except the 1 ohm, 1.9 ohm, and short are physically located on the Ohms Main assembly. The 1 ohm, 1.9 ohm, and short are physically located on the Ohms Cal assembly. The desired resistance is selected by relays on these Ohms assemblies and is connected to the 5700A binding posts by relays on the Analog Motherboard. The Ohms Cal assembly also contains the appropriate circuitry to enable the 5700A to perform resistance calibration. Once calibrated, the 5700A output display shows the true value of the resistance selected, not the nominal (e.g., 10.00031 kilohm, not 10 kilohm).

Four ohms measurement modes are available:

- For the two-wire configuration, measurement with or without lead-drop compensation sensed at the binding posts of the UUT (using the SENSE binding posts and another set of leads), or at the ends of its test leads is available for 19 kilohms and below.

- Four-wire configuration is available for all but the 100 megohm value.

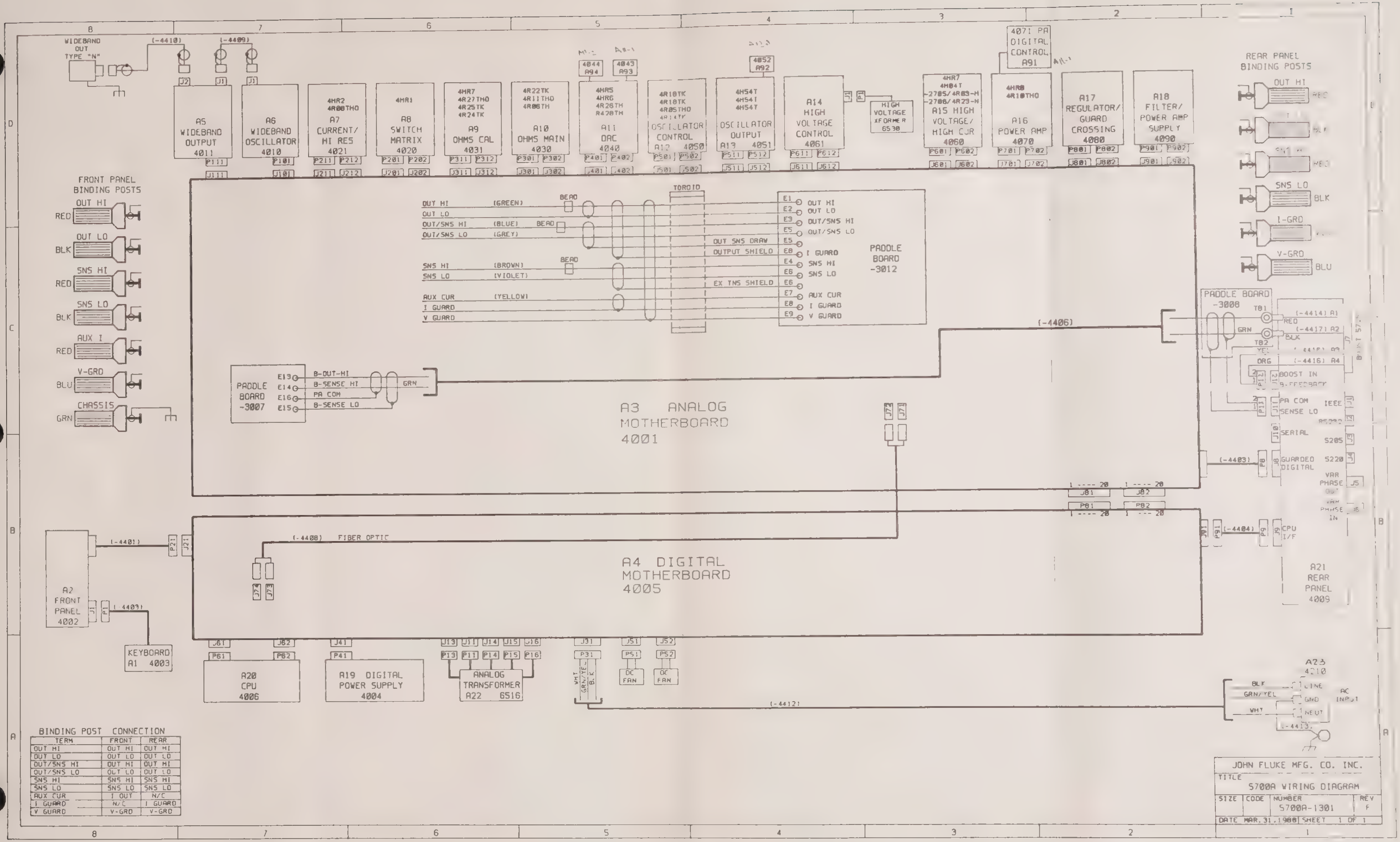
2-16. SYSTEM INTERCONNECT DETAILED CIRCUIT DESCRIPTION

The Motherboard assembly contains the Digital Motherboard assembly (A4), and the Analog Motherboard assembly (A3). These two Motherboards are mechanically fastened together with screws. They are electrically connected by connectors P81 and P82 on the Digital Motherboard and connectors J81 and J82 on the Analog Motherboard. AC voltage taps from the Transformer assembly (A22) are connected to the Analog Motherboard through these connectors. Refer to Figure 2-4 for an overview of system interconnections. Figure 2-4 continues on the reverse side, showing system grounds.

2-17. Digital Motherboard Assembly (A4)

The Digital Motherboard contains the line-select switches, line fuse, power switch, a fiber-optic transmitter (J73), and a fiber-optic receiver (J74). It also contains connectors for the Transformer assembly (A22), Digital Power Supply assembly (A19), CPU assembly (A20), Front Panel assembly (A2), Rear Panel assembly (A21), and the two 24V dc fans mounted in the chassis.

The fiber-optic receiver and transmitter provide the serial communication link between the CPU on the unguarded Digital Motherboard and the Regulator/Guard Crossing on the guarded Analog Motherboard.


WIDEBAND OUT TYPE "N"
(-4410)
(-4409)
J2
J1
J1
A5 WIDEBAND OUTPUT 4011
P111
J111
A6 WIDEBAND OSCILLATOR 4010
P101
J101
4HR2 4R08THO
A7 CURRENT/ HI RES 4021
P211 P212
J211 J212
4HR1
A8 SWITCH MATRIX 4020
P201 P202
J201 J202
4HR7 4R27THO 4R25TK 4R24TK
A9 OHMS CAL 4031
P311 P312
J311 J312
4R22TK 4R11THO 4R08TH
A10 OHMS MAIN 4030
P301 P302
J301 J302
4044 A94
4043 A93
4HR5 4HR6 4R26TH R420TH
A11 DAC 4040
P401 P402
J401 J402
4R18TK 4R18TK 4R05THO
OSCILLATOR CONTROL A12 4050
P501 P502
J501 J502
4052 A92
4H54T 4H54T 4H54T
OSCILLATOR OUTPUT A13 4051
P511 P512
J511 J512
A14 HIGH VOLTAGE CONTROL 4061
P611 P612
J611 J612
HIGH VOLTAGE XFORMER 6530
4071 PA DIGITAL CONTROL A91
4HR7 4H04T -2705/4R03-H -2706/4R23-N
A15 HIGH VOLTAGE/ HIGH CUR 4060
P601 P602
J601 J602
4HR8 4R10THO
A16 POWER AMP 4070
P701 P702
J701 J702
A17 REGULATOR/ GUARD CROSSING 4080
P801 P802
J801 J802
A18 FILTER/ POWER AMP SUPPLY 4090
P901 P902
J901 J902
REAR PANEL BINDING POSTS
OUT HI
SNS LO
BLK
I-GRD
V-GRD
BLU
FRONT PANEL BINDING POSTS
OUT HI
RED
OUT LO
BLK
SNS HI
RED
SNS LO
BLK
AUX I
RED
V-GRD
BLU
CHASSIS
GRN
OUT HI (GREEN)
BEAD
OUT LO
OUT/SNS HI (BLUE)
BEAD
OUT/SNS LO (GREY)
SNS HI (BROWN)
BEAD
SNS LO (VIOLET)
AUX CUR (YELLOW)
I GUARD
V GUARD
TOROID
OUT SNS DRAW
OUTPUT SHIELD
EX TNS SHIELD
E1 OUT HI
E2 OUT LO
E3 OUT/SNS HI
E5 OUT/SNS LO
E5
E8 I GUARD
E4 SNS HI
E6 SNS LO
E6
E7 AUX CUR
E8 I GUARD
E9 V GUARD
PADDLE BOARD -3012
PADDLE BOARD -3007
E13 B-OUT-HI
E14 B-SENSE HI
E16 PA COM
E15 B-SENSE LO
GRN
A3 ANALOG MOTHERBOARD 4001
J72 J71
(-4406)
PADDLE BOARD -3008
TB1
RED
GRN
BLK
TB2
YEL
ORG
(-4414) A1
(-4417) A2
(-4415) A3
(-4416) A4
J7
BOOST 57
P12 J12 BOOST IN
B-FEEDBACK
P11 J11 PA COM SENSE LO
IEEE J1
RS232 J2
J10 SERIAL
5205 J3
5220 J4
(-4403)
P8 J8 GUARDED DIGITAL
VAR PHASE OUT J5
VAR PHASE IN J6
1 ---- 20 J81
1 ---- 20 J82
P81 1 ---- 20
P82 1 ---- 20
J91 P91 (-4404) P9 J9 CPU I/F
A21 REAR PANEL 4009
(-4401)
P21 J21
(-4408) FIBER OPTIC
J74 J73
A4 DIGITAL MOTHERBOARD 4005
A2 FRONT PANEL 4002
J1 P1 (-4403)
KEYBOARD A1 4003
J61 J62 J41
P61 P62 P41
A20 CPU 4006
A19 DIGITAL POWER SUPPLY 4004
J13 J11 J14 J15 J16
P13 P11 P14 P15 P16
ANALOG TRANSFORMER A22 6516
J31
P31
WHT GRN/YEL BLK
J51 J52
P51 P52
DC FAN
DC FAN
(-4412)
A23 4210
BLK
GRN/YEL
WHT
LINE
GND
NEUT
AC INPUT
(-4413)
8 7 6 5 4 3 2 1
D C B A

BINDING POST CONNECTION

TERM	FRONT	REAR
OUT HI	OUT HI	OUT HI
OUT LO	OUT LO	OUT LO
OUT/SNS HI	OUT HI	OUT HI
OUT/SNS LO	OUT LO	OUT LO
SNS HI	SNS HI	SNS HI
SNS LO	SNS LO	SNS LO
AUX CUR	I OUT	N/C
I GUARD	N/C	I GUARD
V GUARD	V-GRD	V-GRD

JOHN FLUKE MFG. CO. INC.
TITLE 5700A WIRING DIAGRAM
SIZE CODE NUMBER 5700A-1301 REV F
DATE MAR.31,1988 SHEET 1 OF 1

Figure 2-4. System Interconnections

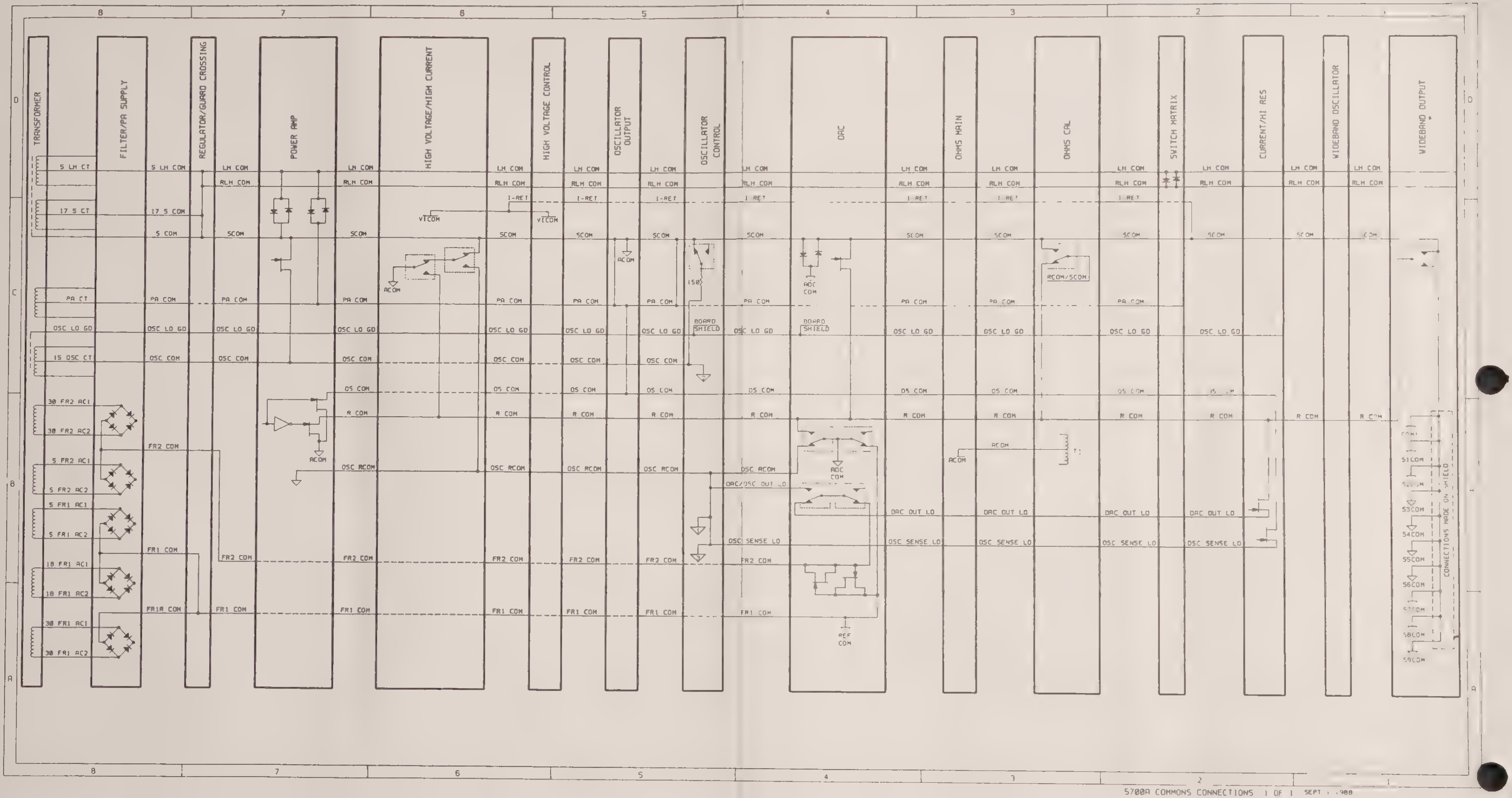

TRANSFORMER
FILTER/PA SUPPLY
REGULATOR/GUARD CROSSING
POWER AMP
HIGH VOLTAGE/HIGH CURRENT
HIGH VOLTAGE CONTROL
OSCILLATOR OUTPUT
OSCILLATOR CONTROL
DAC
OHMS MAIN
OHMS CAL
SWITCH MATRIX
CURRENT/HI RES
WIDEBAND OSCILLATOR
WIDEBAND OUTPUT
5 LH CT
5 LH COM
LH COM
RLH COM
17 5 CT
17 5 COM
5 COM
SCOM
I-RET
VTCOM
ACOM
PA CT
PA COM
OSC LO GD
15 OSC CT
OSC COM
OS COM
R COM
30 FR2 AC1
30 FR2 AC2
FR2 COM
5 FR2 AC1
5 FR2 AC2
5 FR1 AC1
5 FR1 AC2
FR1 COM
18 FR1 AC1
18 FR1 AC2
FR1A COM
30 FR1 AC1
30 FR1 AC2
OSC RCOM
150
BOARD SHIELD
ADC COM
DAC/OSC OUT LO
DAC OUT LO
OSC SENSE LO
REF COM
RCOM/SCOM
S1COM
S3COM
S4COM
S5COM
S6COM
S8COM
S9COM
CONNECTIONS MADE ON SHIELD
8
7
6
5
4
3
2
1
D
C
B
A
5700A COMMONS CONNECTIONS 1 OF 1 SEPT 1988

Figure 2-4. System Interconnections (cont)

2-18. Transformer Assembly (A22)

The Transformer assembly receives ac line inputs routed through the A4 Digital Motherboard. This assembly supplies outputs throughout the 5700A, all of which are routed through the A4 Digital Motherboard.

The Transformer assembly, the filter portion of the Filter/PA Supply assembly (A18), and the regulator portion of the Regulator/Guard Crossing assembly (A17) create the system power supply for all analog assemblies. The Transformer assembly also supplies ac voltages to the Digital Power Supply assembly which generates five regulated dc voltages for use by the CPU, Front Panel assembly, Rear Panel assembly, and the cooling fans.

2-19. Analog Motherboard Assembly (A3)

The Analog Motherboard contains the connectors for all assemblies in the guarded section of the calibrator. The Analog Motherboard also contains 13 relays, a fiber-optic transmitter, a fiber-optic receiver, a cable for binding post connections, and two cables for the interface to the Rear Panel assembly.

Table 2-1 lists Analog Motherboard connectors.

Table 2-1. Analog Motherboard Connectors

MOTHERBOARD CONNECTOR	CONNECTED TO ASSEMBLY
J101	Wideband Oscillator assembly (A6)
J111	Wideband Output assembly (A5)
J201 and J202	Switch Matrix assembly (A8)
J211 and J212	Current/Hi-Res assembly (A7)
J301 and J302	Ohms Main assembly (A10)
J311 and J312	Ohms Cal assembly (A9)
J401 and J402	DAC assembly (A11)
J501 and J502	Oscillator Control assembly (A12)
J511 and J512	Oscillator Output assembly (A13)
J601 and J602	High Voltage/High Current assembly (A15)
J611 and J612	High Voltage Control assembly (A14)
J701 and J702	Power Amplifier assembly (A16)
J801 and J802	Regulator/Guard Crossing assembly (A17)
J901 and J902	Filter/PA Supply assembly (A18)

The fiber-optic transmitter (J72) and the fiber-optic receiver (J71) provide the serial communication link between the Regulator/Guard Crossing assembly and the CPU assembly on the unguarded Digital Motherboard.

Control lines for relays K1-K10 and K13 on the Analog Motherboard assembly are generated on the Switch Matrix (A8) assembly. Control line RLY11*, which controls relay K11, is generated on the Current/Hi-Res assembly (A7). Control line RLY12*, which controls relay K12, is generated on the the Rear Panel assembly (A21).

Line INT OUT HI is the calibrator output for ac voltage operation in the 22V range and below, dc voltage operation in the 220V range and below, all resistance functions, and all ac/dc current ranges. Relays on the Current assembly route the current output to the AUX CURRENT OUTPUT binding post via the I OUT line if so selected by the operator. INT SENSE HI is the sense high path during these modes of operation. INT OUT HI is connected to the OUTPUT HI binding post through relay K1. INT SENSE HI is connected to the SENSE HI or OUTPUT HI binding post through relays K2 and K3.

Line HV OUT is the calibrator output for dc voltage operation in the 1100V range, and ac voltage operation in the 220V and 1100V ranges. Line HV SENSE is the sense high path during these modes of operation. HV OUT is connected to the OUT HI binding post through relays K9 and K1. HV SENSE is connected to the SENSE HI or OUTPUT HI binding post through relays K10, K2, and K3.

The 5725A Amplifier output is B OUT HI and the sense high path is B SNS HI. When the 5725A is active, B OUT HI is connected to the OUT HI binding post through relays K4 and K1. When the 5725A Amplifier is inactive, B OUT HI is connected to GUARD CHASSIS by relay K12. Line B SNS HI is tied to B OUT HI through diode clamps CR1 and CR2 and is connected to the SENSE HI or OUTPUT HI binding post through relays K5, K2, and K3.

The cable from the Motherboard to the binding posts consists of six insulated wires and six shields, each with its own drain wire. The OUT HI line, SENSE HI line, OUT/SENSE HI line and AUX CURRENT line each connect to an insulated wire and each has a shield around the wire. These shields are connected to OUT LO, SENSE LO, OUT/SENSE LO, and I/V GUARD, respectively. The I/V GUARD line is connected to I GUARD during operation in the current mode or V GUARD during operation in the voltage mode. This selection is done by relay K11.

When the 5700A is in standby, all binding posts are open-circuited except the GROUND binding post. In addition, GUARD CHASSIS is connected to S COM by K6. When in the operate condition, this connection is broken (K6 energized) and GUARD CHASSIS is connected to V GUARD via K7, which goes to the GUARD binding post, and to OUT LO via K8. GUARD CHASSIS is also connected to OSC LO GD by K13 except during ac or dc millivolt operation, when instead OSC LO GD is connected to S COM.

2-20. Front/Rear Binding Posts

An internal cable can be configured to enable either the front panel or rear panel binding posts. When compared to front panel binding posts, the rear panel provides the same OUTPUT HI, OUTPUT LO, SENSE HI, SENSE LO, AND V GUARD functions. Also, the rear panel provides an I GUARD (current guard) connection for use when the 5700A is supplying low-level ac current through a long cable. Use of the I GUARD connection removes errors introduced by leakage through such cables. The rear panel binding posts do not provide an AUX CURRENT OUTPUT connection. The procedure to disable the front panel binding posts and enable the rear panel binding posts is to be done at Service Centers, although it is described in this manual in Section 4.

2-21. Rear Panel

The Rear Panel assembly provides physical and electrical connections for the auxiliary amplifiers, along with RS-232-C and IEEE-488 interface connections. Relays on the Rear Panel assembly are used as the interfaces for the 5205A, 5215A, 5220A, or 5725A amplifiers, or for switching the PHASE LOCK IN and VARIABLE PHASE OUT signals.

Three Auxiliary Amplifiers can be physically connected to the Rear Panel assembly of the 5700A: the 5725A at J7, the 5220A at J4, and either 5205A or 5215A at J3. Only one amplifier can be in use at one time.

- The Rear Panel assembly provides relay switching for 5725A signals. Voltage outputs from the 5725A are routed to the binding posts on the 5700A. Current outputs are sourced at the 5725A OUTPUT binding posts. An alternate configuration is also available, allowing for routing of 5700A current outputs to the 5725A OUTPUT binding posts.

- When the 5220A (current output) is selected via the front panel, the output of the 5700A is routed to connector J4 on the rear panel, which is the interface to the 5220A.

- When the 5205A (ac and dc volts) or 5215A (ac volts only) function is selected via the calibrator keyboard, the output of the calibrator is routed to connector J3 (pins 1, 9, 2, and 10) on the Rear Panel assembly.

2-22. Power Supply

The Filter/PA Supply assembly (A18) incorporates two sections. The first section contains filters and regulators for some of the in-guard low-voltage supplies, and the second contains the power supply for the Power Amplifier output. Theory for each section is discussed separately.

2-23. DIGITAL SECTION DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of each assembly in the digital section are provided here. Simplified schematics and block diagrams are provided to supplement the text.

2-24. Digital Power Supply (A19)

The Digital Power Supply assembly receives ac voltages from the transformer and provides five regulated dc voltages for use by the CPU, Front Panel assembly, Rear Panel assembly, and the cooling fans. All power supply voltages are referenced to COMMON, which is the transformer center tap for the ± 12V supplies. Test points at the top of the assembly can be used to check unregulated input voltages, and regulated dc output voltages.

Table 2-2 lists the supplies generated by the Digital Power Supply.

Table 2-2. Supplies Generated by the Digital Power Supply

SIGNAL NAME	TEST POINT	NOMINAL OUTPUT	TOLERANCE	CURRENT LIMIT	RATED OUTPUT
+75V OUT	TP2	73V	8%	121 mA	100 mA
+35V OUT	TP5	35V	7%	52 mA	40 mA
+12 VOLTS	TP8	12V	5%	1.5A	700 mA
-12 VOLTS	TP10	12V	5%	1.5A	450 mA
+5V	TP12	5.2V	5%	2.4A	2.0A
COMMON	TP13				

2-25. +5V POWER SUPPLY

The unregulated +5V supply uses CR25-CR28 in a full-wave rectifier configuration with filter capacitors C12, C13, and C14. Capacitors C20 and C21 filter out high-frequency noise. Inductor L8 is a common-mode choke and C11 is a bypass capacitor. The regulator is fused by 3.15A slow-blow fuse F5.

The regulated +5V is generated by three-terminal low-dropout +5V regulator U3 with heat sink. The regulator's output voltage is increased about 0.2V by CR35, a germanium diode connected between the regulator's ground pin and COMMON. Capacitor C14 is for bypass. Capacitor C23 filters out high-frequency noise. Diode CR29 protects the regulator against input shorts, and diode CR30 protects the regulator from reverse voltage. Inductor L7 and C16 further filter the output to P41.

2-26. ± 12V POWER SUPPLIES

A full-wave rectifier made of diodes CR17-CR20 and filter capacitors C6 and C7 generate the unregulated +12V and -12V supplies. AC inputs are fused by F3 and F4, both 2A slow blow.

The regulated +12V supply is generated by a three-terminal +12V regulator U1 with heat sink. Capacitors C5 and C9 are for bypass. Diode CR21 protects the regulator from input shorts, and diode CR23 protects the regulator from reverse voltage. Capacitor C22 filters out high frequency noise.

Three-terminal -12V regulator U2 with heat sink generates the regulated -12V supply. Capacitors C8, C10, and C19 are for bypass. Diode CR22 protects the regulator from input shorts, and diode CR24 protects the regulator from reverse voltage.

Inductors L3-L6 filter the regulated outputs. R7 further isolates the ±12V FAN lines from the ±12V power lines. The +12V FAN and -12V FAN lines power the two 24V dc fans inside the calibrator.

2-27. +35V POWER SUPPLY

The +35V power supply powers the grid drivers and anode drivers on the front panel output display circuitry.

A full-wave rectifier made of diodes CR9-CR12 and filter capacitor C3 generate the unregulated +35V supply. Its input is fused by F2, a 0.125A slow-blow. Capacitor C18 is for bypass. Capacitor C25 filters out high frequency noise.

Zener diodes VR14, VR15 and transistor Q5 generate the +35V regulated output. Zener diodes VR14 and VR15 (both 18V) make up the control element which sets the output voltage. Transistor Q5 is used as an emitter follower. CR13 is the constant current source supplying current to the zener diodes and the base of Q5. Components R5 and Q6 make up the current-limiting circuit. During an over-current condition, the voltage drop across R5 turns Q6 on, thus drawing current away from the base of Q5 and limiting current flow to the output. Diode CR16 protects this circuit from reverse voltage and C4 is a bypass capacitor. Inductor L2 filters the regulated output. Resistor R13 is a bleed-off resistor for C3.

2-28. +75V POWER SUPPLY

The +75V power supply powers the grid drivers and anode drivers on the front panel control display circuitry.

A full-wave rectifier made of diodes CR1-CR4 and filter capacitor C1 generate the unregulated +75V supply. Its input is fused by F1, a 0.315A slow-blow. Capacitor C17 is for bypass. Capacitor C24 filters out high frequency noise.

The +75V regulated output is generated by 36V zener diode VR6, 39V zener diode VR7, and transistors Q1 and Q3. Zener diodes VR6 and VR7 set the output voltage. Transistors Q1 and Q3, in a Darlington configuration for current gain, are used as an emitter follower. Transistor Q4, zener diode VR5, and resistors R2 and R3 make up the constant current source supplying current to the zener diodes and the base of Q3. Current limiting is performed by R1 and Q2 in the same manner as in the +35V supply. Diode CR8 protects the circuit from reverse voltage and C2 is a bypass capacitor. Inductor L1 filters the regulated output. Resistor R6 is a bleed-off resistor for C1.

2-29. +35V AND +75V SHUT-DOWN CIRCUIT

The +35V and +75V high voltage supplies are shut down when a fault occurs in the control display refresh circuitry. This shut-down circuit prevents the Control Display and Output Display from burning out, and also verifies that the master clock is generating control signals for both displays.

During normal operation, 75VSD is low, turning Q10 off. Line RESETL pulls the base of Q9 high through R9, turning Q9 on. This action in turn pulls the junctions of CR31-CR32 and CR33-CR34 low, turning Q7 and Q8 off. The +75V and +35V constant-current sources can then supply the appropriate zener diodes and drive the bases of the respective emitter followers.

When a display refresh fault occurs, the 75VSD line on P41 pin 5C, coming from the Front Panel assembly, goes high. this signal, pulled up by R4, drives the base of Q10 through base resistor R11. Transistor Q10 then saturates, pulling the base of Q9 near ground, turning Q9 off. On power-up or during a CPU reset, the RESETL signal is low, pulling the base of Q9 near ground through R9, also turning Q9 off. Resistor R12 is a turn-off resistor for Q9. Diodes CR31 and CR33 are in a wired-OR configuration. When Q9 is saturated (on), CR31 and CR33 pull their respective junctions to CR32 and CR34 near ground, turning Q7 and Q8 off. When Q9 is off, the junctions are pulled high through R8 and R10, saturating Q7 and Q8 (on). When on, Q7 removes the base drive from Q3, shutting down the +75V supply. Similarly, Q8 removes the base drive from Q5, shutting down the +35V supply.

Diodes CR32 and CR34 simply insure that Q7 and Q8 are off when Q9 is on. Resistor R8 guarantees that Q7 will hold the +75V supply off until it drops below 15.6V, and R10 holds the +35V supply off to 7.8V.

2-30. CPU (Central Processing Unit, A20)

The CPU (Central Processing Unit) for the 5700A is a single-board computer based on a 68HC000 microprocessor. The CPU assembly communicates with the Guarded Digital section, the Front Panel assembly, and the Rear Panel assembly. The board can be divided into three primary areas:

- The microprocessor and its support circuitry
- Memory
- Peripheral chips and I/O interfaces

Microprocessor support circuitry consists of a power-up and reset circuit, clock generation, a watchdog timer, address decoders and dtack generator, bus error timeout, and interrupt controller.

Figure 2-5 is a block diagram of the CPU assembly. Table 2-3 is a glossary of the acronyms used in the text and schematic for the CPU assembly.

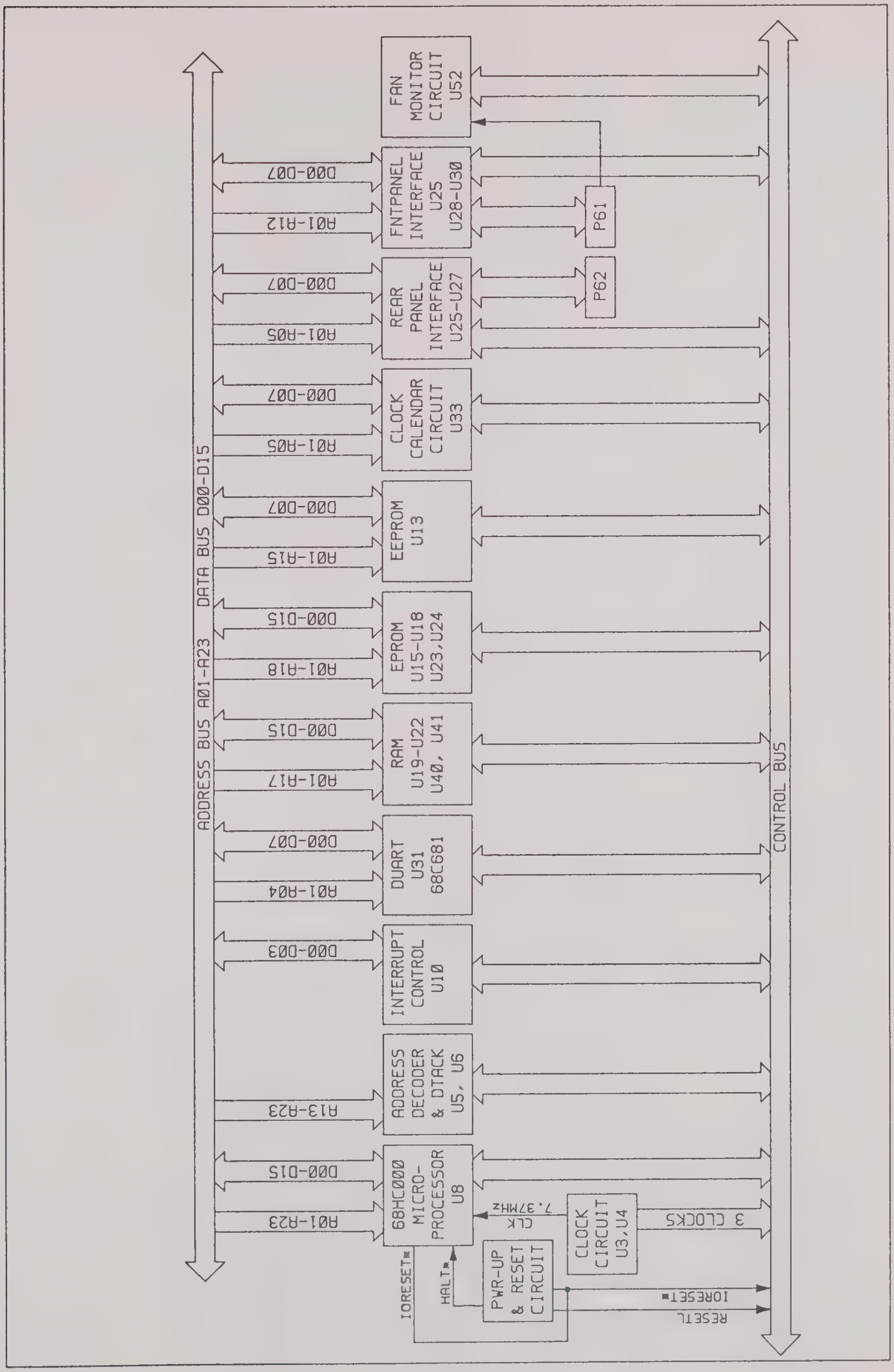

ADDRESS BUS A01-A23   DATA BUS D00-D15
CONTROL BUS
FAN MONITOR CIRCUIT U52
FNTPANEL INTERFACE U25 U28-U30
D00-D07
A01-A12
P61
REAR PANEL INTERFACE U25-U27
D00-D07
A01-A05
P62
CLOCK CALENDAR CIRCUIT U33
D00-D07
A01-A05
EEPROM U13
D00-D07
A01-A15
EPROM U15-U18 U23,U24
D00-D15
A01-A18
RAM U19-U22 U40, U41
D00-D15
A01-A17
DUART U31 68C681
D00-D07
A01-A04
INTERRUPT CONTROL U10
D00-D03
ADDRESS DECODER & DTACK U5, U6
A13-A23
68HC000 MICRO-PROCESSOR U8
D00-D15
A01-A23
7.37MHz CLK
CLOCK CIRCUIT U3,U4
3 CLOCKS
PWR-UP & RESET CIRCUIT
HALT*
IORESET*
IORESET*
RESETL

Figure 2-5. CPU Assembly Block Diagram

Table 2-3. CPU Acronym Glossary

A01-A23	Address lines
ADCLKCS*	Clock/calendar (U33) chip select
AS*	Address strobe
BERR*	Bus error
BGACK*	Bus grant acknowledge
BR*	Bus request
BRPDRTINT*	Rear panel DUART interrupt
BRPDTK*	Rear panel data transfer acknowledge
BRPIEEEINT*	Rear panel IEEE-488 interrupt
CLKCALINT*	Clock/calendar interrupt
D00-D15	Data lines
DOGCLR	Dog clear (clears watchdog timer)
DOGINTH	Dog interrupt (interrupt from watchdog timer)
DRTDTK*	DUART data transfer acknowledge
DTACK*	Data transfer acknowledge
E	Enable for 6800 family devices (737.28 kHz clock)
EXDUARTINT*	External DUART Interrupt
FAN1	Signal monitoring fan 1
FAN2	Signal monitoring fan 2
FANINT*	Fan monitor interrupt
FC0	Function code output 0
FC1	Function code output 1
FC2	Function code output 2
FPDTK*	Front panel data transfer acknowledge
FRNTPNLCS*	Front panel chip select
FRNTPNLEN*	Front panel enable
GCDRTCS*	Guard crossing DUART chip select
GCDUARTINT*	Guard crossing DUART interrupt
INTRCNTL1	Interrupt control 1
INTRCNTL2	Interrupt control 2
IPL0*	Interrupt priority level 0
IPL1*	Interrupt priority level 1
IPL2*	Interrupt priority level 2
KEYBRDINT*	Keyboard interrupt
LDS*	Lower data strobe
MISCCS*	Miscellaneous chip select enable (upper address bits decoder)
NVMCS*	Nonvolatile memory chip select
NVMOE*	Nonvolatile memory output enable
PROM0CS*	PROM 0 chip select (U15 and U16)
PROM1CS*	PROM 1 chip select (U17 and U18)
PROM2CS*	PROM 2 chip select (U23 and U24)
PSFAILINT*	Power supply fail interrupt
RAM0CS*	RAM chip select (U19 and U20)
RAM1CS*	RAM chip select (U21 and U22)
RAM2CS*	RAM chip select (U40 and U41)
R/WR*	Read/write
RDINT*	Read interrupt
RDL*	Read data lower
RDU*	Read data upper
RDY/BSYL	Ready/busy

Table 2-3. CPU Acronym Glossary (cont)

RPSEL*	Rear panel chip select
RRPNLEN*	Rear panel enable
RXDA	Receive Data Port A
RXDB	Receive Data Port B
SCLK	Serial clock
TXDA	Transmit Data Port A
TXDB	Transmit Data Port B
UDS*	Upper data strobe
WRL*	Write lower
WRU*	Write upper
XDUARTCS*	External DUART chip select

2-31. POWER-UP AND RESET CIRCUIT

The power-up and reset circuitry consists of line monitor chip U1, C5, C6, CR1, R3, Z3, switch SW1, and inverters on U2. This circuit provides a 195 ms reset pulse at power-up or upon pressing and releasing SW1, placing the CPU assembly in a known safe condition. If the power supply glitches or falls below 4.55V ±0.05V, U1 resets the 5700A. The reset pulse duration is determined by C5. Note that SW1 performs a different function than the front panel RESET button. SW1 is a hardware reset that is hard-wired to and directly read by the microprocessor. The front panel RESET button is a software reset; it tells the system software to restore the 5700A configuration to a default condition.

The heart of this circuit is the line monitor chip U1. On power-up or when SW1 is pushed, U1 forces an active-low reset pulse on RESETL and an active-high pulse on RESET. RESETL helps to prevent accidental writes to EEPROM and drives an inverter in U2 to turn off LED CR1. CR1 indicates that the +5V supply is on and that the CPU is operating, i.e. not reset. RESETL also resets the rear panel assembly. The other output, RESET, drives two inverters in U2. One of these inverters provides HALT*. The other generates IORESET*, which drives the processor's RESET, and provides a reset for the front panel interface and DUARTs (dual universal asynchronous receiver/transmitter) circuitry.

2-32. CLOCK GENERATION

The clock generation circuit uses components Y1, Y2, U3, U4, R4, R5, C8, C9, and E5. The crystal Y1, along with the resistors, capacitors, and an inverter in U3 generates the 7.3728 MHz primary system clock CLK. This system clock is used by the processor and is divided down by a binary counter (U4) for clocks of 3.6864 MHz, 28.8 kHz, and 450 Hz. The 450 Hz clock is used by the watchdog timer, the 28.8 kHz is used by U6 in the decoding circuit, and the 3.6864 MHz is used by the DUARTs, and the clock filter circuit. Jumper E5 allows for selection of the alternate oscillator (Y2) as the system clock.

2-33. WATCHDOG TIMER

The watchdog timer circuitry uses a 74HC4020 binary counter (U11) to divide the 450 Hz from the clock generation circuit to produce interrupt DOGINTH, signifying that the system may be locked up. This interrupt is generated 1.14 seconds after the last DOGCLR2 signal from interrupt controller U10. Therefore, DOGCLR2 must occur more often then every 1.14 seconds to clear U11 and prevent the watchdog interrupt. Generation of DOGCLR2 is under software control. The watchdog timer can be disabled by cutting jumper E1.

2-34. ADDRESS DECODING AND DTACK

Two Programmable Logic Devices (PLDs) accomplish address decoding and dtack (data acknowledge) generation. ICs U5 and U6 provide chip selects and generate acknowledgement signals for those devices without data acknowledge lines. IC U5 receives dtack signals from the asynchronous devices and ORs these signals together to form DTACK*. Table 2-4 is the memory map for the system. It shows the chip select, address range, and notes whether AS* (address strobe) or LDS* (lower data strobe) is required.

Table 2-4. CPU Memory Map

CHIP SELECT	READ/WRITE	ADDRESS RANGE	AS* OR LDS* REQUIRED?
PROMOCS*	R	0 - 3FFFF	no
PROM1CS*	R	40000 - 7FFFF	no
PROM2CS*	R	80000 - BFFFF	no
RAMOCS*		600000 - 60FFFF	no
RAM1CS*		610000 - 61FFFF	no
RAM2CS*		620000 - 623FFF	no
NVMCS*	R/W	C00000 - CFFFFF	no
MISCCS*	R/W	D00000 - DFFFFF	no
RPSEL*	R/W	D00000 - D01FFF	LDS*
RPDUARTCS*	R/W	D00000 - D0001F	LDS*
RPIEEECS*	R/W	D00020 - D0002F	LDS*
Y52XXRD*	R	D00030 - D00031	LDS*
Y5205WR*	W	D00032 - D00033	LDS*
Y5220WR*	W	D00034 - D00035	LDS*
FRNTPNLCS*	R/W	D02000 - D03FFF	AS*
OTDCS*	R/W	D02000 - D027FF	AS*
DMDCS*	R/W	D02800 - D02FFF	AS*
ENCODERCS*	R	D03000 - D033FF	AS*
ENCODERRESET*	W	D03000 - D033FF	AS*
LED_OUTPUT_CNTRL	R	D03400 - D037FF	AS*
LED_LATCH_EN	W	D03400 - D037FF	AS*
KEYBOARDCS*	R/W	D03800 - D038FF	AS*
GCDRTCS*	R/W	D04000 - D05FFF	LDS*
XDUARTCS*		D06000 - D07FFF	LDS*
RDINT*	R/W	D08000 - D09FFF	AS*
DOGCLR	W	D08000 - D09FFF	even only, AS*
ADCLKCS*		E00000 - EFFFFF	AS*

2-35. INTERRUPT CONTROLLER

PLD U10 is the priority interrupt controller. The interrupt controller reads incoming interrupts and interrupt control lines, then encodes the highest priority interrupt into the interrupt level for the 68HC000. When the 68HC000 responds to an interrupt request, it asks the interrupt controller for an 8-bit vector that corresponds to the pending interrupt of highest priority. The interrupt controller responds with the 4 LSB's of the vector according to how it is programmed. The 4 MSB's are pulled up on resistor network Z1. Table 2-5 shows the interrupts, their priority levels, and vectors.

Table 2-5. CPU Interrupts, Priorities, and Vectors

INTERRUPT	PRIORITY LEVEL	VECTOR (HEX)	
NMI	7	-	(not used)
DOGINTH	6	F4	
BRPDRTINT*	5	F6	
GCDUARTINT*	5	F7	
EXDUARTINT*	5	F8	
CLKCALINT*	4	F5	
BRPIEEEINT*	4	F9	
KEYBRDINT*	3	FA	
BPSFAILINT*	2	FB	
FANINT*	0	FF	(not used)
RDY/BSYL	0	FF	(not used)
No interrupt	0	FF	

2-36. GLUE LOGIC

ICs U2, U3, and U9 form the glue logic circuit, which keeps various CPU functions running properly. The four OR gates in U9 and an inverter in U3 use control signals UDS*, LDS*, and R/WR* from the microprocessor to generate control signals WRU*, WRL*, RDL*, and RDU*.

2-37. RAM (RANDOM-ACCESS MEMORY)

Random-access memory is contained in three pairs of sockets, U19 and U20, U21 and U22, and U40 and U41. These sockets accommodate either 32K x 8 or 128K x 8 static CMOS RAM modules (32KB or 128 KB each). The 5700A is shipped with U19-U22 installed, using 32K x 8 parts and providing 128 KB of static RAM.

2-38. ROM (READ-ONLY MEMORY)

Read-only memory is contained in three pairs of sockets, U15-U16, U17-U18, and U23-U24. These sockets accommodate 27010 EPROMS, 128K x 8 devices (128 KB each). Jumpers allow 256 KB devices to be used in their place. The 5700A is shipped with U15-U18 installed, providing 512 KB of EPROM.

2-39. ELECTRICALLY-ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)

IC U13 is an EEPROM. The socket accommodates a 32K x 8 device (32 KB of storage.) A jumper is provided to allow an 8K x 8 (8 KB) device to be used in place of the 32 KB device. The 5700A is shipped with a 32KB EEPROM installed.

The EEPROM requires protection against inadvertent writes during power-up and power-down sequences, which could corrupt calibration constants stored there by the 68HC000. The 32 KB EEPROM provides for software-controlled protection against accidental writes.

Hardware is also used to further ensure data integrity. The EEPROMs are designed so that writes to the device are prevented by holding the output enable line (NVMOE*) low. Diodes CR5, CR6 and CR8, together with resistor R6, perform a wired-OR function for three signals that control NVMOE*. Components R6, CR6 and C17 hold NVMOE* to a valid logic low for typically 37.3 ms during power-up; 26.8 ms minimum, 49.6 ms maximum. Diode CR7 provides a discharge path for C17 on power-down, allowing the operator to quickly turn the 5700A off then on again, without interfering with the power-up charge time of the capacitor. Diode CR8 allows the normal microprocessor read of the device to take place. And diode CR5 allows power monitoring IC U1 to hold NVMOE* low when the +5V power supply drops below 4.5V on power-down or during power glitches.

2-40. DUART (DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER) CIRCUIT

The 68C681 DUART (U31) has several functions. Its primary function is to provide the asynchronous serial lines that communicate with the Guarded Digital Controller over the fiber-optic path off the Digital Motherboard. A 75451 driver chip (U32) drives the fiber-optic transmitter on the digital Motherboard.

The DUART has 8 output lines that perform various functions. INTRCNTL1 and INTRCNTL2 go to the interrupt controller and are fed back to the DUART inputs. These are used by the interrupt controller to enable certain interrupts. Line SCLK is a test output of the channel A serial clock.

The DUART monitors the EEPROM ready signal and the FANINT* signal. It also has a spare serial channel that goes to connector J5. Components U44 and U43 convert the TTL-level signals at the DUART to RS-232-C-level signals at J5.

The DUART generates its own dtack signal, DRTDTK*, which is used by U5 to generate system dtack, DTACK*. A second DUART, U42, with associated RS-232-C drivers and receivers is used only for test purposes. It generates its own dtack, wire-ORed to DRTDTK*.

2-41. CLOCK/CALENDAR CIRCUIT

Time and date information is stored in a battery-backed clock/calendar circuit consisting of 32.768 kHz crystal Y3, 3V lithium battery BT1, clock/calendar IC U33, and capacitors C10 and C11. The clock/calendar IC has the necessary circuitry internally to switch operation from the power supply to battery BT1. Pull-up resistors in Z5 off U33 are to ensure low power operation when the +5V supply is off. U33 generates CLKCALINT* under software control.

2-42. CLOCK FILTER CIRCUIT

The clock filter circuit generates a 3.6864 MHz 200 mV sine wave for the Rear Panel and Front Panel assemblies. This circuit buffers the 3.6864 MHz Clock with an inverter in U3. The circuit contains dc-blocking capacitor C80 which forms a high-pass filter with R81, two stages of a low pass LC filter (L80 and C81, L81 and C82), load resistor R81, transformer T51, and termination resistor R82.

2-43. CPU TO REAR PANEL INTERFACE

Components U25, U26, U27, and connector P62 interface the CPU to the rear panel. Bi-directional bus transceiver U26 buffers the data lines. Control signal R/WR* controls the transmission direction of the data lines, and RRPNLEN* is the chip enable. IC U25 buffers control lines BRPDRTINT*, BRPIEEEINT*, and BRPDTK*. U27, enabled by RRPNLEN*, buffers address line A01-A05 and control lines WRL* and R/WR*. Control lines RESETL, RPSEL*, TXDB, RXDB, and XMT go directly to connector P62.

2-44. CPU TO FRONT PANEL INTERFACE

Components U25, U28, U29, U30 and connector P61 interface the front panel to the CPU. Bi-directional bus transceiver U30 buffers the data lines. Control signal R/WR* controls the transmission direction of the data lines, and FRNTPNLEN* is the chip enable. IC U28, enabled by FRNTPNLEN*, buffers address lines A05-A12. IC U29, also enabled by FRNTPNLEN*, buffers address lines A01-A04 and control line R/WR*. Two sections of U25 in parallel buffer IORESET*, providing twice the drive current of a single section, generating BRESET*. Three other sections of U25 buffer FPINT*, FPDTK*, and PSFAILINT*. Control line FRNTPNLCS* goes directly to connector P61.

2-45. FAN MONITOR

The fan monitor circuit detects whether one of the two fans is fully or partially shorted, open-circuited, or drawing excessive current. Current-sense resistors on the Digital Motherboard send analog signals FAN1 and FAN2 to the CPU through P61. FAN1 is subtracted from FAN2 in U52D, and the difference is amplified before being sent to a window comparator made up of U52B and U52C (plus associated resistors). Capacitors C12 and C13 act as low-pass filters for the two signals, preventing spurious noise from interfering with detection circuitry.

When the output of U52D is greater than +5V, the output of U52B goes low (to about -11V); otherwise the output is high (about +11V). U52A takes the +5V and generates a -5V reference for comparator U52C. When the output of U52D is more negative than -5V, the output of U52C goes low (to about -11V); otherwise the output is high (about +11V). The outputs of U52B and U52C are wire-ORed through CR2 and CR3, using R52 and R53 to limit current sunk by the comparators when their respective outputs are low. Schottky barrier diode CR4 converts the -11V outputs of the comparators, when either is low, to a TTL-level logic low, which is the active (true) level of FANINT*.

When both fans are functioning properly, diodes CR2 and CR3 are reverse-biased, effectively taking the comparators out of the circuit. At this point, R51 pulls FANINT* to a valid TTL-level logic high, the inactive state of FANINT*. R51 and CR4 level-shift the ±11V signal to valid TTL levels.

Signal FANINT* goes to DUART U31 and to the interrupt controller U10 for further processing. System software monitors FANINT* through U31, and can program the DUART to generate a GCDUARTINT* interrupt signal on FANINT* going low.

2-46. Front Panel Assembly (A2)

The Front Panel assembly, operating in conjunction with the Keyboard assembly (linked by a cable), is the operator interface to the 5700A. This assembly contains two separate vacuum-fluorescent displays: the Control Display and the Output Display. Each display has its own control, high voltage drive, and filament-switching circuits. This assembly also contains clock regeneration, refresh failure detect, keyboard scanner, rotary knob encoder, LED drive, and decoding and timing circuitry.

Connector J2 connects this assembly with the Keyboard/Encoder. Connector J1 interfaces with the CPU assembly and the Digital Power Supply assembly via the Digital Motherboard.

2-47. CLOCK REGENERATION CIRCUITRY

To minimize EMI (electro-magnetic interference), the Front Panel assembly accepts a low-level sine-wave (approximately 200 mV p-p) 3.6864 MHz clock from the CPU assembly and converts it to a TTL-acceptable level. This is done by high-speed differential comparator (U7A), operating on incoming signals 3.6864MHZCLK and 3.6864MHZCLK*. The output of U7A is the input to U8 and is also inverted by U11B to create the 3.6864 MHz clock signal CLOCK. Twelve-stage binary counter U8 divides the 3.6864 MHz clock by eight and U11A inverts the signal to create 460.8 kHz. The master clock is further divided by U8, which outputs a 900 Hz signal on pin 1. These clocks provide system timing for the other ICs on the assembly. A -5.2V supply for U7 is provided by VR5, with C64 acting as the supply bypass.

2-48. REFRESH FAILURE DETECT CIRCUITRY

If a clock failure were to occur, the refresh cycles of the vacuum-fluorescent displays would be interrupted. This condition could damage the tubes if not immediately detected. Refresh failure detect circuitry monitors the GRIDDATA output from the last high voltage driver (U23) for the Control Display. This output (REFRESH) is used to clear a watchdog timer (U6) every refresh cycle. If the refresh is interrupted and GRIDDATA does not occur, the watchdog timer times out and latches U12. Flip-flop U12 generates control lines 75VSD and PSFAILINTR*. Control line 75VSD is routed to the Digital Power Supply assembly to shut down the +35V and +75V power supplies, thus preventing damage to the vacuum-fluorescent displays. Interrupt line PSFAILINTR* is used by PLD U3 to properly blank the Control Display and Output Display through DMDBLANK and OTDBLANK, and alerts the CPU that this failure has occurred.

2-49. DECODING AND TIMING CIRCUITRY

Main decoding and master timing functions for the front panel is accomplished by an EP900 PLD (Programmable Logic Device), U3. Two state machines control display refresh and filament switching. Filament switching is handled by two non-overlapping 57.6 kHz signals.

Signals GSTRBE and STROBE are master timing and synchronization signals used by the other ICs. Signal DMDBLANK controls the Control Display grid drivers, ABCLK and CDCLK control the Control Display anode drivers, and OTDBLANK controls the Output Display grid and anode drivers. Front panel DTACK and interrupt functions, and generation of the various chip select and reset signals are also provided by U3.

Table 2-6 is a memory map for the front panel.

Table 2-6. Front Panel Memory Map

NAME	READ/WRITE	ADDRESS
OTDCS*	R/W	D02000-D027FF
DMDCS*	R/W	D02800-D02FFF
ENCODERCS*	R	D03000-D033FF
ENCODERRESET*	W	D03000-D033FF
LED_OUTPUT_CNTRL	R	D03400-D037FF
LED_LATCH_EN	W	D03400-D037FF
KEYBOARDCS*	R/W	D03800-D03BFF

2-50. CONTROL DISPLAY CIRCUITRY

Control display circuitry consists of a 26-row by 256-column vacuum-fluorescent dot matrix display under the control of PLD U4, four high voltage grid drivers (U20-U23), four high voltage anode drivers (U16-U19), a filament switching circuit, and 1K x 8 (1 KB) dual-port RAM U1.

This display is divided into 129 grids; alternate grids contain two anode columns lettered B C or D A. Grid G129 and column C in grid G128 are not used. Each column contains 26 individual anodes.

IC U4 is an EP900 Programmable Logic Device (PLD). It provides the timing and control signals for control display circuitry. Display data written by the microprocessor into the Control Display's dual port RAM (U1) is read by U4 and sent serially to the high voltage anode drivers. Both the anode and grid drivers are serial TTL-level input, 32-bit parallel high voltage output devices. IC U4 also controls the grid timing and display refresh.

```
**************      *************      *************
*            *      *           *      *           *
*   B    C   *      *   D   A   *      *   B   C   *
*            *      *           *      *           *
*     G4     *      *    G5     *      *    G6     *
*            *      *           *      *           *
**************      *************      *************
```

Adjacent columns in adjacent grids are driven, while the opposite columns are turned off. For instance, grid G4 contains columns B and C, and grid G5 contains columns D and A. G4 and G5 are driven simultaneously while anode columns G4-C and G5-D are activated, and G4-B and G5-A are driven off. Next, grids G5 and G6 are driven simultaneously, while columns G5-A and G6-B are activated, and G5-D and G6-C are driven off. This pattern is repeated for all 128 grids at a refresh rate of about 75 Hz.

This particular scheme was selected because of the way the anode drivers are loaded with display data. Both the A and C (U16 and U18), and B and D (U17 and U19) anode drivers' input registers are latched with the same data, while the output drivers are appropriately enabled and displaying the data previously strobed to the driver outputs from the input registers. The input register data is strobed to the output drivers while all of the drivers are disabled, or blanked. Following this, either the A and B drivers are enabled to display the A-B data, when the C and D drivers, latched with A-B data, are disabled, or the C and D drivers are enabled to display the C-D data, when the A and B drivers, latched with C-D data, are disabled.

Control display filament driver circuitry consists of transistors Q1 through Q6 and zener diodes VR1 and VR2, with associated resistors. The transistors are driven by 7406 open collector drivers U13B and U13A. These drivers are controlled by AOUT and BOUT. AOUT and BOUT are synchronous, non-overlapping, three-eighths duty cycle, 57.6 kHz timing signals generated by U3. Each signal is alternately active high for 6.51 us, with a dead time between active signals of about 2.17 us to allow for turn-off times of the drive transistors. When AOUT is high, U13B turns Q2 and Q4 on. Q4 turns Q6 on, providing a path for the filament current through Q2 and Q6. Zener diode VR2 provides the dc voltage offset necessary for proper filament operation. Then when BOUT is high, U13A turns Q1 and Q3 on. Q1 turns Q5 on, providing a path for the filament current through Q3 and Q5, effectively reversing the direction of the voltage driving the filament. Zener diode VR1 provides the dc voltage offset necessary for proper filament operation.

PLD U4 also generates the 225 Hz square-wave SCAN signal used by PLD U9 to control front panel keypad scanning and key debounce.

Dual-port RAM U1 contains all the Control Display data written by the 68HC000 microprocessor on the CPU board. PLD U4 contains a 10-bit address counter which is used by U4 to read the contents of U1. U1 provides a BUSYD signal to U3, which is active low whenever the CPU and U4 try to access the same RAM location at the same time. If the microprocessor attempts to write to the RAM location that U4 is reading (as it refreshes the DMD), U3 uses BUSYD to hold off DTACK to the microprocessor. This prevents the written data from being lost. The other busy signal, generated when U4 attempts to read from a location being written to by the microprocessor, is ignored. Losing display data for one refresh cycle is insignificant.

2-51. OUTPUT DISPLAY CIRCUITRY

Output display circuitry consists of a custom 2-row, 22-character vacuum-fluorescent display under the control of PLD U5. The circuit contains high voltage grid driver U15, high voltage anode driver U14, a filament switching circuit, and a 1K x 8 (1 KB) dual-port RAM, U2.

The custom display is divided into 24 grids. The 22 characters are made up of fourteen seven-segment digits and eight 14-segment characters.

IC U5 is an EP900 PLD, programmed to provide the timing and control signals for the output display circuitry. Display data written by the microprocessor into the Output Display's dual-port RAM U2, is read by U5 and sent serially to the high voltage anode driver. Both the anode and grid drivers are serial TTL-level input, 32-bit parallel high voltage output devices. Only 31 anode driver outputs and 24 grid driver outputs are used, the remaining high voltage outputs are left unconnected. IC U5 also controls grid timing and display refresh.

A special refresh scheme is used by the Output Display to intensify a specific digit to be displayed. This feature is used by the 5700A when in Error Mode, while editing a value displayed on the Output Display. The digit selected for editing is brighter than the other digits. To accomplish this, U5 monitors data it reads from the dual-port RAM. Following the entry of the fourth data byte to the input registers of the anode driver, the registers are strobed to the high voltage output drivers, then the drivers are enabled. If data bit D7 of the fourth byte is low, the state machine in U5 simply goes on to refresh the next digit at the normal rate of approximately 200 Hz. If, however, bit D7 of the fourth byte is high, the state machine enters a delay routine that adds about 625 us to the normal 5 ms anode and grid on-time, thereby intensifying the digit. Unlike the Control Display, only one grid at a time is turned on.

Output display filament driver circuitry consists of transistors Q7-Q12 and zener diodes VR3 and VR4, plus associated resistors. The transistors are driven by 7406 open-collector drivers U13C and U13D. These drivers are controlled by AOUT and BOUT as in the Control Display. When AOUT is high, U13C turns Q8 and Q10 on. Q10 turns Q12 on, providing a path for the filament current through Q8 and Q12. Zener diode VR4 provides the dc voltage offset necessary for proper filament operation. Then when BOUT is high, U13D turns Q7 and Q9 on. Q7 turns Q11 on, providing a path for the filament current through Q9 and Q11, effectively reversing the direction of the voltage driving the filament. Zener diode VR3 provides the dc voltage offset necessary for proper filament operation.

Dual-port RAM U2 contains all the Output Display data written by the 68HC000 microprocessor on the CPU board. U5 contains a 7-bit address counter which U5 uses to read the contents of U2. U2 provides a BUSYO signal to U3, which is active low whenever the CPU and U5 try to access the same RAM location at the same time. If the microprocessor attempts to write to the same RAM location U5 is reading as it refreshes the Control Display, U3 uses BUSYO to hold off DTACK to the microprocessor. This prevents written data from being lost. The other busy signal, generated when U5 attempts to read from a location being written to by the microprocessor, is ignored. Losing display data for one refresh cycle is insignificant.

IC U5 also generates the FPINTR* (front panel interrupt, active low) signal sent to the 68HC000 microprocessor, telling it there is an encoder or keyboard interrupt. The interrupt inputs to U5, ENCODERINTR (encoder interrupt, active high) and KEYBOARDINTR (keyboard interrupt, active high), are generated by PLDs U24 and U9 respectively.

2-52. KEYBOARD SCANNER CIRCUITRY

The key matrix is scanned by PLD U9. It sequentially drives one of the eight columns for about 2.2 ms, then reads all six rows of the matrix on each column scan. When a key is pressed and the column associated with that key is scanned, the row associated with that key goes low. If the key is still pressed after a 6.6 ms debounce period, U9 generates signal KEYBOARDINTR. This signal goes to U5 where it generates FPINTR*, which interrupts the 68HC000 microprocessor. The microprocessor generates KEYBOARDCS* through PLD U3, causing U9 to output encoded row and column data on the data bus for the microprocessor to read. This also resets the keyboard interrupt.

The microprocessor controls the speaker, also referred to as the beeper. Writing a logic high on data line D6 to U9 enables the speaker, writing a logic low on D6 disables the speaker. When enabled, a 900 Hz square-wave signal generated by U8 is gated out to the speaker through U9.

2-53. KNOB ENCODER CIRCUITRY

Knob encoder circuitry consists of PLD U24 and resistors R22, R23, R26, and R27. The resistors configure the U24 knob inputs as Schmitt trigger inputs, with approximately 400 mV of hysteresis. The Schmitt inputs receive the two quadrature signals from the optical shaft encoders at the knob, and remove digital bounce that can result from slowly rotating the knob. The state machine inside U24 uses these signals to determine direction and amount of rotation.

A feature was incorporated to allow the operator to quickly spin the knob and allow the 5700A to properly track it in spite of the inherent delay servicing the interrupt. Every time the operator moves the knob through a 180° rotation of a single detent, U24 generates ENCODERINTR which is sent to U5. IC U5 then generates FPINTR*, interrupting the 68HC000 microprocessor. The microprocessor services the encoder interrupt by reading U24. On a read, indicated by a logic low on ENCODERCS*, U24 places the contents of a seven-bit up/down counter on the data bus. The counter keeps track of the number of 180° rotations that have occurred between the time the interrupt was first initiated and the counter is read. The counter is incremented or decremented depending on the direction of rotation. Signal ENCODERRESET*, generated by U3 on a write to the front panel encoder address space, clears the encoder interrupt.

2-54. LED CIRCUITRY

The LED circuit controls the four light-emitting diodes mounted on the keyboard assembly. It includes a 74LS373 8-bit latch (U10), and four resistors (R16-R19). The respective LEDs light when the following states are active: external sense (EX SNS), external guard (EX GRD), the wideband module is active (WBND), or when an attached 5725A Amplifier is active (BOOST).

Latch (U10) is controlled by the LED_LATCH_EN signal from the decoding PLD U3. Signal LED_LATCH_EN latches the CPU data bus into the internal latches of U10 on a write to the front panel LED memory space. This data appears at the output when control line LEDENABLE* goes low. Control line LED_OUTPUT_CNTRL from U3 is inverted by U11C to create LEDENABLE*. Table 2-7 shows which line activates each LED.

Table 2-7. Control Lines for the Keyboard LEDs

KEYBOARD LED	CONTROL LINES
EX SNS	LED1A
EX GRD	LED2A
W BND	LED2B
BOOST	LED1B

2-55. Keyboard Assembly (A1)

The Keyboard assembly provides the operator with front panel control of the 5700A Calibrator. It connects to the Front Panel assembly (A2) through a cable, and includes an elastomeric keypad, four LEDs, and a rotary encoder (output adjustment) knob.

The elastomeric keypad and the printed circuit board form a 45-switch keyboard arranged in eight columns and six rows. The keyboard scanner circuit on the Front Panel assembly sequentially drives columns one through eight. When a key is pressed, a low appears on the corresponding row as the key's column is scanned. The keyboard scanner circuit encodes the key's row and column location, then takes appropriate action.

The four LEDs (CR1-CR4) are controlled by the LED driver circuit on the Front Panel assembly. LED CR1 is turned on by LED1A when external sensing is selected. LED CR2 is turned on by LED2A when external guard is selected. LED CR3 is turned on by LED2B when the wideband module is active. LED CR4 is turned on by LED1B when an attached 5725A Amplifier is active.

The rotary output adjustment knob activates UUT "Error Mode", allowing the operator to adjust the 5700A output. It can also control the phase shift for variable phase output. The knob assembly consists of two optocouplers (DT1 and DT2) and a magnetically-detented rotary knob. As the knob is turned, optocoupler DT1 generates a pulse signal on ENCODERA and optocoupler DT2 generates a pulse signal on ENCODERB. These signals are routed to the Front Panel assembly where knob encoder circuitry interprets these signals and takes appropriate action. The current-limiting resistor for LEDs within DT1 and DT2 is located on the Front Panel assembly.

2-56. ANALOG SECTION DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of each assembly in the analog section are provided here. Simplified schematics are provided to supplement the text.

2-57. Filter/PA Supply (A18), Low-Voltage Filter/Regulator Section

The Filter assembly receives various ac inputs from the main power transformer and provides unregulated dc to the Regulator/Guard Crossing assembly (A17), and regulated dc supplies +5FR1, -18FR1, and -5FR2 to the DAC assembly. The unregulated supplies are listed in Table 2-8 and the regulated supplies are listed in Table 2-9.

Table 2-8. Unregulated Supplies from the Filter Assembly

SIGNAL NAME	NOMINAL OUTPUT	TOLERANCE	MAX. P-P RIPPLE	RATED OUTPUT	TEST POINT
+15 OSCR	27V	±8V	2V	200 mA	TP2
-15 OSCR	27V	±8V	2V	200 mA	TP5
OSC COM	RETURN				TP4
+5 LHR	12V	±4V	3V	3.5A	TP1
-5 LHR	12V	±4V	2V	400 mA	TP6
LH COM	RETURN				TP3
+44 SR	60V	±15V	3V	155 mA	TP7
-44 SR	60V	±15V	3V	460 mA	TP9
44 S COM	RETURN		SEE NOTE BELOW		TP22
+17 SR	27V	±8V	3V	1.3A	TP10
-17 SR	27V	±8V	3V	1.3A	TP14
17 S COM	RETURN				TP12
+5 FR1R	12V	±4V	2V	400 mA	TP17
-18 FR1R	27V	±8V	2V	50 mA	TP20
FR1 COM	RETURN				TP19
+30 FR1R	50V	±15V	3V	85 mA	TP15
FR1R COM	RETURN				TP16
+30 FR2R		±15V	3V	85 mA	TP8
FR2 COM	RETURN				TP11

NOTE: 44 S COM and 17 S COM are tied together on the Regulator/Guard Crossing assembly (A17).

Table 2-9. Regulated Supplies from the Filter/PA Supply

Signal Name	Nominal Output	Tolerance	Current Limit	Rated Output	Test Point
-5 FR2	-5V	±0.3V	0.15A	0.03A	TP13
FR2 COM	RETURN				TP11
+5 FR1	+5V	±0.3V	2A	0.1A	TP18
-18 FR1	-18V	±0.9V	2A	0.05A	TP21
FR1 COM	RETURN				TP19

2-58. UNREGULATED OSC SUPPLIES

Line OSC COM is the return path for the +15 OSCR and -15 OSCR supplies. These supplies use a full-wave center-tapped configuration. They consist of bridge rectifier CR3 and two filter capacitors, C4 and C6, for +15 OSCR and -15 OSCR, respectively. Inputs are fused with 1.6A slow-blow fuses F1 and F2.

2-59. UNREGULATED LH SUPPLIES

Line 5 LH COM is the return path for the +5 LHR and -5 LHR supplies. These supplies use a full-wave center-tapped configuration, and consist of four diodes (CR1, CR2, CR4, CR5) configured as a bridge rectifier.

Capacitors C2 and C3 filter +5 LHR, and C5 filters -5 LHR. Capacitor C1 reduces the level of generated transients.

2-60. UNREGULATED S SUPPLIES

The ±44 SR supplies use full-wave center-tapped rectifiers. Bridge rectifier CR6 is followed by two filter capacitors C7 and C8 for the +44 SR and -44 SR supplies, respectively. Inputs are fused by 0.5A slow blow fuses, F3 and F5. The ±17 SR supplies also are full-wave center-tapped, consisting of four diodes (CR8, CR10, CR12, CR13) configured as a bridge rectifier. Capacitors C13 and C14 filter the +17 SR supply, while C15 and C16 filter the -17 SR supply.

2-61. TRIAC CIRCUIT

The triac circuit protects the 5700A if it is inadvertently plugged into an excessively high line voltage. For example, it protects the 5700A if it is plugged into a 230V line when the rear panel line voltage select switches are set for 115V operation.

This circuit contains triac CR19, zener diodes VR20, VR21, resistor R1, and capacitor C23. The zener diodes set a trip voltage of 82V. If the ac voltage across the main transformer secondary for the ±17V supply exceeds 82V, the triac fires, shorting out the winding, which causes the main transformer primary fuse to blow.

2-62. FR1 SUPPLIES

Line FR1 COM is the return path for the unregulated +5 FR1R raw supply and the regulated +5 FR1, and -18 FR1 supplies. Each supply uses a full-wave bridge configuration.

The unregulated +5 FR1R supply consists of bridge rectifier CR15 and filter capacitor C19. The input is fused with 1.6A slow-blow fuse F8. The regulated +5 FR1 supply uses the unregulated +5 FR1R supply and contains regulator U2, filter capacitor C20, and protection diode CR16.

The -18 FR1 supply consists of bridge rectifier CR17 and filter capacitor C21. Its input is fused with 0.5A slow-blow fuse F9. The regulated -18 FR1 supply uses the unregulated -18 FR1 supply and contains regulator U3, filter capacitor C22, and protection diode CR18.

2-63. UNREGULATED FR1 SUPPLY

FR1R COM is the return path for the unregulated +30 FR1 supply. This supply uses full-wave bridge rectifier CR14 and filter capacitor C18. Its input is fused with 0.5A slow-blow fuse F7.

2-64. FR2 SUPPLIES

FR2 COM is the return path for unregulated +30 FR2R supply and regulated -5 FR2 supply. Each supply uses a full-wave, bridge configuration. The unregulated +30 FR2R supply consists of bridge rectifier CR7 and filter capacitor C9. Its input is fused with 0.5A slow-blow fuse F4. The -5 FR2 supply consists of bridge rectifier CR11, filter capacitor C11, regulator U1, bypass capacitor C12, and protection diode CR9. The input is fused with 315 mA slow-blow fuse F6.

2-65. Filter/PA Supply (A18), Power Amplifier Output Supply Section

The power amplifier output power supply section of the Filter/PA Supply assembly (A18) receives ac voltage from the main power transformer to generate power supplies +PA and -PA for the output stage of the Power Amplifier assembly (A16). These two power supplies can be switched between the following three modes of operation, depending on the needs of the Power Amplifier.

- o +PA and -PA to ±185V respectively.
- o +PA and -PA to ±365V respectively.
- o +PA and -PA are both turned off.

Figure 2-6 is a simplified schematic for the Power Amplifier Supply section of this assembly.

2-66. ±PA SUPPLIES DIGITAL CONTROL

Circuitry to control the three modes of operation of the +PA and -PA supplies is located on the Power Amplifier Digital Control SIP assembly (A16A1). This SIP assembly is mounted on the main Power Amplifier assembly (A16). Not on the assembly is the quad comparator U201.

The main Power Amplifier assembly generates four control lines:

- o +HI/LO V
- o LO/HI I
- o +ON/OFF
- o H/LV S

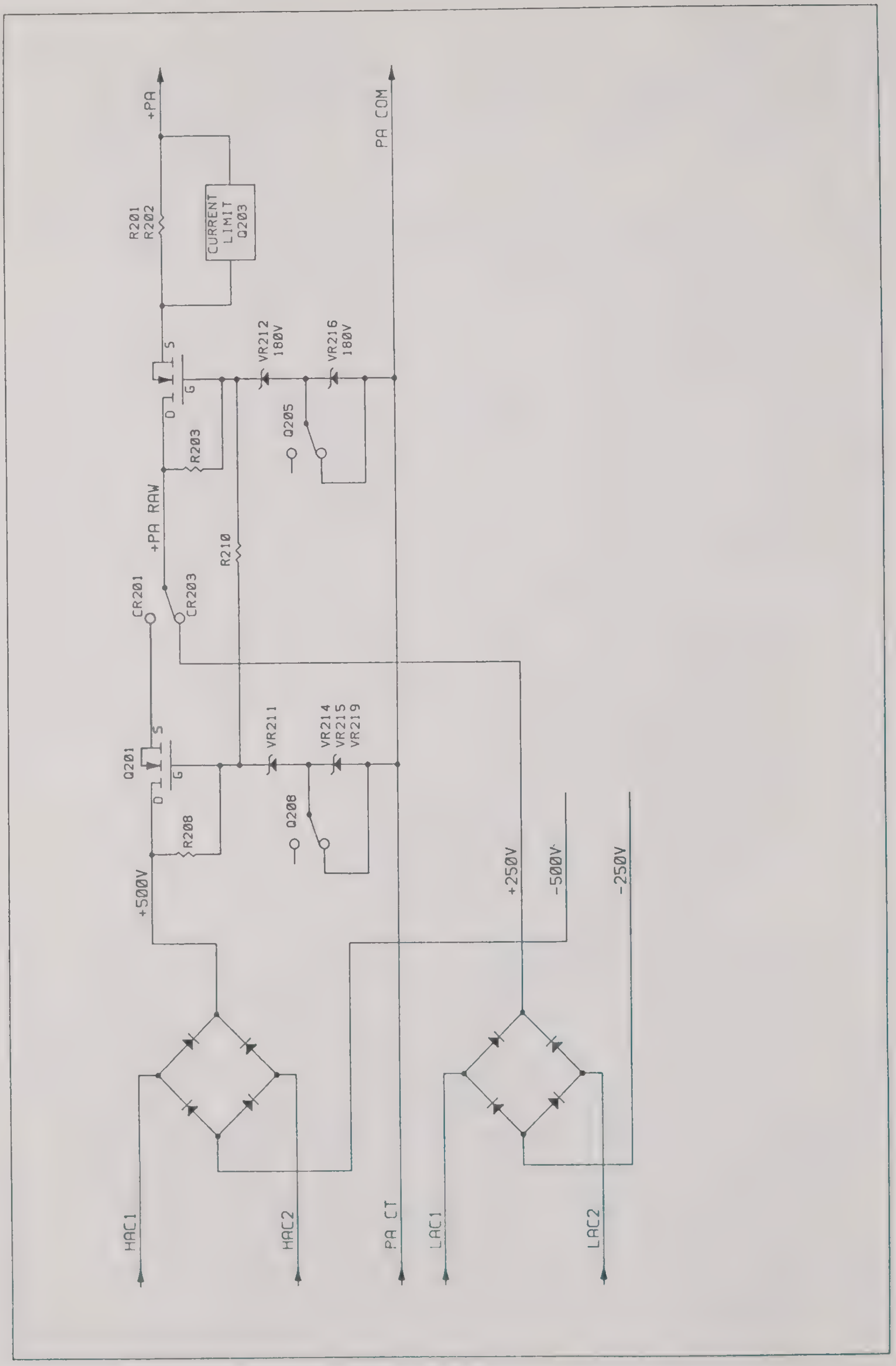

+PA
PA COM
R201
R202
CURRENT LIMIT Q203
S
G
D
VR212 180V
VR216 180V
Q205
R203
+PA RAW
R210
CR201
CR203
Q201
S
G
D
VR211
VR214
VR215
VR219
Q208
R208
+500V
+250V
-500V
-250V
HAC1
HAC2
PA CT
LAC1
LAC2

Figure 2-6. Power Amplifier Supply Simplified Schematic

Component Z201 pulls these signals up. At calibrator power up, the ±PA supply is off. The Power Amplifier Digital Control SIP (A16A1) selectively pulls these control lines low to achieve the two modes of operation. Pulling control lines +HI/LO V and +ON/OFF low sets the +PA supply to +365V. Releasing +HI/LO V changes the +PA supply to 185V.

The comparator (U201) provides level shifting to control the PMOSFETS in the -PA circuit in a similar way. Signal -ON/OFF is generated from +ON/OFF, and -HI/LO V from -H/LV. Control line +LO/HI I switches transistor Q217 which controls relay K201. Relay K201 selects the current limit for both +PA and -PA supplies.

2-67. ±250V AND ±500V SUPPLIES

Input signals PA CT, PA HAC1, PA HAC2, PA LAC1, and PA LAC2 come from the main transformer.

- PA CT is the center tap.
- PA HAC1 and PA HAC2 are high voltage taps with approximately 400V rms and are fused by F201 and F204 respectively.
- PA LAC1 and PA LAC2 are lower voltage taps with approximately 200V rms and are fused by F202 and F203 respectively.
- PA LAC1 and PA LAC2 and bridge rectifier CR222 generate the unregulated ±250V supplies.
- PA HAC1 and PA HAC2 and diodes CR217, CR218, CR220, CR221, CR223, CR224, CR227, and CR228 are in a bridge rectifier configuration to generate the unregulated ±500V supplies.

When the PA supply outputs ±185V, current is drawn only from the lower voltage taps LAC1 and LAC2.

2-68. +PA AND -PA SUPPLIES

Unregulated voltage for +PA is selected between the +250V and +500V unregulated supplies by control line +HI/LO V and diodes CR201, CR203, CR208, and CR210.

Transistor Q204 is a current source that biases VR212 and VR216.

Supply +PA is +185V when the +HI/LO V signal is above 3V. (Transistors Q205 and Q208 are turned on.) Transistor Q205 shorts VR216, while Q208 places a short across VR214, VR215, and VR219. A voltage of +185V appears at the gate of Q202 because of VR212. Approximately 140V appears at the gate of Q201. This 140V and about 250V at the anode of CR208 reverse biases CR201 and CR210, thereby shutting off Q201. Current flows out of the 250V unregulated supply through CR203 and Q202. Regulated supply voltage +PA is determined by the gate voltage of Q202, which is about 190V when +HI/LO V is above 3V.

When +HI/LO V is close to 0V, both Q208 and Q205 are turned off, and over 400V appears at the gate of Q201. CR203 and CR208 are reverse biased, and the supply current flows from the +500V unregulated supply through Q201, CR201, and Q202. The gate voltage of Q202 is approximately 370V, nearly the same as +PA.

The -PA side works exactly like the +PA side except -PA is switched between -185V and -365V by control line -HI/LO V.

The ±PA supplies can be replaced by the ±44SR unregulated supplies by moving switch S201 switched towards the top edge of the board. This feature provides the means to troubleshoot the Power Amplifier using reduced voltages.

NOTE

> Make sure S201 is returned to the ±PA position before resuming normal operation.

2-69. ±PA SUPPLY CURRENT LIMIT

The current limit for both the +PA and -PA supplies is set to either about 90 mA (K201 de-energized) or 150 mA (K201 energized) by K201. Control line +LO/HI I controls relay K201. The high-current mode (150 mA) is used during operation in the 1100V dc range and the 2.2A range.

Output current on the +PA side is sensed between the emitter and base of Q203 by R202 and/or R201. Supply +PA shuts off to near 0V when enough current is flowing through +PA to forward-bias Q203. Then, current though Q203 charges capacitor C209 through R214 to a voltage above the threshold voltage at the inverting input of comparator U201C. The overcurrent condition must persist for about 75 ms for C209 to charge above the threshold. The output of U201 goes high, turning on Q207. This forces the zener diode bias current to flow through Q207 instead of VR212 or VR216, leaving only a few volts at the gate of Q202, thus shutting +PA off. The output of U201C also saturates Q218 and reduces the comparator threshold voltage to near 0V. This provides the comparator with hysteresis; C209 has to discharge close to 0V before +PA can turn on again. The +PA supply cycles on and off as long as the overcurrent condition exists.

Transistor Q206 provides another current limit. While otherwise similar to the Q203 limit, the Q206 current limit turns on at 0.5A and turns off immediately without any delay. The Q206 limit thereby protects the supply under short circuit conditions.

Current limiting on the -PA side works similarly to the +PA side with one difference. That is that shutoff of -PA can happen under two circumstances:

- -PA is loaded beyond its current limit.
- +PA is shut off. (Shut off of -PA is slaved to shut off of +PA.)

2-70. Regulator/Guard Crossing Assembly (A17)

The Regulator/Guard Crossing assembly (A17) provides two separate functions: voltage regulation for the analog power supplies, and digital control of the guard crossing. The voltage regulation portion is described first followed by the digital control portion. Refer to the schematic diagrams for the Regulator/Guard Crossing Assembly for this discussion.

2-71. VOLTAGE REGULATOR CIRCUITRY

The regulator circuit receives unregulated dc from the regulator filter circuit on the Filter/PA Supply assembly (A18) and provides 13 regulated dc outputs and 1 unregulated dc output for the various analog assemblies. Table 2-10 lists the regulated supplies from the Regulator/Guard Crossing Assembly.

Table 2-10. Regulated Outputs from the Regulator/Guard Crossing Assembly

SIGNAL NAME	NOMINAL OUTPUT	TOLERANCE	CURRENT LIMIT	RATED OUTPUT	TEST POINT
+15 OSC	+15V	±800 mV	2A	200 mA	TP3
-15 OSC	-15V	±800 mV	2A	200 mA	TP5
+5RLH	+5.975V	±425 mV	2A	600 mA	TP14
+5LH	+5.1V	±300 mV	2A	600 mA	TP11
-5LH	-5V	±300 mV	2A	400 mA	TP15
+44S	+44.15V	±2.03V	0.5A	140 mA	TP13
-44S	-44.15V	±2.03V	0.5A	140 mA	TP16
+17S	+17.475V	±475 mV	4A	1.0A	TP8
-17S	-17.865V	±835 mV	6A	1.0A	TP12
+15S	+15V	±800 mV	2A	300 mA	TP18
-15S	-15V	±800 mV	2A	300 mA	TP19
+30FR1	+30.96V	±1.7V	1A	85 mA	TP2
+30FR2	+30.96V	±1.7V	1A	85 mA	TP7

2-72. REGULATED OSC SUPPLIES

The +15 OSC and -15 OSC supplies are used exclusively by the Oscillator Output (A12) and Oscillator Control (A13) assemblies. OSC COM is the return path for these supplies. The +15 OSC uses the unregulated +15 OSCR from the Filter assembly and consists of three-terminal TO-220 regulator U2 with heat sink, bypass capacitors C1 and C2, and protection diodes CR2 and CR3. The -15 OSC uses the unregulated -15 OSCR from the Filter assembly and consists of three-terminal TO-220 regulator U3 with heat sink, bypass capacitors C4 and C5, and protection diodes CR5 and CR7. Capacitors C2 and C5 improve the stability of U2 and U3 respectively. Diodes CR3 and CR5 protect U2 and U3 from reverse voltages. Diodes CR2 and CR7 protect U2 and U3 from input shorts.

2-73. REGULATED LH SUPPLIES

LH COM is the return path for the +5RLH, +5LH, -5LH and +8RLH supplies. The +5RLH, +8RLH, and +5LH supplies use the unregulated +5LHR supply from the Filter assembly. The +5RLH supply uses three-terminal TO-3 regulator U11 with heat sink, bypass capacitors C20 and C21, protection diodes CR17 and CR20, and the diode combination of CR34 and CR35. The +5LH supply uses three-terminal TO-3 regulator U8 with heat sink, bypass capacitor C16, protection diodes CR14 and CR16, and resistor R13. The -5LH supply uses the unregulated -5LHR from the Filter assembly and consists of three-terminal TO-220 regulator U12 with heat sink, bypass capacitors C23 and C24, and protection diodes CR21 and CR24. Capacitors C16, C21, and C24 improve the stability of U8, U11, and U12 respectively. Diodes CR14, CR17, and CR24 protect the regulators from input shorts. Diodes CR16, CR20, and CR21 protect the regulators from reverse voltage. Resistor R13 and diodes CR34 and CR35 increase the output of regulators U8 and U11. The unregulated +8RLH supply is generated by fusing the unregulated +5LHR supply from the Filter assembly with 3.15A slow-blow fuse F1.

2-74. REGULATED S SUPPLIES

Line S COM is the return path for the +44S, -44S, +17S, -17S, +15S and -15S supplies. Line S COM is also connected to LH COM. The +44S supply uses the unregulated +44SR from the Filter assembly. This supply uses three-terminal TO-39 regulator U10, Q2, VR3, VR4, VR5, R20, R14, R15, CR18, CR19, CR25, C17, C18, C19, C65, PTC resistor R60. The regulator IC (U10) provides the current and thermal limiting. Its regulated output voltage is set by R14 and R15, yielding a nominal output of +44.15V. Components Q2, R20, VR3 and VR4 act as an emitter follower to protect the regulator against a potentially excessive input-output voltage differential in the event of a short circuit. Capacitor C65 filters this voltage to the regulator. Diodes CR19 and CR25 protect the regulator against shorts at the input, while CR18 protects the regulated output from reverse voltage. Capacitors C17 and C18 are for bypass. Capacitor C19 improves rejection of input variations. Components U10 and Q2 have heat sinks to provide thermal protection for both normal and short-circuit conditions. The regulator is shunted by R60 and VR5, which normally pass 28 mA of current to remove the power from the regulator.

In an output short condition, the value of the PTC increases, limiting current through the device to less than 17 mA at 25oC.

The -44S supply uses the unregulated -44SR supply from the Filter assembly. This supply uses three-terminal TO-39 regulator U13, Q1, VR1, VR2, VR6, R17, R18, R19, PTC Resistor R61, CR22, CR23, CR32, CR33, C22, C25, C26, and C66. The regulator IC, U13, provides the current and thermal limiting. Its regulated output voltage is set by R17 and R18, yielding a nominal output of -44.15V. Components Q1, R19, VR1, VR2 and CR32 act as an emitter follower and protect the regulator against a potentially excessive input-output voltage differential if a short circuit occurs. Capacitor C66 filters the voltage to the regulator. The regulator is shunted by R61 and VR6, which pass 28 mA. In an output short condition, the value of the PTC increases, limiting current through the device to less than 17 mA at 25°C.

Diode CR32 removes VR2 from the circuit in a shorted condition to meet U13's input-output differential specifications. Diodes CR22 and CR33 protect the regulator against shorts at the output, while CR23 protects the regulated output from reverse voltage. Capacitors C25 and C26 are for bypass. Capacitor C22 improves rejection of any input variations. The heat sink on regulator U13 guarantees thermal protection for both normal and short-circuit operating conditions.

The +17S supply uses the unregulated +17SR supply from the Filter assembly. This supply uses three-terminal TO-3 regulator U6 with heat sink, and R5 and R6. The output voltage is set by resistors R5 and R6 in the same manner as the +44S supply. Capacitors C8 and C9 are for bypass. Capacitor C11 improves ripple rejection. Diodes CR8 and CR26 protect the regulator against shorts at the input, while CR11 protects the regulated output from reverse voltage.

The -17S supply uses the unregulated -17SR supply from the Filter assembly. It uses three-terminal TO-3 regulator U7 and R10 and R11. The output voltage is set by resistors R10 and R11 in the same manner as the -44S supply. Capacitors C13 and C15 are for bypass. Capacitor C14 improves ripple rejection. Diodes CR15 and CR27 protect the regulator against shorts at the input, while CR13 protects the regulated output from reverse voltage.

The +15S supply uses the unregulated +17SR supply from the Filter assembly. It consists of +15V three-terminal TO-220 regulator U4. Capacitor C27 is required for the stability of U4. Diode CR28 protects the regulator against shorts at the input, while CR29 protects the regulated output from reverse voltage.

The -15S supply uses the unregulated -17SR supply from the Filter assembly. It consists of -15V three-terminal TO-220 regulator U9. Capacitor C29 stabilizes U9. Diode CR31 protects the regulator against shorts at the output, while CR30 protects the regulated output from reverse voltage.

2-75. FR1 SUPPLY

FR1 COM is the return path for the +30FR1 supply. This supply uses the unregulated +30FR1R supply from the Filter assembly and consists of three-terminal TO-39 regulator U1 with heat sink, bypass capacitors C3 and C6 and protection diodes CR1, CR4, and CR6. Resistors R1 and R2 set the output voltage in the same manner as the +44S supply. Capacitor C7 improves ripple rejection. Diodes CR1 and CR4 protect U1 against input shorts, while CR6 protects against reverse voltage.

2-76. FR2 SUPPLY

FR2 COM is the return path for the +30FR2 supply. This supply uses the unregulated +30FR2R supply from the filter assembly and consists of three-terminal TO-39 regulator U5 with heat sink, bypass capacitors C10 and C28, and protection diodes CR9, CR10, and CR12. Resistors R4 and R8 set the output voltage in the same manner as the +44S supply. Capacitor C12 improves ripple rejection. Diodes CR9 and CR10 protect U5 against input shorts, while CR12 protects against reverse voltage.

2-77. GUARDED DIGITAL CONTROL CIRCUITRY

The Inguard CPU controls all the analog assemblies. It communicates with the Unguarded CPU assembly (A20) through a serial fiber-optic link. The Inguard CPU is a Hitachi 637A01Y0 CMOS microcontroller (U56) with 16K x 8 bit (16 KB, or 16 kilobyte) internal CMOS EPROM. Support circuitry includes 8K x 8 bits (8 KB) of external CMOS static RAM, watchdog timer circuitry, reset and power glitch detect circuitry, test switches, a serial fiber-optic link to the unguarded CPU, and decoders and buffers to interface to the guarded digital bus. The assembly also generates an 8 MHz sine wave for use by some of the analog assemblies.

2-78. Inguard CPU Memory Map

Table 2-11 shows the memory map of the Inguard processor.

2-79. Inguard Memory Configuration

The microcontroller (U56) has 16 KB (kilobytes) of internal EPROM program memory. IC U62 provides 8 KB of external static CMOS RAM, with a jumper option for a plug-in replacement with a 2 KB device.

2-80. Inguard Clock Circuit

This circuit uses 8 MHz crystal Y52 and step-down transformer T51 to generate a low-level (200 mV p-p) 8 MHz clock used by other guarded assemblies throughout the calibrator. Transformer (T51) has a center-tapped secondary, and provides CLK COM, CLK and CLK*. The CLK and CLK* sine-wave signals are sent to certain analog assemblies where they are converted into square wave clock signals for timing purposes.

Table 2-11. Inguard CPU Memory Map

ADDRESS SPACE (HEX)	NAME	USE
0000 - 0027		Internal Registers on the 6301
0028 - 003F		Unused memory space
0040 - 013F		Internal RAM 256 Bytes
0140 - 3FFF		Unused memory space
4000 - 4007	CS0*	Wideband Output (A5)
4008 - 400F	CS1*	Current/Hi-Res (A7)
4010 - 4017	CS2*	Switch Matrix (A8)
4018 - 401F	CS3*	Ohms Cal (A9)
4020 - 4027	CS4*	Unused
4028 - 402F	CS5*	DAC (A11)
4030 - 4037	CS6*	DAC (A11)
4038 - 403F	CS7*	Current/Hi-Res (A7)
4040 - 4047	CS8*	Oscillator Control (A12)
4048 - 404F	CS9*	Oscillator Output (A13)
4050 - 4057	CS10*	High Voltage Control (A14)
4058 - 405F	CS11*	Power Amplifier (A16)
4060 - 4067	CS12*	Rear Panel (A21) Boost
4068 - 406F	CS13*	Current/Hi-Res (A7)
4070 - 4077	CS14*	Wideband Oscillator (A6)
4078 - 407F	CS15*	Unused
4080 - 5FFF		Unused(memory overlay of 4000-407F)
6000 - 9FFF		Unused
A000 - BFFF		External RAM
C000 - FFFF		Internal ROM or EPROM

2-81. Inguard Watchdog Timer

The watchdog timer circuit uses a 74HC4020 (U59) and part of Programmable Logic Device (PLD) U58. The microcontroller (U56) generates a 19.2 kHz square wave (SCLK) on pin 11. The frequency of this clock is the same as the baud rate of the serial interface. Once the clock frequency is initialized, it runs without software supervision. This clock drives U59, which divides by 16384 to obtain a logic low interval of 427 ms followed by a logic high interval of 427 ms. The output of the U59, POPIN, goes to the PLD, which asserts POP to the analog hardware and NMIPOP* to the processor if U59 is not reset every 427 ms. The PLD also asserts POP on power-up and on any hardware reset. In order to prevent POP and NMIPOP*, the watchdog counter must be reset by reading or writing any analog hardware, or by toggling the POPCLRL line. The POPCLRL line is also used to disable the watchdog by going low.

2-82. Power-Up and Reset Circuitry

This circuit consists of U60, SW51, C55, C56, R52, and Z51. The line monitor chip (U60) detects three events: the power supply falling below 4.5V, reset being initiated by closure of momentary contact switch SW51, or BREAK being asserted from the break detection circuitry. If any of these conditions occurs, U60 resets the board for 130 ms. Pin 5 of U60 is an open-collector output, pulled high by pin 12 of Z51.

2-83. Break Detection

The break-detect circuit acts as a serial communications break detector enabling the CPU assembly (A20) to reset U56 and U58 via the power-up and reset circuitry. This break-detect circuit uses a 74HC4020 binary counter (U63) and an inverter U51C. The microcontroller (U56) outputs the 1.2288 MHz ECLK clock on pin 64. This signal clocks U63, which in turn divides the signal by 16,384 to produce successive logic low and high intervals (each of 6.67 ms) at the BREAK output (U63, pin 3). Under normal conditions the RCV (receive) line is high to hold U63 clear. The main 68HC000 CPU can force a reset of the Guard Crossing over the fiber-optic link by holding RCV low for more than 6.67 ms, which causes BREAK to go high. BREAK, inverted by U51C, is used by the reset circuitry to force a Guard Crossing reset via RESET*.

2-84. Fiber-Optic Link to CPU

Guarded digital and analog circuits are isolated from the unguarded CPU assembly (A20) by a fiber-optic link that asynchronously transmits serial data. On the transmit side, the microcontroller transmit output (XMT) controls a 75451 (U57) which drives fiber-optic transmitter J72 mounted on the Analog Motherboard. Receive signal RCV comes from fiber-optic receiver J71 also mounted on the Analog Motherboard. The receiver converts the light signal to TTL levels that become the RCV signal at the microcontroller. A fiber-optic cable links the fiber-optic transmitter on the Analog Motherboard to the fiber-optic receiver on the Digital Motherboard. Another fiber-optic cable links the other receiver/transmitter pair on the motherboards.

2-85. Interface to Guarded Digital Bus

The interface to the guarded digital bus consists of a 74HCT245 (U55), a 74HCT244 (U52), two 74HC137s (U53 and U54), inverters U51B and U51D, resistor packs Z52, Z53, and Z54, and the POP line from U58. U52A and U52B buffer various control and address lines. Resistors from Z52 pull the lines of U52A to desired inactive states when BUSEN* is at a logic high, disabling the bus. U55 is a bi-directional data bus buffer (D0-D7). Resistor packs Z53 and Z54 match the lines of the buffered data bus, reducing reflected noise. ICs U53, U54, and U51D perform a 4-to-16 decode of address lines A3-A6, generating 16 chip-select lines (CS0*-CS15*) on the guarded digital bus. These 16 signals select the various assemblies on the Analog Motherboard. U51B buffers and inverts the INT interrupt signal from the DAC assembly. The POP signal from U58 is a reset line sent to the analog assemblies.

2-86. Inguard CPU Interrupts

The Inguard CPU microprocessor handles many different interrupts. These are listed in Table 2-12 in order of priority with the highest priority interrupts first.

Table 2-12. Inguard CPU Interrupts

VECTOR MSB	VECTOR LSB	INTERRUPT	DESCRIPTION
FFFE	FFFF	*RES	Power Up Reset
FFEE	FFEF	TRAP	Address error or op code error
FFFC	FFFD	!NMI	Non maskable interrupt (NMIPOPL)
FFFA	FFFB	SWI	UNUSED
FFF8	FFF9	!IRQ1	!IRQ1,ISF (A/DINTL)
FFF6	FFF7	ICI	Timer 1 input capture (unused)
FFF4	FFF5	OCI	Timer 1 output compare 1,2 (unused)
FFF2	FFF3	TOI	Timer 1 overflow (unused)
FFEC	FFED	CMI	Timer 2 counter match
FFEA	FFEB	!IRQ2	UNUSED
FFF0	FFF1	SIO	RDRF + ORFE + TDRE + PER

RDRF - Receive Data Register Full
ORFE - Overrun Framing Error
TDRE - Transmit Data Register Empty
PER - Parity Error

2-87. Switch Matrix Assembly (A8)

The Switch Matrix Assembly does the following tasks:

- Coordinates the flow of signals from each analog assembly (excepting the Wideband AC Module (Option -03)) to the calibrator's binding posts. This communication determines the calibrator's range.
- Coordinates the connection of various analog and digital common lines during operate, standby, and calibration modes.
- Controls such binding post functions as operate/standby, internal/external sense, and internal/external guard.
- Provides an internal cal zero amplifier used in the calibration of offsets for all dcv ranges (except the 1100V range).

The Switch Matrix Assembly consists of 33 latching type, two- and four-pole relays. The relays are driven by special driver chips, which are controlled by the assembly's 24-output 82C55 chip. The Switch Matrix also contains the 5700A-4HR1 Temperature-Controlled Precision DC Amplifier Hybrid and RNET assembly, which is used when the calibrator is in the dc 2.2V or 220 mV range. The resistor network also is used to create resistive dividers to generate the ac or dc 220 mV, ac 22 mV, and ac 2 mV ranges. Additional analog circuitry in the Switch Matrix Assembly includes the dc 2.2V range output stage, the internal cal zero amplifier, FETs to support assembly calibration, assembly diagnostics, and circuitry to control some of the motherboard relays.

2-88. SWITCH MATRIX DIGITAL CONTROL

Refer to sheet four of the 5700A-1020 schematic diagram during the following discussion. The heart of the Switch Matrix digital control circuitry is an 82C55 Programmable Peripheral Interface IC (U1) under software control via the guarded digital bus. This IC has three ports that generate 24 outputs. These outputs are used to control eight UCN5801 Latching Driver ICs (U5-U12) controlling all Switch Matrix latching relays, one UCN5801 Latching Driver (U13) controlling the 10 non-latching relays on the Motherboard, a 4028 decoder (U2), five FET switches (Q6-Q7, Q9-Q11), and an analog multiplexer (U4) for self diagnostics.

Eight UCN5801 latching driver ICs (U5-U12) drive Switch Matrix latching relays. Port A (PA0-PA7) from U1 provides a common input bus. Each driver chip has a separate strobe line. A 4028 decoder (U2) generates strobe lines U5STB-U13STB for strobing U5-U13 respectively. These individual strobe lines are decoded from PB0-PB3 of U1. When a strobe line is selected, the data on the bus is strobed in the respective driver chip. The output enables are controlled directly by PC0-PC3 of U1. One bit of port C enables two drivers. PC0 enables U5 and U6, PC1 enables U7 and U8, PC2 enables U9 and U10, and PC3 enables U11 and U12. By enabling only two driver ICs at a time, excessive power supply current draw is prevented. To insure that the relays are latched properly, the driver chips must be enabled for 10 ms. As an example, the following steps are taken to set up relays in the first bank:

1. Write the proper data for the relays associated with driver U5 (K2, K9, K11, and K15) to port A of the 82C55.
2. Write 0 hex to PB0-PB3 to make U5STB go high. Now write 9 hex to PB0-PB3 to make all strobe lines go low. The data has now been strobed into U5.
3. Write the proper data for the relays associated with U6 (K3, K4, K5, and K24) to port A of the 82C55.
4. Write 1 hex to PB0-PB3 to make U6STB go high. Now write 9 hex to PB0-PB3 to make all strobe lines go low. The data has now been strobed into U6.
5. Write FE hex to port C (PC0 is low), wait 10 ms and write FF hex to port C. This takes the outputs of U5 and U6 out of tri-state and allows the proper relay coils to be energized for 10 ms.

A UCN5801 driver (U13) drives non-latching relays on the Motherboard. The Motherboard non-latching relay supply circuit, as outlined in sections A6 through A8 of the schematic diagram, contains U17, Q1, Q2, CR1, CR2, CR10, and R6-R12. Port A of U1 provides data for this driver (PA0-PA7), and decoder U2 provides the strobe signal. Since this driver controls non-latching relays, the enable is tied to LH COM.

The non-latching relay supply circuit provides approximately 7V to the relays on the Motherboard during pull-in, and approximately 3.5V during normal operation. This voltage is routed to the Motherboard on the RLY+V line. The 7V is needed to insure pull-in while the 3.5V is sufficient to prevent drop out. This cuts relay heating and thermal EMFs. PC5 controls the non-inverting amplifier U17. This amplifier is the control element for Transistor Q1. When PC5 is low, the output is 3.5V, and when PB5 is high, the output is 7V. Components CR1, Q2 and R10-12 form a foldback current limit for the supply. The following steps are taken to select a particular state for Motherboard relays RLY1-RLY10:

1. Write the data corresponding to the desired state to port A (PA0-PA7) of the 82C55 (U1).
2. Strobe the data into U13 by writing 8 hex to PB0-PB3 to make U13STB go high, then a 9 hex to make it go low.
3. Apply 7V to the relay coils by setting PC5 high.
4. Wait approximately 20 ms for the relays to pull in, then reduce the coil voltage to 3.5V by setting PC5 low.

There are five FETs on the Switch Matrix. Q9 and Q10 (sheet 3, C7), which are N-channel JFETs controlled by port B (PB5) of U1, are driven by an LM393 open-collector comparator (U15A) to provide the proper level shifting. DMOS enhancement FETs are used for the remaining three FETs (Q6, Q7, and Q11). Refer to sheet 1, B5 of the schematic diagram. FETs Q6 and Q7 are driven by U1, port B, with a high on PB4 turning on Q6, and a logic high on PB7 turning on Q7. FET Q11 is driven on by a logic high from U1, port C (PC4).

The diagnostic circuit (sheet 4, B7) enables the calibrator to monitor +8RLH, the 2.2V range output voltage, +5RLH, -5LH, +17S, -17S, the assembly temperature (U3), and the OVEN TEMP line from the heated hybrid. OVEN TEMP, +5RLH, -5LH, and +8RLH are divided down by a factor of ten by Z5 and Z6. A 4051 analog multiplexer (U4) is controlled by PA0-PA2 and PC6 from U1. This multiplexer selects which one of these eight voltages is applied to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11).

2-89. SWITCH MATRIX OPERATION: 11V DC AND 22V DC RANGES

Refer to Figure 2-7 for the following discussion. DC 11V and 22V ranges are generated by the DAC assembly and routed directly to the front panel binding posts through relays on the Switch Matrix and Motherboard.

Line DAC HI is connected to INT OUT HI through relays K18B, K27, and K30. INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line DAC SENSE HI is connected to INT SENSE HI through relays K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUTPUT/SENSE HI during internal sensing.

Lines PA COM and DAC LO are connected by relays K11 and K12, and connected to the OUTPUT LO binding post by relay K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or to OUTPUT/SENSE LO during internal sensing.

2-90. SWITCH MATRIX OPERATION: 2.2V AC AND 22V AC RANGES

Refer to Figure 2-8 for the following discussion. AC 2.2V and 22V ranges are generated by the Oscillator assemblies and routed directly to the front panel binding posts through relays located on the Switch Matrix and Motherboard.

Line OSC OUT is connected to INT OUT HI through relays K19A, K18B, K27, and K30. INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line OSC SENSE is connected to INT SENSE HI through relays K19B, K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUTPUT/SENSE HI during internal sensing.

Line OSC COM is connected to the OUTPUT LO binding post through relays K11 and K10 on the Switch Matrix. Switch Matrix relays K13 and K15 connect OSC SENSE LO to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

2-91. SWITCH MATRIX OPERATION: 220V AC AND DC RANGES

Refer to Figure 2-9 for the following discussion. In the dc 220V range, PA OUT HI from the Power Amplifier assembly (A16) is routed to the High Voltage Control assembly (A14), where it goes through relay K10 and becomes PA OUT DC. Line PA OUT DC is routed to the Switch Matrix and connected to INT OUT HI through relays K20, K19A, K18B, K27 and K30. Relay K1 on the Motherboard connects INT OUT HI to the OUTPUT HI binding post.

Line PA SENSE DC is connected to INT SENSE HI through relays K20, K19B, K18A, K25, and K26. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or OUT/SENSE HI during internal sensing. PA COM and DAC LO are connected by relays K11 and K12, and connected to the OUTPUT LO binding post by relay K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

In the ac 220V range, Power Amplifier outputs PA OUT HI and PA SNS AC are routed to the High Voltage Control assembly (A14) where relays K10, K3, and K13 connect them to HV OUT and HV SNS respectively. HV OUT is connected to the OUTPUT HI binding post through relays K9 and K1 on the Motherboard. Motherboard relays K10, K2, and K3 connect HV SNS to the SENSE HI binding post during external sensing, or to OUTPUT/SENSE HI during internal sensing. Connection to the OUTPUT LO and SENSE LO binding posts is done with relays on the Switch Matrix. PA COM is connected to the OUTPUT LO binding post through relays K11 and K10. Switch Matrix Relays K13 and K15 connected OSC SENSE LO to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

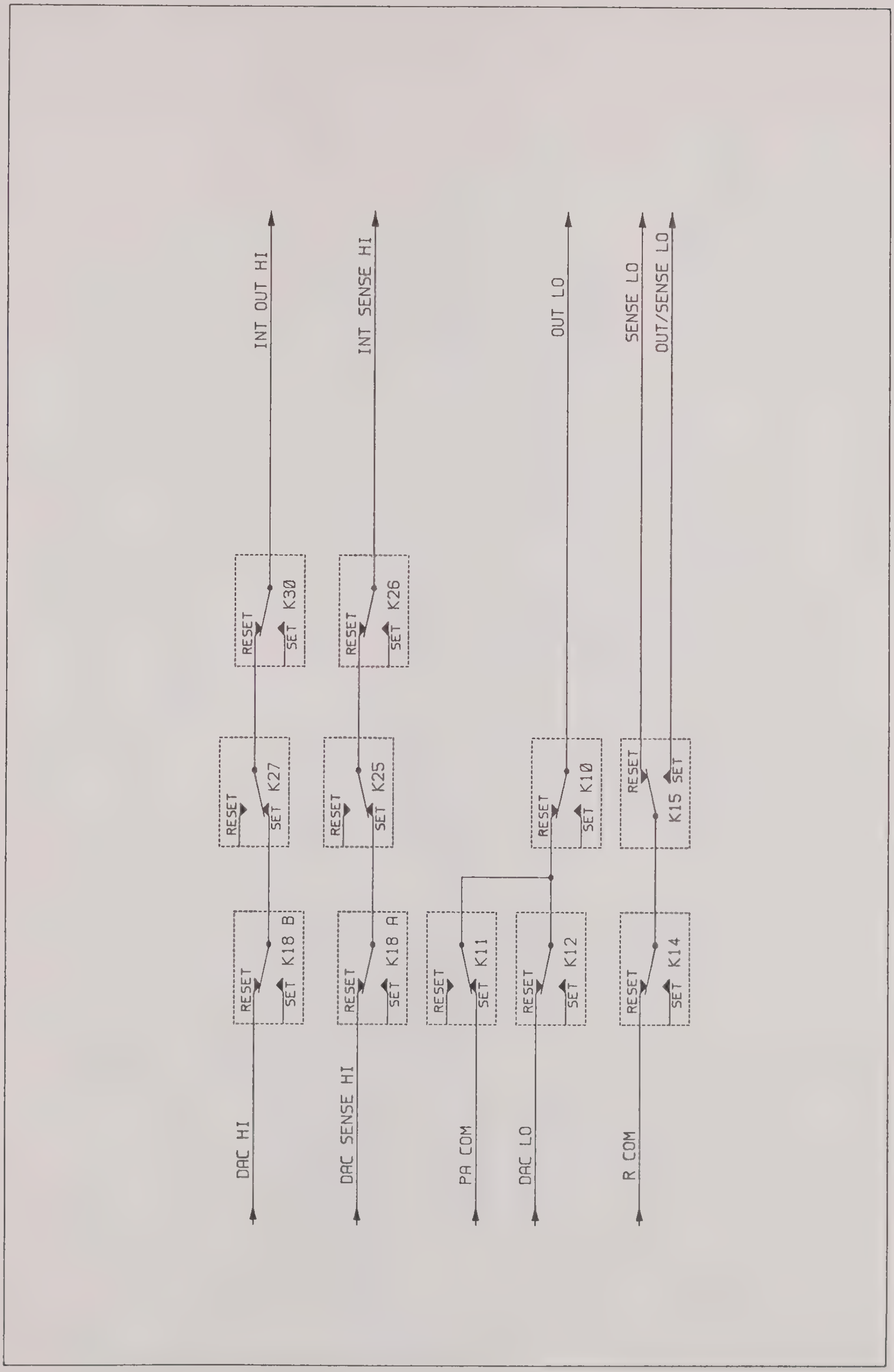

INT OUT HI
INT SENSE HI
OUT LO
SENSE LO
OUT/SENSE LO
RESET
SET
K30
K26
K27
K25
K10
K15
K18 B
K18 A
K11
K12
K14
DAC HI
DAC SENSE HI
PA COM
DAC LO
R COM

Figure 2-7. Switch Matrix Configuration for 11V dc and 22V dc Ranges

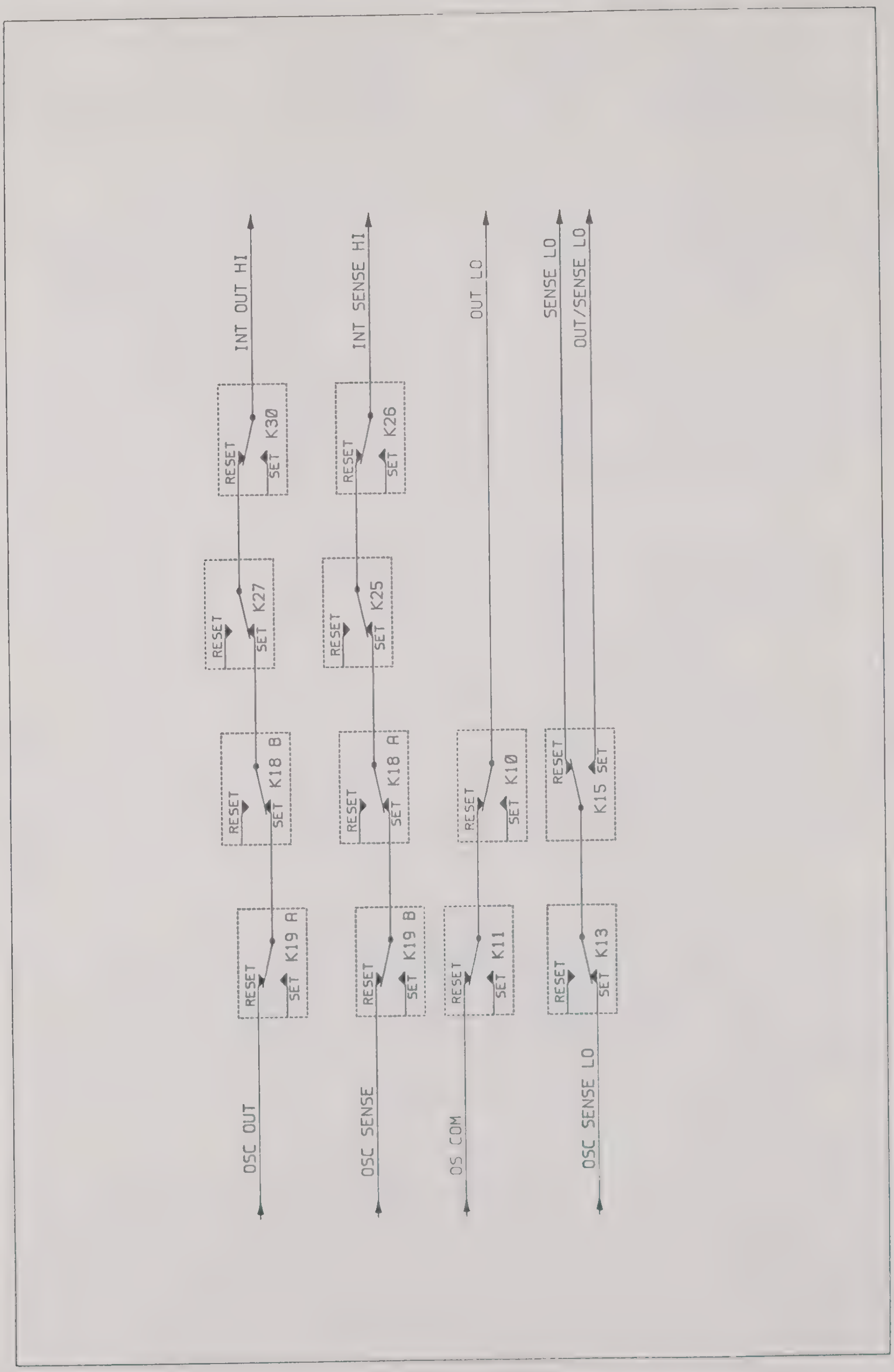

INT OUT HI
INT SENSE HI
OUT LO
SENSE LO
OUT/SENSE LO
RESET
SET
K30
K27
K18 B
K19 A
K26
K25
K18 A
K19 B
K10
K11
K15
K13
OSC OUT
OSC SENSE
OS COM
OSC SENSE LO

Figure 2-8. Switch Matrix Configuration for 2.2V and 22V ac Ranges

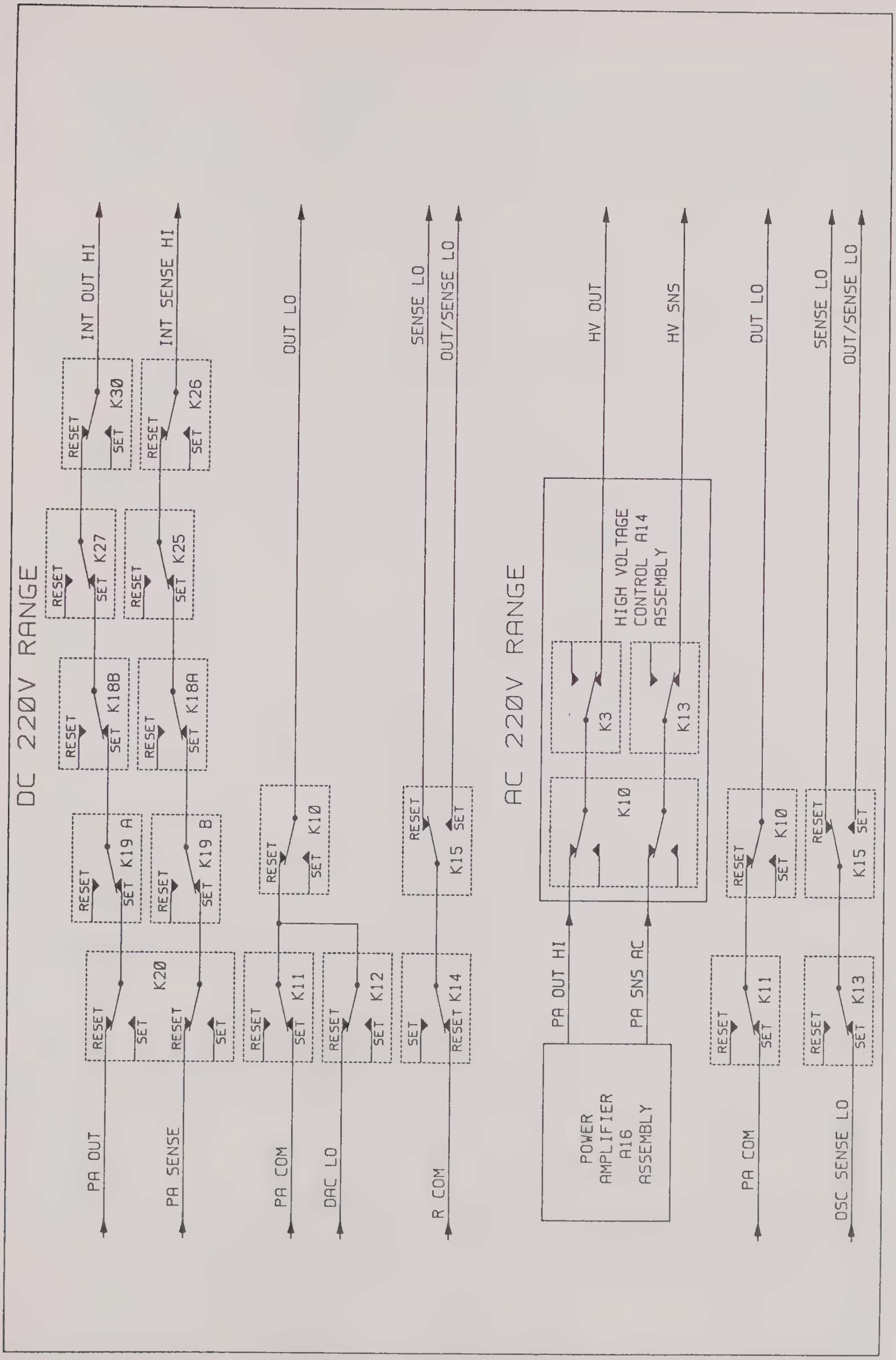

DC 220V RANGE
PA OUT
PA SENSE
PA COM
DAC LO
R COM
K20
RESET
SET
K11
K12
K14
K19 A
K19 B
K18B
K18A
K27
K25
K30
K26
K10
K15
INT OUT HI
INT SENSE HI
OUT LO
SENSE LO
OUT/SENSE LO
AC 220V RANGE
POWER AMPLIFIER A16 ASSEMBLY
PA OUT HI
PA SNS AC
HIGH VOLTAGE CONTROL A14 ASSEMBLY
K10
K3
K13
HV OUT
HV SNS
PA COM
OSC SENSE LO
K11
K13
K10
K15
OUT LO
SENSE LO
OUT/SENSE LO

Figure 2-9. Switch Matrix Configuration for 220V dc and ac Ranges

2-92. SWITCH MATRIX OPERATION: 2.2V DC RANGE

Refer to Figure 2-10 for the following discussion. The dc 2.2V range circuit consists of the dc 2.2V attenuator and a dc 2.2V range amplifier as outlined on page 3 of the Switch Matrix schematic. This circuit contains a CA3096 transistor array IC (U19A-E), transistor Q4, FETs Q12 and Q13, resistors R20 and R25-R32, relays K1 and K2, part of the resistor network 4R07, and a dc amplifier heated hybrid.

The resistor network is bonded to the hybrid and this entire assembly is called the 5700A-4HR1 (HR1) on the schematic. Transistor Q3 drives the heater resistor on the hybrid. The heater control circuit adjusts the base voltage of Q3 to deliver the correct power to the heater resistor to maintain thermal control. Transistor Q8 protects the hybrid in case Q3 fails.

To produce the dc 2.2V range, the DAC assembly (A11) is set to the 11V range. DAC OUT HI and DAC SENSE HI are connected to pin 10 of the resistor network by relay K1, and DAC LO is connected to pin 9 by relay K2. The network divides the voltage by five. The divided voltage from pin 8 is connected to the input (pin 11) of the dc amplifier hybrid.

This temperature-controlled amplifier is used as a buffer amplifier. The output of the buffer amplifier (pin 18) drives the 2.2V range high current output stage consisting of U19, Q4, R25-R32, and CR7-CR9. This circuit enables the 2.2V range to support 50 mA of current with current limiting. FETs Q12 and Q13 provide localized feedback for the precision dc amplifier during unusual conditions, such as a short circuit at the OUTPUT binding posts or when this range is in standby.

Line 2.2V OUT is connected to INT OUT HI through relays K27 and K30 on the Switch Matrix. Line INT OUT HI is connected to the OUTPUT HI binding post through relay K1 on the Motherboard. Line 2.2V SENSE is connected to INT SENSE HI through relays K25 and K26 on the Switch Matrix. Motherboard relays K2 and K3 switch INT SENSE HI to the SENSE HI binding post during external sensing, or to OUTPUT/SENSE HI during internal sensing.

Line PA COM is connected to the OUTPUT LO binding post through relays K11 and K10. Switch Matrix relays K14 and K15 connect R COM to the SENSE LO binding post during external sensing, or OUTPUT/SENSE LO during internal sensing.

2-93. CALIBRATION OF THE 2.2V RANGE

Refer to Figure 2-11 for the following discussion. Calibration of the 2.2V range involves determining its offset and gain constants.

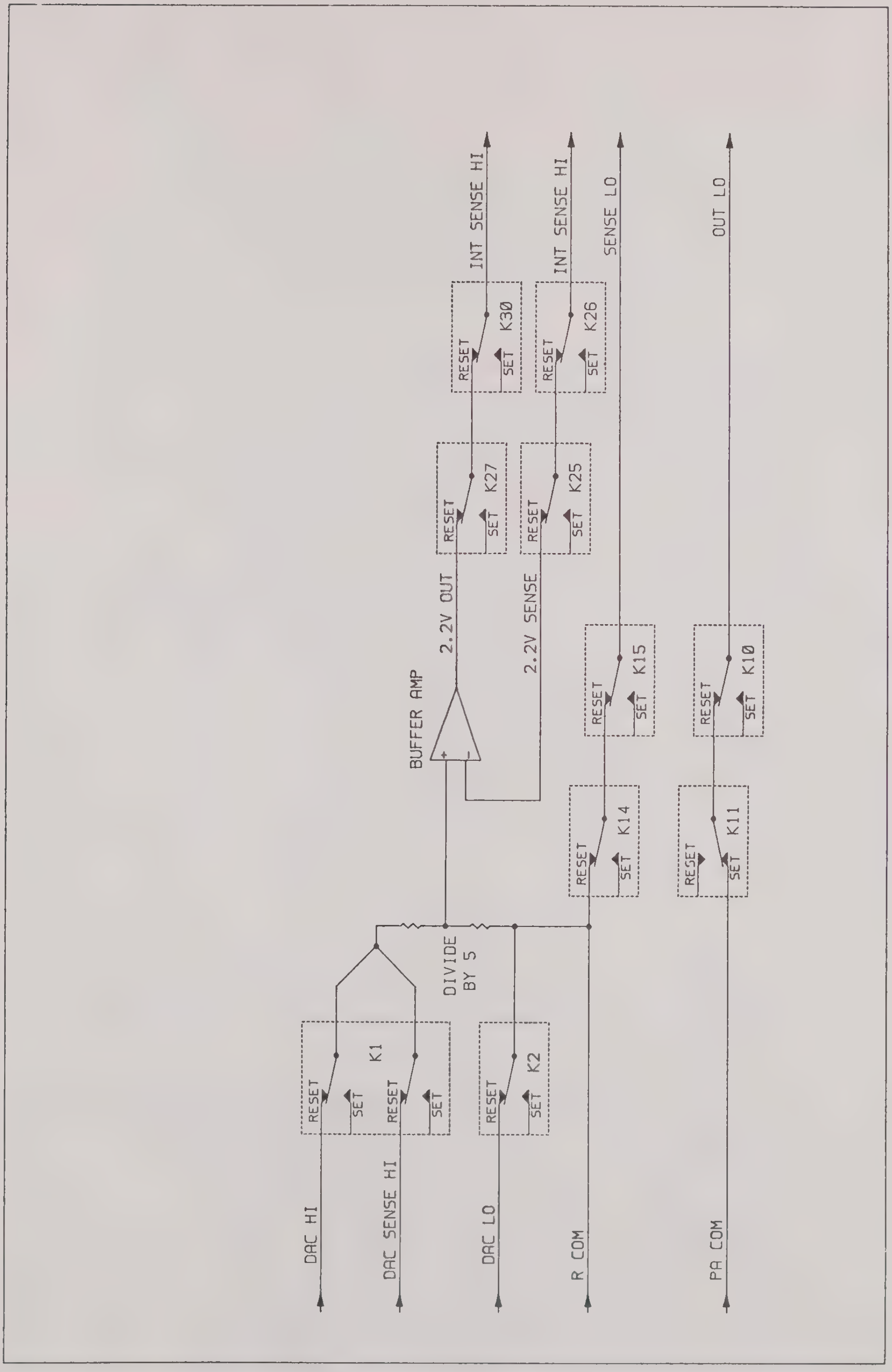

DAC HI
DAC SENSE HI
DAC LO
R COM
PA COM
RESET
SET
K1
K2
DIVIDE BY 5
BUFFER AMP
+
-
2.2V OUT
2.2V SENSE
K14
K11
K15
K10
K27
K25
K30
K26
INT SENSE HI
INT SENSE HI
SENSE LO
OUT LO

Figure 2-10. Switch Matrix Configuration for 2.2V dc Range

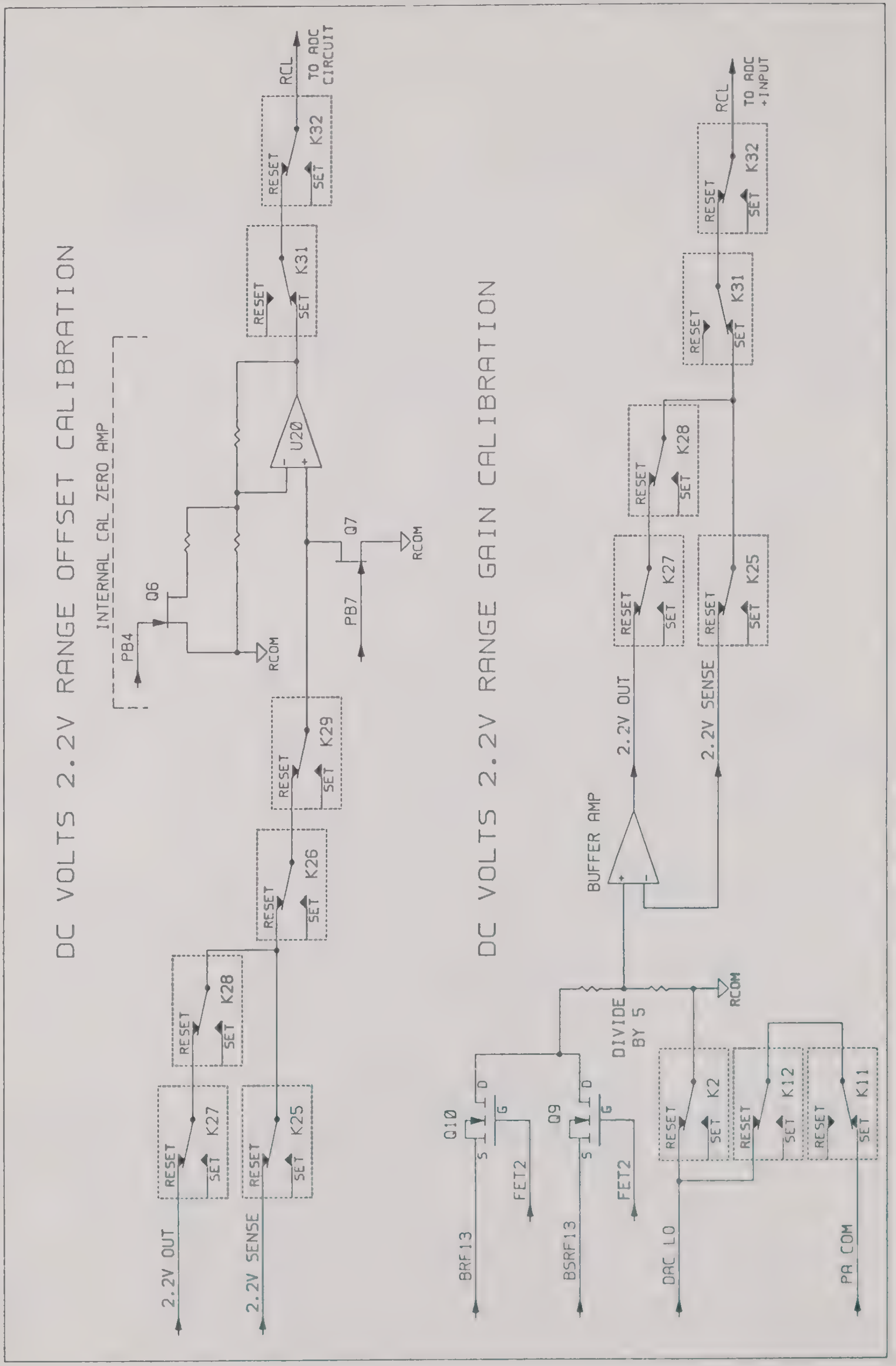

DC VOLTS 2.2V RANGE OFFSET CALIBRATION
INTERNAL CAL ZERO AMP
2.2V OUT
2.2V SENSE
RESET
SET
K27
K25
K28
K26
K29
PB4
Q6
RCOM
U20
Q7
PB7
RCOM
K31
K32
RCL
TO ADC CIRCUIT
DC VOLTS 2.2V RANGE GAIN CALIBRATION
BRF13
BSRF13
DAC LO
PA COM
Q10
Q9
D
G
S
FET2
FET2
DIVIDE BY 5
RCOM
K2
K12
K11
BUFFER AMP
2.2V OUT
2.2V SENSE
K27
K25
K28
K31
K32
RCL
TO ADC +INPUT

Figure 2-11. Calibration of the 2.2V dc Range

To calibrate the offset:

1. The gain of the internal cal zero amplifier is set to 130 by turning on Q6 via PB4.

2. A checkpoint reading is taken, which represents 0V at the input of the internal cal zero amplifier. In this configuration, PB7 turns on FET Q7 connecting RCOM to the internal cal zero amplifier input, K29 is open (set position), and the output of the cal zero amplifier is connected to RCL via relays K31 and K32.

3. The input of the internal cal zero amplifier is connected to the output of the 2.2V range. The 2.2V range is adjusted until the adc reads the same as the checkpoint reading within the given tolerance. In this configuration, 2.2V OUT and 2.2V SENSE are tied together by relay K28 and the output (INT SENSE HI) of the range is channeled into the internal cal zero amplifier input (page 1) through relay K29.

To calibrate the gain of the 2.2V range, the 13V buffered reference (BRF13 and BSRF13) from the DAC assembly (A11) is connected to the input of the 2.2V range by FETs Q9 and Q10 on page 3 of the schematic. Since this network divides the voltage by five, a voltage of 2.6V is obtained at the 2.2V OUT and 2.2V SENSE points. These points are tied together by relay K28. This voltage is then channeled to the RCL line by relays K31 and K32 where it is connected to the +input of the adc amplifier on the DAC assembly (A11). The DAC output is connected to the -input of the adc amplifier and is adjusted until a null is achieved. At this point, the DAC voltage represents the output voltage of the 2.2V range. Gain is determined since the output, input, and offset of the 2.2V range are now known.

2-94. SWITCH MATRIX OPERATION: 220 mV DC RANGE

Refer to Figure 2-12 for the following discussion. The 220 mV range is an extension of the dc 2.2V range. The 2.2V range is divided by ten to produce the 220 mV range. This 10:1 divider (on page 2 of the Switch Matrix Schematic) is part of the resistor network on the 4HR1 assembly.

The 220 mV range is passive with an output resistance of 50 ohms. This range is generated by connecting the 2.2V OUT and 2.2V SENSE to pin 3 of the 10:1 divider by relays K16 and K6. Lines PA COM and R COM are connected to pin 2 of the 10:1 divider by relays K11 and K21. This divided output from pin 1 is called AC/DC mV on the schematic. This portion of the resistive attenuator is also used for generating the ac 2.2 mV and 22 mV ranges. The AC/DC mV signal is then connected to INT SENSE HI through relay K17A on page 1 of the Switch Matrix schematic. Line INT SENSE HI is connected to the OUTPUT HI binding post through relays K2 and K3 on the Motherboard. Sensing for the LO occurs by connecting R COM and PA COM via K11 and K21. A single line is run out to the OUTPUT LO binding post by relay K33 on the Switch Matrix.

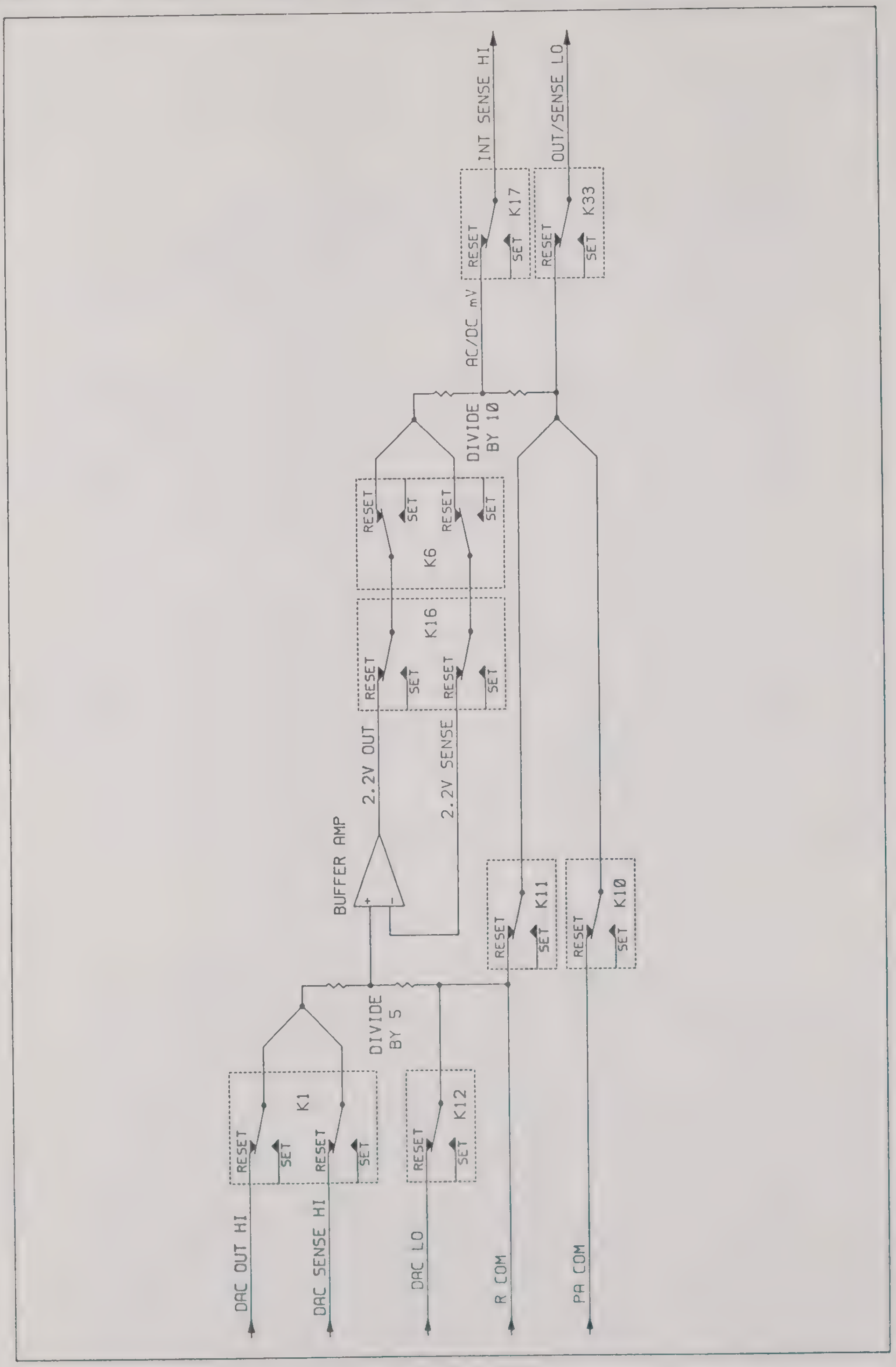

INT SENSE HI
OUT/SENSE LO
RESET
SET
K17
RESET
SET
K33
AC/DC mV
DIVIDE BY 10
RESET
SET
RESET
SET
K6
RESET
SET
RESET
SET
K16
2.2V OUT
2.2V SENSE
BUFFER AMP
+
-
RESET
SET
K11
RESET
SET
K10
DIVIDE BY 5
RESET
SET
RESET
SET
K1
RESET
SET
K12
DAC OUT HI
DAC SENSE HI
DAC LO
R COM
PA COM

Figure 2-12. Switch Matrix Configuration for 220 mV dc Range

2-95. SWITCH MATRIX OPERATION: 220 mV AC RANGE

Refer to Figure 2-13 for the following discussion. As previously mentioned, the ac 220 mV range uses the same resistor network as the dc 220 mV range. In generating the ac 220 mV range the Oscillator assembly is set to the 2.2V range. Lines OSC OUT and OSC SENSE are connected to pin 3 of the 10:1 divider by relays K5 and K6. Lines OS COM and OSC SENSE LO are connected to pin 2 by relays K11 and K9 respectively.

This divided output from pin 1 is referred to as AC/DC mV on the schematic. The AC/DC mV is then connected to INT SENSE HI through relay K17 on page 1 of the Switch Matrix schematic. Signal INT SENSE HI is connected to the OUTPUT HI binding post through relays K2 and K3 on the Motherboard. Sensing for the LO occurs by connecting OS COM and OSC SENSE LO via K11 and K9. A single line is run out to the OUTPUT LO binding post by relay K33 on the Switch Matrix.

2-96. SWITCH MATRIX OPERATION: 2.2 mV AND 22 mV AC RANGES

Refer to Figure 2-13 for the following discussion. The ac 2.2 mV and 22 mV ranges use the 100:1 divider and the 10:1 divider of resistor network on 4HR1 for a total division of 1000:1. Switch Matrix operation for these two ranges is the same. For the 2.2 mV range, the Oscillator assembly is set to the 2.2V range. For the 22 mV range, the Oscillator assembly is set to the 22V range.

Signals OS COM and OSC SENSE LO are connected to pin 6 of the 100:1 divider and pin 2 of the 10:1 divider by relays K11 and K9. OSC OUT and OSC SENSE are connected to the input (pin 7) of the 100:1 divider by relay K3 (A and B). The output of this 100:1 divider is then connected to the input of the 10:1 divider (pin 3) by relay K7. At the output of the 10:1 divider (called AC/DC mV on the schematic) there is a total division of 1000:1. Connection to the binding posts is done in the same manner as in the ac 220 mV range. In all cases, the output impedance of the millivolt ranges is 50 ohms.

2-97. CALIBRATION OF THE mV RANGES

Calibration of the mV ranges involves determining the resistor ratios of the 10:1 divider and the 1000:1 divider (100:1 and 10:1 dividers cascaded). In addition, an offset calibration is performed on the 10:1 divider to remove thermal EMF error for the 220 mV dc range.

Refer to Figure 2-14 for the following discussion. The 10:1 divider offset is calibrated by configuring the Switch Matrix for the 220 mV dc range, except with the output of the range (AC/DC mV) switched into the input of the internal cal amplifier through relays K17 and K29. The Calibration procedure is the same as described for the 2.2V range offset calibration except that during a checkpoint reading, control line PC4 turns on Q11 which connects SWM SENSE LO to the input of the zero amplifier, representing 0V for the 220 mV range.

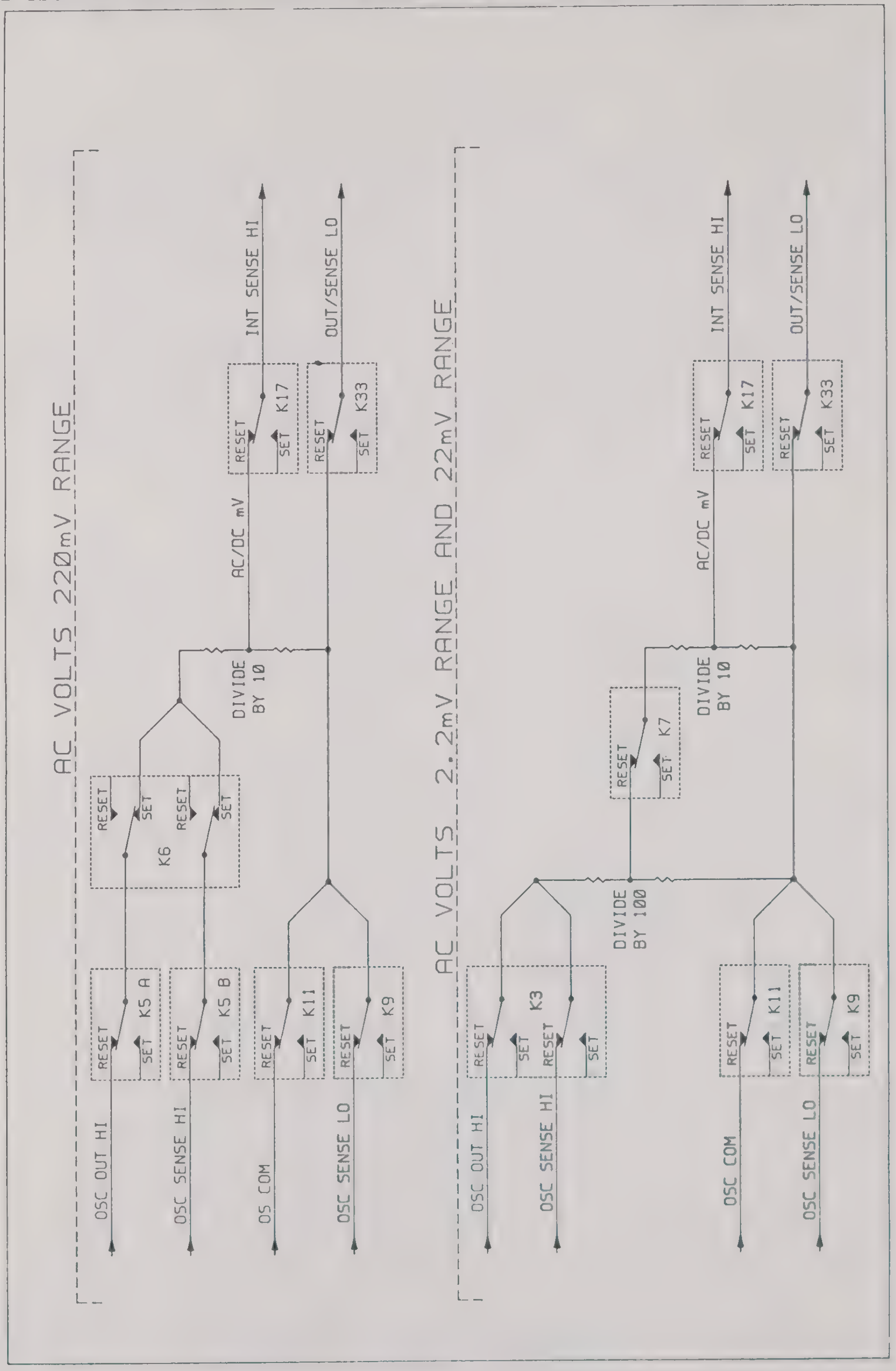

AC VOLTS 220mV RANGE
OSC OUT HI
OSC SENSE HI
OS COM
OSC SENSE LO
RESET
SET
K5 A
K5 B
K11
K9
K6
DIVIDE BY 10
AC/DC mV
INT SENSE HI
OUT/SENSE LO
K17
K33
AC VOLTS 2.2mV RANGE AND 22mV RANGE
OSC OUT HI
OSC SENSE HI
OSC COM
OSC SENSE LO
K3
K11
K9
DIVIDE BY 100
K7
DIVIDE BY 10
AC/DC mV
INT SENSE HI
OUT/SENSE LO
K17
K33

Figure 2-13. 220 mV ac, 2.2 mV ac, and 22 mV ac Ranges

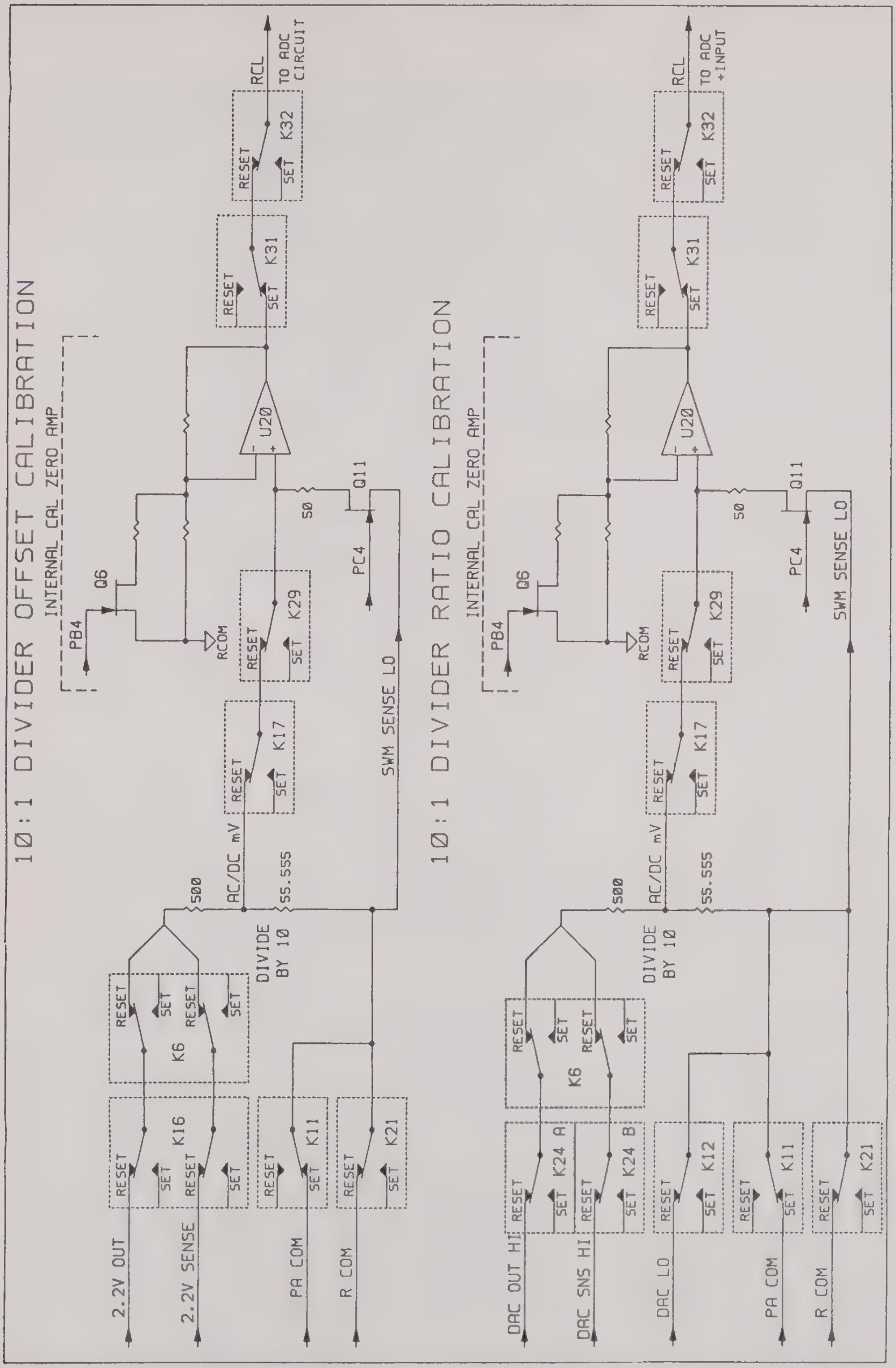

10:1 DIVIDER OFFSET CALIBRATION
2.2V OUT
2.2V SENSE
PA COM
R COM
K16
K6
K11
K21
RESET
SET
DIVIDE BY 10
500
55.555
AC/DC mV
K17
K29
RCOM
Q6
PB4
INTERNAL CAL ZERO AMP
U20
50
Q11
PC4
SWM SENSE LO
K31
K32
RCL
TO ADC CIRCUIT
10:1 DIVIDER RATIO CALIBRATION
DAC OUT HI
DAC SNS HI
DAC LO
PA COM
R COM
K24 A
K24 B
K12
K11
K21
K6
DIVIDE BY 10
500
55.555
AC/DC mV
K17
K29
RCOM
Q6
PB4
INTERNAL CAL ZERO AMP
U20
50
Q11
PC4
SWM SENSE LO
K31
K32
RCL
TO ADC +INPUT

Figure 2-14. 10:1 Divider Calibration

Calibration of the 10:1 divider ratio is accomplished by connecting the DAC assembly output (DAC OUT HI and DAC SENSE HI) through relays K24 (A and B) and K6 to the input of the 10:1 divider. DAC LO, PA COM, and R COM are connected to the common of the 10:1 divider by relays K12, K11, and K21 respectively. The DAC output is set to 2.2V to produce approximately 0.22V at the output of the 10:1 divider (AC/DC mV). Relays K17 and K29 direct this voltage to the internal cal zero amplifier, which is configured for a gain of 10, giving 2.2V plus an unknown error at its output.

The equation for this output is the DAC output (2.2V) multiplied by the 10:1 divider ratio (unknown) multiplied by the internal cal zero amp gain (calibrated, approximately 10). Once the output of the internal cal zero amplifier is determined, the 10:1 divider ratio is the only unknown, so it can be calculated.

To determine the output of the internal cal zero amplifier for this configuration, a checkpoint reading is first taken by connecting both inputs of the DAC's adc amplifier to the DAC output, which is set to 2.2V. This reading represents a null at 2.2V. The output of the internal cal zero amplifier is then channeled to the RCL line by relays K31 and K32 and to the +input of the adc amplifier on the DAC assembly with the DAC output still connected to the -input. An adc reading is now taken and the checkpoint reading is subtracted from it. This value is the adc's representation of the deviation of the internal cal zero amplifier output from 2.2V.

However, due to inaccuracy in the adc, an additional step must be taken. The -input of the adc amplifier is connected to RCOM and the +input to the DAC output. The DAC output is adjusted until the adc reads the previous value within the given tolerance. At this point, the DAC output voltage represents accurately the deviation of the internal cal zero amplifier output from 2.2V. The output of the internal cal zero amplifier is now calculated, allowing the 10:1 divider ratio to be determined.

Refer to Figure 2-15 for the following discussion. Calibration of the 100:1 divider ratio is similar to calibration of the 10:1 divider ratio. The 13V buffered reference (BRF13 and BSRF13) is connected to the input of the 100:1 divider pin 7 by relay K4 (A and B). DAC LO, PA COM , and R COM are connected to pin 6 of the 100:1 divider by relays K12, K11, and K21 respectively. The voltage at the divider output (pin 5) is approximately 0.13V. Relay K7 connects the output of the 100:1 divider to the input of the 10:1 divider. Relays K6 and K8 connect it to the ac mV CAL line, which is the input to the internal cal zero amplifier. The result is 1.3V at the amplifier output. This voltage is switched onto the RCL line by relays K31 and K32 to the DAC assembly, where the DAC is nulled to it. At this point, the DAC voltage represents the internal cal zero amplifier output and the 100:1 divider ratio is calculated.

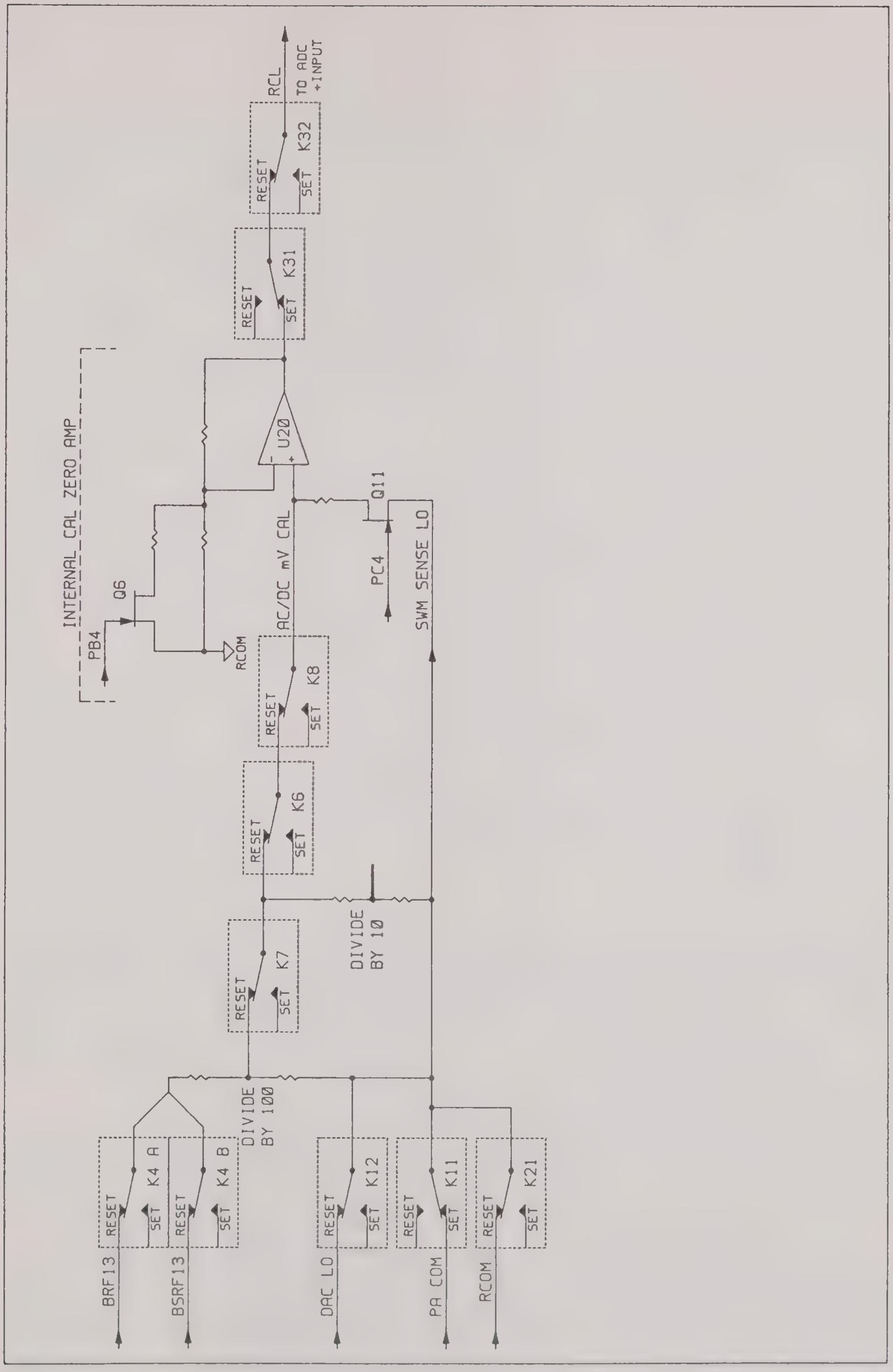

BRF13
BSRF13
DAC LO
PA COM
RCOM
RESET
SET
K4 A
K4 B
K12
K11
K21
DIVIDE BY 100
K7
DIVIDE BY 10
K6
K8
RCOM
PB4
Q6
INTERNAL CAL ZERO AMP
AC/DC mV CAL
U20
Q11
PC4
SWM SENSE LO
K31
K32
RCL
TO ADC +INPUT

Figure 2-15. 100:1 Divider Gain Calibration

2-98. INTERNAL CAL ZERO AMPLIFIER

The main function of the internal cal zero amplifier is to remove the offsets of each of the dc ranges except the 1100V range. (The 1100V dc range is zeroed at the High Voltage/High Current assembly.) The internal cal zero amplifier is switched into two gain configurations for range zeroing; a gain of 130 for the 22V ranges and below, and a gain of 10 for the 220V range. Each range is channeled into the internal cal zero amplifier via relay K29. The range is then compared against 0V by connecting R COM to the amplifier via FET Q7. For the 220 mV range, the reading for 0V (or checkpoint reading) is taken by turning on Q11 instead of Q7 in order to achieve a 50 ohm impedance. The output of the amplifier is connected to the RCL line by relays K31 and K32, and then channeled to the DAC assembly where the signal is measured by the adc.

The internal cal zero amplifier is outlined in a broken line rectangle on page 1 of the schematic. Its functional parts are U20-U21, R43-44, R46-47, Q6-7, Q11, and Z2. When Q7 is on, the input of the zero amplifier is connected to 0V for a reference point. When Q6 is on, the gain of the zero amplifier is 130. Op amp U21 and its associated resistors form a current-cancellation circuit. It senses the output of the zero amplifier and creates a current equal in magnitude but opposite in polarity to the current through the gain resistors (Z2), resulting in zero current in the precision common (RCOM).

2-99. SWITCH MATRIX 5725A AMPLIFIER INTERFACE

The Switch Matrix also provides switching between the calibrator and the 5725 Amplifier. The ac and dc input signals necessary to operate the 5725A are connected by relay K22. Relay K23 connects B SNS LO to either OSC SENSE LO or R COM via relay K14.

2-100. DAC Assembly (A11)

The DAC (digital-to-analog converter) is the basic building block of the calibrator. Other assemblies create ac and dc voltages and currents with its precision dc voltage. The DAC contains five assemblies:

- DAC Main Board (A11)
- DAC Filter SIP (A11A1)
- DAC Buffered Reference SIP (A11A2)
- Reference Hybrid (HR5)
- DC Amplifier Hybrid (HR6).

The DAC assembly serves two main functions:

- To provide a highly repeatable stable dc voltage
- To support calibration of the calibrator

The DAC's adc circuit is used to accomplish calibration. It is made up of an analog to digital converter (adc) and the adc amplifier. Together, these are used to completely characterize the calibrator, using only one external voltage source and two external resistor standards.

2-101. BASIC DAC THEORY OF OPERATION

Figure 2-16 is a simplified schematic of the DAC assembly. The DAC uses a pulse-width-modulated scheme to produce a precision dc voltage of 0V to 22V with positive and negative polarity. The DAC contains:

- A 13V temperature-controlled reference hybrid (HR5)
- Duty-cycle control circuitry
- A five-pole active filter (A11A1 assembly)
- An output stage
- Digital control circuitry

These basic subcircuits work together for a stable and linear dc voltage.

The DAC assembly also contains:

- A sense-cancellation circuit
- Linearity control circuits
- Negative offset circuit
- An output switching circuit

The two inputs of the five-pole filter are two precision square waves with different fixed amplitudes and independently variable duty cycles controlled by software. The filter's first input square wave is called the first channel. It is switched between the reference voltage (13V) and 0V.

The filter's second input square wave is called the second channel. It is switched between approximately 0.78 mV and 0V. Its amplitude is derived by resistively dividing the 13V reference. This second channel is used for extra resolution.

The filter rejects all ac components of the waveforms above 10 Hz. Since the frequency of the square waves is 190 Hz, the output of the filter is a dc voltage which is the sum of average voltages of the two waveforms. The Output Stage, which consists of the dc amplifier hybrid and the output buffer, isolates the filter output from the DAC output and gives current drive to the DAC output.

The output stage has a current limit of approximately 60 mA. It can be configured for a gain of one for the 11V range, or a gain of two for the 22V range. Relays on the DAC output lines allows them to be inverted for negative polarity.

To change the DAC voltage, the average value of the two square waves must be varied. To determine the average value, multiply the waveforms amplitude by its duty cycle. Vary the duty cycle and keep the amplitude fixed to change the DAC voltage.

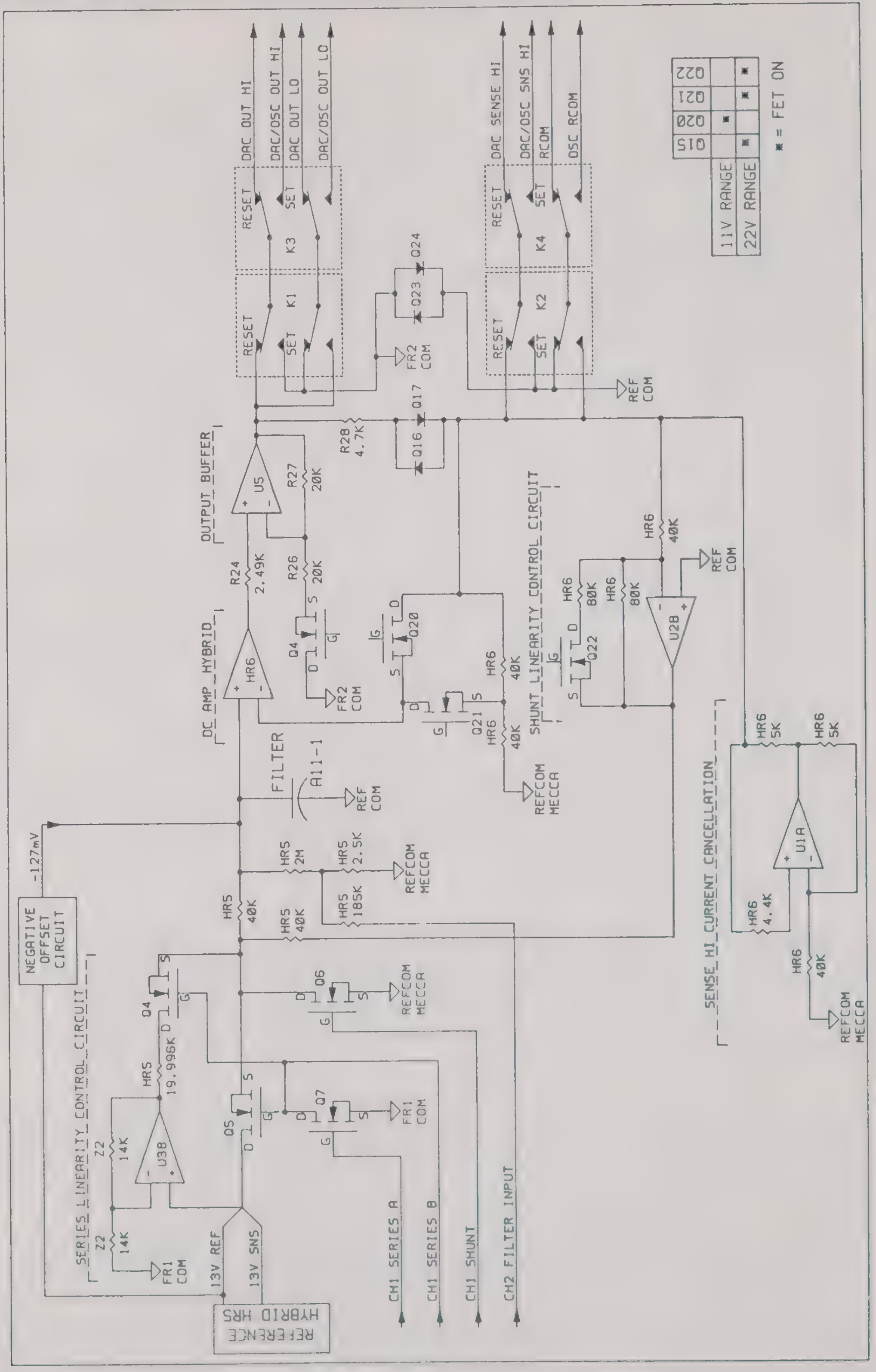

DAC OUT HI
DAC/OSC OUT HI
DAC OUT LO
DAC/OSC OUT LO
DAC SENSE HI
DAC/OSC SNS HI
RCOM
OSC RCOM
RESET
SET
K3
K1
K4
K2
Q24
Q23
FR2 COM
REF COM
Q17
Q16
R28 4.7K
OUTPUT BUFFER
U5
R27 20K
R26 20K
R24 2.49K
DC AMP HYBRID
HR6
Q4
Q20
Q21
HR6 40K
SHUNT LINEARITY CONTROL CIRCUIT
HR6 80K
Q22
U2B
FILTER
A11-1
REFCOM MECCA
-127mV
NEGATIVE OFFSET CIRCUIT
HR5 40K
HR5 2M
HR5 2.5K
HR5 185K
Q6
SERIES LINEARITY CONTROL CIRCUIT
HR5 19.996K
U3B
Z2 14K
Q5
Q7
FR1 COM
13V REF
13V SNS
REFERENCE HYBRID HRS
CH1 SERIES A
CH1 SERIES B
CH1 SHUNT
CH2 FILTER INPUT
SENSE HI CURRENT CANCELLATION
U1A
HR6 5K
HR6 4.4K
Q15 Q20 Q21 Q22
11V RANGE: Q20 *
22V RANGE: Q15 * Q21 * Q22 *
* = FET ON

Figure 2-16. DAC Assembly Simplified Schematic

For example, if the duty cycle of the first channel is 10% and the second channel 50%, the overall average voltage would be:

$$(0.1 \times 13V) + (0.5 \times 0.78\ mV) = 1.300390V.$$

The duty cycle resolution is 0.0024%, which gives a first channel resolution of 0.309 mV and second channel resolution of 18.5 nV.

The duty cycle control circuitry creates the two digital square waves for the first and second channels. These two waveforms are first run through optocouplers for isolation and then into analog switching and level shifting circuits. These circuits derive the proper signals to switch the input of the filter at the levels explained above.

2-102. DAC ASSEMBLY DIGITAL CONTROL

The digital control circuit is located on page 6 of the DAC schematics. The 82C55 Programmable Peripheral Interface IC (U31) is the heart of this circuit.

This IC, which is under software control via the guarded digital bus, has three ports that provide 24 static lines. Port A (PA0-PA7) is configured as a read-only port register. It passes the adc readings from the ADC IC (U25) to the guarded digital bus.

PB0-PB4 of port B control relays K1-K4 and K6-K8 via relay drivers U33 and U34. PB0 is also control line DAC OUT SEL used to turn on FET Q25, via FET Q26, and connect RCOM to SCOM during calibrator operation in the ac function.

PC7 of port C, buffered by U8A, provides the enable for these relay drivers. Relay driver U33 controls latching relays K7 and K8. Outputs from U33 are also used by Relay driver U34 to control latching relays K1-K6. PB5-PB7 are decoded by U32 to create six control lines. These control lines are used to select one input to the adc amplifier -input. K5SEL is an input to the relay drivers to control latching relay K5. The remaining five control lines are used by comparators in U35 and U36. These comparators provide the proper level shifting to create control lines BSRF6 SEL, BSRF13 SEL, REF6 SEL, REF13 SEL, and ADC COM SEL. These control lines are used to control FETs on the DAC Buffered Reference SIP assembly (A11A2).

PC0 of port C is buffered by U8 (B and C) and routed through opto-isolator U37 to create RANGE SELECT, which sets the DAC to the 11V or 22V range. PC1 is used in the duty cycle control circuit to shut off the 8 MHz clock via buffer U8F and the first channel via OR gate U9D. This is done during calibrator operation in the resistance function. PC2 controls a FET in U23 for use in self-diagnostics. PC3 and PC4 are level-shifted by comparators in U36 before they are used to control FETs in U23. PC5 of port C is connected to a comparator in U36. This comparator provides the proper level shifting to create control line ADCAMP OUT SEL to control a FET in U23. PC6 is control line ADC TRIGGER which triggers the adc (analog-to-digital converter) IC U25. A0, A1, and CS*, from the guarded digital bus, are used by OR gates in U9 (B and C) to create control line ADC READ for use by the adc IC U25.

2-103. DAC ASSEMBLY REFERENCE CIRCUITRY

The reference circuitry is on the reference hybrid, located on the HR5 assembly. The HR5 assembly contains a ceramic substrate reference hybrid bonded to a resistor network.

All components on this assembly are surface mount devices, except U6 and U7. The resistors are screened with a thick film paste. Associated resistors, capacitors, and zener diodes are mounted on the main board to supply this hybrid with the appropriate power and ground returns.

As previously explained, the amplitudes of the pulse width modulated signals for the first and second channel are assumed to be fixed. Any change in amplitude shows up as an error on the output of the DAC. Since the reference is used to determine the amplitude, it must be very stable and generate little noise.

The 13V reference contains two cascaded 6.5V temperature compensated transistor/zener diode pairs called ref amps (U6 and U7). The excellent temperature characteristics of the ref amps are obtained by biasing the collector current on their transistors with a value such that the TC (temperature coefficient) of its base-emitter junction cancels the TC of the zener diode. Since the base-emitter junction and the zener diode are in series, the result is a near zero TC.

Correct bias currents are achieved with a thin-film resistor network in a surface-mount package mounted on the hybrid.

The reference circuit is designed such that the effects of the thin-film resistors and op amp errors are second order. Thus, accuracy is determined almost entirely by the ref amps.

To further reduce the effects of ambient temperature variations, the hybrid is heated to a constant 62 oC by the heater control circuitry on page 1 of the DAC schematic.

Temperature is sensed near the ref amps by a thermistor (RT1). If the substrate temperature changes, the thermistor resistance changes. This creates a correction voltage to the base of Q2 (on the main board). This, in turn, causes the power into the heater resistor, which is screened on the back of the substrate, to increase or decrease as necessary to maintain a stable temperature.

Thermal runaway is prevented by a protection circuit. Once the substrate temperature reaches approximately 67°C, the change in resistance of RT2 causes Q9 to turn on. As transistor Q9 turns on, it steals base current from Q1 on the main board, which brings it out of saturation. This breaks the current path through the heater resistor. This condition exists only if there is a failure.

The exact value of the reference is determined during calibration. Because of the stability of the reference, it can be used for future internal calibration procedures to remove short term errors in the calibrator.

The 13V output, REF13 HI, is from pin 9 and REF13 SENSE is on pin 12. Also, a 6.5V reference line, REF6, is brought out on pin 14 of the reference for use during calibration.

In order to make these reference voltages available to other assemblies, the 6.5V and 13V references are buffered on the DAC Buffered Reference SIP assembly (A11A2). This assembly also contains the circuitry to switch the references and buffered references into the input of the adc during calibrator calibration. Refer to the section on the DAC Buffered Reference SIP for more information.

2-104. DUTY-CYCLE CONTROL CIRCUIT

Duty-cycle control circuitry is pictured on page 3 of the schematics. DAC output voltages are represented in software by what are called first and second channel counts. Each count is a 16-bit number which is sent to the DAC assembly via the guarded digital bus.

For example, a first channel count of 20,000 (in decimal) represents a DAC output voltage of approximately 6.5V (half the reference voltage).

The first function of the duty-cycle control circuitry is to convert each count into a stable, TTL level, square wave, with a duty cycle proportional to the numeric value of the count. This is accomplished with the 82C54 programmable interval timer (U6).

A low-level 8 MHz clock is generated on the Regulator/Guard Crossing assembly (A17) and routed to the DAC assembly via the motherboard. This low-level clock, CLK and CLK*, is amplified to a TTL level by comparator U7 to generate the 8 MHz clock which is used by U6 and the adc IC U25.

The 82C54 programmable interval timer receives its input counts from the guarded digital bus and creates the second channel signal on OUT2 (pin 20) and the first channel signal on OUT1 (pin 16).

The second channel signal is buffered by U8 (D and E) and runs through opto-isolator U12 to become CH2 FLOATING. This signal alternately turns FETs Q30 and Q32 on and off to turn the 3V source (called 3V) into a floating 3V pulse width modulated waveform called CH2 FILTER INPUT.

The 3V source is created from the 13V reference. The 13V reference is buffered by op amp U1B, configured as a voltage follower. The output from U1B is divided down to 3V by a 100 kilohm and 30 kilohm resistor in the HR5 assembly, creating 3V.

This 3V is again buffered by op amp U11, configured as a voltage follower, to create the 3V, which is switched by FETs Q30 and Q32. CH2 FILTER INPUT uses three resistors on the HR5 assembly to resistively divide its 3V amplitude by an additional factor of approximately 3800.

The first channel signal is buffered by U8 (G and H) and run through opto-isolator U13, to become CH1 FLOATING. Since the first channel is much more critical than the second, CH1 FLOATING is clocked into a flip flop (U14) to insure an accurate waveform.

To clock in this waveform, the low-level 8 MHz clock (CLK and CLK*) from the Regulator/Guard Crossing assembly (A17) is isolated by transformer T1 and amplified to a TTL level by comparator U10. This generates the clock inputs for U14. The output Q1 (pin 5) from U14 creates CH1 SERIES A, which switches Q7. The output Q1* (pin 6) is inverted by Q35, creating CH1 SHUNT, which switches Q6. The output Q1*, which is a TTL level, is also amplified by components Q33, Q34, VR11, VR12, and R44-R46, so it switches from 0 to 18V, creating CH1 SERIES B, which switches Q4 and Q5.

The watchdog timer sets the first channel filter input to 0V if a failure occurs on the 8 MHz clock. This circuit uses a monostable multivibrator (one shot) U15, C63, and R48. The 8 MHz clock is divided to 4 MHz by U14. This 4 MHz clock is connected to U15 and discharges C63 to ground. If the 4 MHz clock stops, C63 charges up, causing the Q1 output of U15 to go low. This logic low on Q1 is connected to the preset pin of U14 (PRI), which causes its Q1 output high and its Q1* output low. This condition turns on the shunt switch and turns off the series switch, which forces the filter input to be REFCOM.

2-105. DAC FILTER CIRCUIT

The dac filter circuit is located on the DAC Filter SIP (A11A1) assembly. The dominant pole of the filter is near 10 Hz. This gives 120 dB of rejection at 190 Hz.

The +30FR1 supply and 15V zener diode, VR1, create the 15V supply (15V) for the op amps in the filter circuit. 15V is also connected to the main DAC board, where it is used with R111 as a pull up for the RANGE SELECT control line.

2-106. DAC OUTPUT STAGE

The output stage of the DAC assembly consists of the DC Amplifier Hybrid assembly (HR6) and the output buffer circuitry. Like the Reference Hybrid, the DC Amplifier Hybrid is constructed of surface-mount components (except precision op amp U2), on a ceramic substrate hybrid, bonded to a resistor network.

It is temperature-controlled by a heater control circuit in the same manner as explained on the Reference Hybrid. Transistor Q3 provides proper power to the heater resistor.

The DC Amplifier Hybrid consists of a precision op amp U2, with a bootstrapped power supply (Q1, Q2, R1-R4, VR1-VR2). The op amp has low noise and low offset. It is bootstrapped to improve the common-mode rejection in its noninverting configuration.

The DC Amplifier assembly interfaces with the output buffer (U5) to create the output stage. Control line RANGE SELECT configures this output stage for unity gain for the 11V range or a gain of 2 for the 22V range. In the 11V range, Q15 is turned off, which gives U5 unity gain, and Q20 is on, which gives the DC Amplifier unity gain.

In the 22V range, Q20 is off and Q21 is on, which switches in the 40 kilohm feedback resistors located on the HR6 assembly. Precise ratio matching of these resistors provides high accuracy in the 22V range.

FET Q15 is on in the 22V range so that the output of the dc amplifier is half the output of the DAC. This is necessary so that the output of the dc amplifier is approximately the same as its inputs, which allows the bootstrap circuit to work.

The output buffer (U5) provides drive for the DAC output. It is used in a feedback loop with the DC Amplifier Hybrid so that the dc accuracy is dependent upon the dc amplifier, and the output drive capability is dependent on the output buffer.

The output buffer is current-limited to a short circuit current of about 60 mA. The short-circuit protection circuitry works as follows:

The supply current is sensed by R23. When the output current of U5 reaches approximately 50 mA, the voltage across R23 is large enough to turn on Q10. As Q10 turns on, the voltage across R20 increases, and pulls down the supply voltage at pin 4 of U5. In order to prevent the supply of U5 from dropping below the input, Q8 saturates turning on Q11 which shorts the input to FR1 COM. When the short is removed, R22 and C41 cause Q11 to turn off slowly, which prevents a large overshoot at the DAC output.

2-107. SENSE CURRENT CANCELLATION CIRCUIT

This circuit uses op amp U1A and four resistors on the HR6 assembly. This circuit supplies the sense current of equal, but opposite, polarity to the feedback resistors in the 22V range. This eliminates current in the sense lead during external sensing.

2-108. LINEARITY CONTROL CIRCUIT

The linearity control circuitry contains the series linearity control circuit and the shunt linearity control circuit, as outlined on the schematic. These linearity control circuits eliminate filter current in the series switch (Q5) and the shunt switch (Q6). This is necessary because Q5 and Q6 have finite resistance (3 to 5 ohms) and a small mismatch in the resistances can cause a linearity error.

The series linearity control circuit uses op amp U38, resistor network Z2, and a single 19.996 kilohm resistor on the HR5 assembly. This circuit eliminates filter current in the series switch Q5.

When the series switch (FET Q5) is on, it connects the 13V reference to the first channel input of the filter, and FET Q4 is also turned on. This causes U38 to supply the current to the filter through the 19.996 kilohm resistor in HR5 and Q4, which makes the resistance from TP2 to TP5 look like near 0 ohms.

The shunt linearity control circuit uses op amp U2B, FET Q22, three 80 kilohm resistors on the HR6 assembly, and one resistor in the HR5 assembly.

Op amp U2B is configured as an amplifier with an inverting gain of 1 in the 11V range, and an inverting gain of 0.5 in the 22V range. This gain is determined by FET Q22 and the three 80 kilohm resistors in the HR6 assembly.

When the shunt switch (FET Q6) is on, connecting the input of the filter to REFCOM, the current from the filter flows through the two 40 kilohm resistor (pin 7 to pin 8) on the HR6 assembly to the output of U2B. This cancels out the current that would flow through Q6 which makes it look like 0 ohms.

2-109. NEGATIVE OFFSET CIRCUIT

This circuit creates a constant offset voltage of approximately -127 mV at the filter input. Thus, for a DAC output voltage of 0V, the first channel count must be approximately 400 to offset this negative voltage. This guarantees a minimum duty cycle pulse width of approximately 50 us.

This minimum duty cycle is necessary to overcome the offset of the output stage and to allow the reference voltage to settle out after being switched into the filter input. Op amp U2A and two 20 kilohm resistors in HR6 form an amplifier with an inverting gain of 1. This amplifier input is the 13V reference which produces -13V at its output. This -13V is divided by resistors in the HR5 assembly to create the -127 mV on the filter input.

2-110. DAC OUTPUT SWITCHING

The floating outputs of the DAC are switched with latching-type relays K1, K2, K3, K4, and K8.

Relays K1 and K2 determine the polarity of the DAC. In the reset position, the DAC output is positive. In the set position, output is negative. Relay K1 also generates DAC LO DIAG and DAC HI DIAG which are used by the adc circuit during DAC diagnostics.

Relays K3 and K4 switch the DAC to various assemblies. In the reset position, the DAC is available to all assemblies except the oscillator. Relays K3 and K4 are set during operation in the ac function so the DAC output is connected to the DAC/OSC lines which run only to the Oscillator assembly. Also during operation in the ac function, control line DAC OUT SEL turns on FET Q25, via FET Q26, to connect SCOM to RCOM.

Relay K8, when in the set position, allows the DAC to be sensed right on the output of the DAC assembly.

2-111. DAC BUFFERED REFERENCE SIP

The DAC Buffered Reference SIP assembly (A11A2) has two main functions. First, it buffers the the 6.5V and 13V references so they can be used by other assemblies.

The 6.5V reference, REF6, is buffered by op amps U1A and U2A which creates BRF6 and its sense line BSRF6. The 13V reference, REF13 FILT, is buffered by op amps U1B and U2B which creates BRF13 and its sense line BSRF13. These are routed to other assemblies in the calibrator for use during calibrator calibration.

Second, it allows the the reference voltages, or the buffered reference voltages, to be switched to the REFCAL line, which is connected to the inverting input of the adc amplifier by K5 during calibration of the DAC assembly.

Control line REF6 SEL and FETs Q1 and Q2 connect the 6.5V reference REF6 to REFCAL.

Control line BSRF6 SEL and FETs Q5-Q7 tie BRF6 and BSRF6 together and connects them to REFCAL.

Control line REF13 SEL and FETs Q8 and Q9 connect the 13V reference REF13 to REFCAL.

Control line BSRF13 SEL and FETs Q12-Q14 tie BRF13 and BSRF13 together and connects them to REFCAL.

ADC COM can also be connected to REFCAL by FET Q15 and control line ADC COM SEL.

2-112. SELF-CALIBRATION HARDWARE

The main components of the calibration hardware are the adc amplifier and the adc (analog to digital converter). This adc circuitry converts dc analog voltages into 22-bit binary numbers which the software interprets.

2-113. ADC AMPLIFIER

ADC amplifier circuitry is located on page 4 of the DAC schematic. The adc amplifier is used like a null detector. It has two inputs (inverting and noninverting) and a single output with ADC AMP OUT and ADC AMP SENSE connected together.

The noninverting input (+INPUT) is switched between ADC COM, RCL, or DAC SENSE CAL by relays K6 and K7. DAC SENSE CAL is the output of the DAC and RCL is the calibration line which other assemblies use during their calibration.

The inverting input (-INPUT) is switched between DAC SENSE CAL and REFCAL by relay K5. ADC amplifier inputs are high impedance. The output voltage is the voltage difference between the inputs multiplied by the overall adc amplifier gain of 11.

To determine adc amplifier output, the following formula is used:
(Noninverting input - inverting input) X 11 = adc amplifier output.

For example if the noninverting input is a 5.0V and the inverting input is at 5.1V, the output would be -1.1V. (The calculation for this example is (5.0V - 5.1V) X 11 = -1.1V.) Op amp U20A configured as an amplifier with an inverting gain of 1 is used to cancel the current in ADC COM generated from op amp U19A.

Zener diodes VR19 and VR20 keep the output of the adc amplifier from exceeding ±4.0V. Similarly, this protection is provided for the adc amplifier inputs by VR17, VR18, VR21 and VR22.

The advantage of having a gain of 11 is that the noise of the adc is divided by this gain. For example, if the noise of the adc is 4 uV rms, the effective noise of the adc becomes 4 uV/11 = 0.36 uV rms, referred to as the adc amplifier inputs.

2-114. ADC INPUT SELECTION

The input to the adc chip, U25, is selected by a quad FET analog switch array, U23. A large filter (R74 and C84) and a buffer (U24) are put on the adc input line to filter out 60 Hz and 190 Hz before it is connected to the adc chip input (pin 22).

During calibrator diagnostics, control line PC2 selects the SDL (system diagnostic line) line, which is used by other analog assemblies to monitor their diagnostic voltages.

During diagnostics of the DAC assembly control, line PC3 selects DAC HI DIAG which is divided by R79 and R84. Control line PC4 selects DCAMP HEATER and REF HEATER which are summed and divided by R80, R81, and R83.

Since DCAMP HEATER and REF HEATER are referenced to FR1 COM, DAC LO DIAG is buffered by U22 to provide the proper current return.

During calibrator calibration, control line ADC OUT SEL selects the output of the adc amplifier.

2-115. ADC CIRCUIT

The adc (analog-to-digital converter) is shown on page 5 of the DAC schematic.

Most of the adc is contained on one chip (U25) which uses the Fluke-patented recirculating remainder technique.

The adc has rms noise of approximately 20 uV between readings. This is reduced by a factor of 5 by averaging the readings. The adc measures input voltages between -1.8V and +1.8V.

Hardware for the adc has four major sections external to adc IC U25. These sections are:

- ADC reference voltage
- ADC dac
- ADC comparator/amplifier
- Timing/data control circuitry.

The adc reference voltage circuit is made up of zener diodes VR29, VR30, and resistors R91-R93, which generate a 6.4V reference. This -6.4V is inverted by U27B to create the +6.4V reference and is also buffered by U27A and connected to U25. A reference common point for the adc reference is made by buffering ADC COM with op amps U20B and U26A, resulting in an isolated ADC COM. Buffering allows the common point to be referenced to ADC COM, yet current from R85, C89, C90, R93, VR29, and VR30 to return to SCOM through the output of the buffer instead of through ADC COM.

The adc dac contains the dac amplifier, U28B, and a binary ladder network consisting of resistors in Z10. Digitally controlled analog bit switches are contained in U25. The bit switches determine the output voltage of U28B by control of the binary ladder network. The output voltage of U28B can be varied from -1.95V to 1.95V.

The adc comparator/amplifier contains op amp U29, two remainder storage capacitors (C89 and C90), an autozero storage capacitor (C95), and several digitally-controlled analog switches in U25.

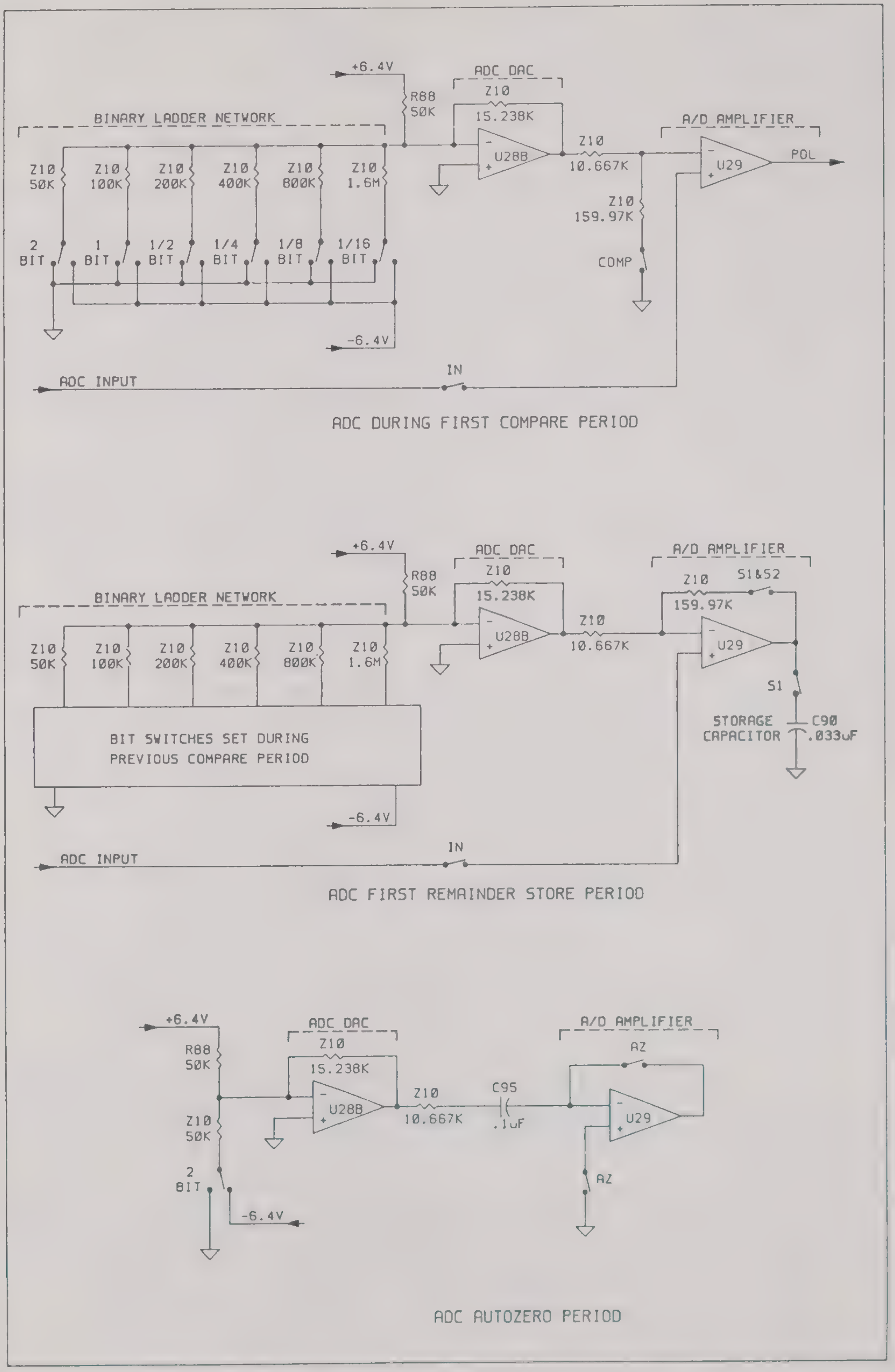
The supplies for U29 are bootstrapped off its input voltage. This circuitry includes U28A, VR31-VR34, R95-R100, Q56, Q57, and C97.

The timing/data control circuit is the digital portion of U25. This internal circuitry controls the adc by manipulating the switches in the adc comparator/amplifier and the bit switches in the adc dac.

An adc conversion cycle is triggered by the falling edge of control line ADC TRIGGER from the digital control circuit. Once triggered, the adc, under control by U25, generates five 6-bit nibbles without any further interaction.

Once the adc is triggered, it goes through five measurement cycles. Each cycle is made up of three functions, an autozero function, a compare function and a remainder store function. Figure 2-17 illustrates these three functions.

Before the adc is triggered, it stays in the autozero function. In this function, the adc dac is set to 0V with some offset error. Through U25, pin 3 of U29 is connected to ADC COM and pins 2 and 6 are connected together. In this function, the offset of the adc dac is stored on C95.


+6.4V
ADC DAC
R88
50K
Z10
15.238K
BINARY LADDER NETWORK
A/D AMPLIFIER
Z10
10.667K
U28B
U29
POL
Z10 50K
Z10 100K
Z10 200K
Z10 400K
Z10 800K
Z10 1.6M
Z10
159.97K
2 BIT
1 BIT
1/2 BIT
1/4 BIT
1/8 BIT
1/16 BIT
COMP
-6.4V
ADC INPUT
IN
S1&S2
S1
STORAGE CAPACITOR
C90
.033uF
BIT SWITCHES SET DURING PREVIOUS COMPARE PERIOD
C95
.1uF
AZ

ADC DURING FIRST COMPARE PERIOD

ADC FIRST REMAINDER STORE PERIOD

ADC AUTOZERO PERIOD

Figure 2-17. ADC Circuit Measurement Functions

In the compare function, U29 compares the adc dac with the adc input (during the first pass) or the stored remainder (C89 or C90) during the remaining four passes. The voltage to be measured is switched into pin 3. The adc dac is connected to pin 2 and adjusted according to the polarity output of U29 resolving the voltage on pin 3. During this function the six bits of one nibble are determined.

During the remainder store function, U29 amplifies and stores the difference between the ADC INPUT and the adc dac output on one of the remainder storage capacitors, C89 or C90. In this function, U29 is configured by the adc as a difference amplifier with a gain of 16. The output of U29 is now the difference between the input voltage and the DAC voltage, multiplied by 16. This voltage is stored on C89 or C90.

On the next cycle, this remainder voltage is switched into U29 as the input voltage during the compare function.

Once this is repeated five times, U25 sends out an interrupt signal (ADC INT) to tell the processor that it is waiting to read. To read the five passes of the adc, the processor reads port A of the 82C55 five times.

For the most critical applications, the adc measures the output of the adc amplifier. Since the output of the adc amplifier is adjusted until it reaches a checkpoint voltage, the adc needs only to be repeatable at this voltage and low in noise. This reduces the constraints on adc linearity and long term stability which allows a much simpler adc reference to be used.

2-116. HOW THE DAC IS USED IN SELF-CALIBRATION

For internal and external calibration, the adc amplifier output is switched to ADC INPUT.

The adc amplifier acts as a null meter. It measures the voltage difference between its inverting and noninverting inputs and amplifies it by a gain of 11.

The adc amplifier can measure common-mode voltages up to 14V. Input switching circuitry allows the DAC SENSE, buffered and unbuffered reference, RCL, and ADC COM to be switched into the adc amplifier inputs.

To make a typical cal measurement, software sets the DAC to the approximate expected common-mode voltage. The DAC is then switched into both adc amplifier inputs and an adc reading is taken. This is the checkpoint measurement. It represents the adc amplifier common-mode and offset error, and the errors in the adc and adc amplifier input switching. The unknown voltage is switched into one input of the adc amplifier and the DAC is adjusted by software until the adc reading matches the checkpoint reading. At this point the unknown voltage is equal to the DAC voltage and is represented by the current DAC counts.

2-117. DAC ASSEMBLY CALIBRATION

The DAC assembly is completely characterized using a single external 10V source. Calibration occurs in the following steps:

Ratio calibration of the first and second channels is performed first. The first channel count is set for a DAC output of near 0V. The second channel count is set to its minimum value of approximately 10,000. The DAC output is connected to the input of the zero amplifier on the Switch Matrix assembly (A8) and its output connected to the +input of the adc amplifier via the RCL line and the -input is connected to ADC COM.

The adc measures this value and stores it as a checkpoint reading. The first channel is decremented by one count and the second channel is increased until the adc reads the same as the previous checkpoint. The number of counts the second channel is increased represents the channel ratio constant.

The ±11V and ±22V range zeros are calibrated next. This is done by the same technique as the ratio cal except the checkpoint reading is obtained by connecting the input of the zero amplifier on the Switch Matrix assembly to RCOM. The DAC output (DAC SENSE CAL) is then connected to the zero amplifier input and adjusted until the adc reads the same as the previous checkpoint. This determines the exact first and second channel counts for a 0V output.

Next, the +11V and +22V range gain constants are calibrated by nulling the DAC to the external 10V source, connected to the front panel binding posts of the calibrator. This 10V source is connected to the RCL line by relays on the Switch Matrix assembly (A8).

The RCL line is connected to the +INPUT of the adc amplifier. The DAC output is connected to the -INPUT of the adc amplifier and is adjusted until the adc reads a null. This determines the first and second channel counts required for an exact 10 V output from the DAC. Software determines floating point gain constants from these counts.

The exact value of all the reference voltages (6.5V and 13V) are determined next. The reference voltage to be determined is connected to the -INPUT of the adc amplifier. The DAC output is connected to the +INPUT and adjusted until the adc reads a null. The reference voltage is the value to which the DAC is set. This procedure is done for the 6.5V buffered and unbuffered, and 13V buffered and unbuffered references.

2-118. Oscillator Section Overview

The ac module consists of two plug-in assemblies, the Oscillator Output assembly (A13) and the Oscillator Control assembly (A12). These assemblies generate a precision amplitude-stabilized ac sine wave from 0.22V to 22V with a frequency range of 10 Hz to 1.2 MHz. This signal is either routed to the OUTPUT binding posts if the desired output is within this range, or used internally by the Power Amplifier, High Voltage, Wideband, Current, Switch Matrix, or an Auxiliary Amplifier (Model 5725A, 5205A, 5215A, or 5220A) for voltages and/or functions outside this range.

Output sensing of the amplitude helps obtain an accurate output signal regardless of output amplitude and load variations. Sensing is available for all voltage ranges above 200 mV at the calibrator SENSE binding posts. In the current function, and for voltages less than 200 mV, sensing is performed internally and output accuracy is guaranteed only for specified operating conditions.

The Oscillator Output assembly (A13) creates an ac voltage. The Oscillator Control assembly (A12) controls the amplitude of this ac signal by comparing the SENSE HI signal from the Oscillator Output with an accurate dc voltage from the DAC assembly (A11). The Oscillator Control assembly adjusts the amplitude of the Oscillator Output via the OSC CONT line. The frequency accuracy is controlled by the phase-locked loop circuit on the Oscillator Output assembly, which phase locks to the signal created by the Current/Hi-Res assembly (A7), or to an external signal connected to the 5700A rear panel through the PHASE LOCK IN jack.

The following discussions separately cover these two assemblies.

2-119. Oscillator Control Assembly (A12)

The Oscillator Control assembly (A12) contains all the precision ac amplitude control circuitry except the output AGC amplifier, which is located on the Oscillator Output assembly (A13). The primary function of the Oscillator Control assembly is to monitor the output of the 5700A in the ac voltage function, and to adjust the output until the rms voltage across the SENSE point is equal to the voltage requested by the operator. This assembly provides amplitude control for both the ac current function and the Wideband AC Module (Option -03) during low-frequency operation.

The oscillator control circuitry contains an averaging converter, an error intergrator, a three-pole filter, an ac/dc thermal transfer circuit, an ac/ac thermal transfer circuit, a 15-bit dac, and a digital control circuit.

All power supplies used by this assembly are generated by the Guard Crossing/Regulator assembly (A17) except the +5 OSC supply, which is generated by a three-terminal +5V regulator (U25) from the +15 OSC supply. The ±15 OSC supplies are buffered by L3, L4, C34 and C35 to create the ±15A supplies, and L1, L2, C86 and C87 to create the ±15B supplies. A +2.5V reference voltage is created from the +5LH supply by resistors R52 and R53. A -200 mV reference voltage is created from the -15V OSC supply by resistors R57 and R58 for use exclusively by the protection circuitry for the thermal sensors U14 and U16.

2-120. OSCILLATOR CONTROL DIGITAL CONTROL

The digital control circuit contains an 82C55 Programmable Peripheral Interface (U20) and latching relay drivers (U23, U24). The 82C55 is controlled via the guarded digital bus, and has three ports that generate 24 outputs. Port A (PA0-PA7) is a common input bus (DATA) for the relay drivers (U23, U24) and the 14-bit DAC (U10). Relay driver U23, which controls latching relays K1 through K4, K6, and K8, is strobed by PC5 and enabled by PC7 of port C. Relay driver U24, which controls latching relays K5, K7, and K9, is strobed by PC6 and enabled by PC7 of port C. The SW control bus contains control lines SW1-SW4 from PB4-PB7 of port B which control a CMOS analog switch IC U19. PC1-PC4 of port C create control lines GCAL, AC*/DC, DAC* and BIT14* respectively. The Oscillator Output assembly (A13) generates two more control lines: LFCOMP* and HFCOMP*. These control lines are routed to this assembly via the Motherboard and enter on pins 18A/C and 19A/C of connector P502.

A self-diagnostic circuit contains a multiplexer (U18) and resistor networks Z5 and Z6. It monitors ±15V, VREF, and the outputs of the error integrator and 14-bit DAC. These inputs are divided by the resistor networks, while U18 applies one to the SDL line. The SDL line is routed to the DAC assembly (A11) to be measured by the adc circuit.

2-121. OSCILLATOR INPUT SWITCHING

Relay K1 selects an input to the Oscillator Control assembly. During ac voltage operation, relay K1 is reset. This connects the input (SENSE HI) to the averaging converter and the ac sense buffer to OSC SENSE HI. The reference voltage, VREF, is connected to both DAC/OSC OUT HI and DAC/OSC SENSE HI, which is the dc voltage from the DAC assembly (A11). During internal calibration K1 is set, so VREF is the 6.5V reference voltage (BRF6 and BSRF6) from the DAC assembly. The input to the averaging converter and ac sense buffer is DAC/OSC OUT HI and DAC/OSC SENSE HI from the DAC assembly.

2-122. SENSE CURRENT CANCELLATION

The SENSE HI current cancellation circuit, containing op amp U1, Q1, Q2, K8, K2B and associated components, supplies the current into SENSE HI (Z2 pin 1) so that no current is pulled from the OSC SENSE HI line. During operation in the 2.2V and 22V, range K8 is set so the input is OSC OUT. In the 220V range K8 is reset so OSC SENSE HI is connected to the input. Relay K2B is reset in the 2.2V range and set in the 22V range. Transistors Q1 and Q2 form a bootstrapped supply for U1.

The SENSE LO current cancellation circuit, built around op amp U2, forces the return current back to SCOM instead of OSC SENSE LO. Relay K2A is reset in the 2.2V range and set in the 22V range.

To better understand the detailed circuit descriptions for the averaging converter, error intergrator, and three-pole filter, refer to Figure 2-18.

2-123. AVERAGING CONVERTER

The averaging converter contains the buffer amplifier and rectifying amplifier circuits as outlined on page 1 of the schematic.

The buffer amplifier is a non-inverting unity gain amplifier (U3). Input to the buffer amplifier is either a 0 or 20 dB attenuator contained in Z2 as selected by K3. In the 2.2V range, SENSE HI is connected directly to the buffer amplifier with K3 in the reset position. In the 22V range, K3 is in the set position, so the buffer amplifier input (SENSE HI) is attenuated 20 dB by the 18 kilohm and 2 kilohm resistors in Z2. The buffer amplifier output voltage is always between 0.22 and 2.2V, and is capacitively coupled to the rectifying amplifier by C22 and C25.

The rectifying amplifier is comprised of U5, U7, Q3 and Q4, and has an inverting gain of 2. When the input voltage (from the buffer amp) is positive, feedback is negative through CR5 and a 2 kilohm resistor in Z1 (pins 6 and 5). When the input voltage is negative, the feedback path is through CR4 and a different 2 kilohm resistor in Z1 (pins 3 and 5). This amplifier produces a full-wave rectified negative output current proportional to input voltage. Output current is summed at the input of the error intergrator with the positive adjustable reference current (VREF, which is the output of the DAC assembly).

2-124. ERROR INTEGRATOR

The error integrator circuit contains op amp U11, CMOS analog switch U8A, and capacitors C42 and C43. When operating at frequencies above 119 Hz, op amp U11 and C43 form an integrator. When operating at frequencies below 119 Hz, control line LFCOMP* goes low to close U8A, adding C42 to C43. This reduces the integrator crossover point by a factor of ten. If the magnitude of the averaging converter dc output current is different than the reference current, the output of the error integrator begins to change. Error integrator output goes through a three-pole filter and is buffered by U9A to generate OSC CONT. OSC CONT is routed to the Oscillator Output assembly to adjust the Oscillator amplitude. The output of the error integrator is also monitored by the diagnostic circuit via ERROR INT. OUT.

2-125. THREE-POLE FILTER

The three-pole filter contains op amp U9B, CMOS analog switches U8B-U8D, and C26-C31. This circuit filters out ac from the output of the error integrator. Control line LFCOMP* goes low when operating at 119 Hz or less to reduce the crossover point.

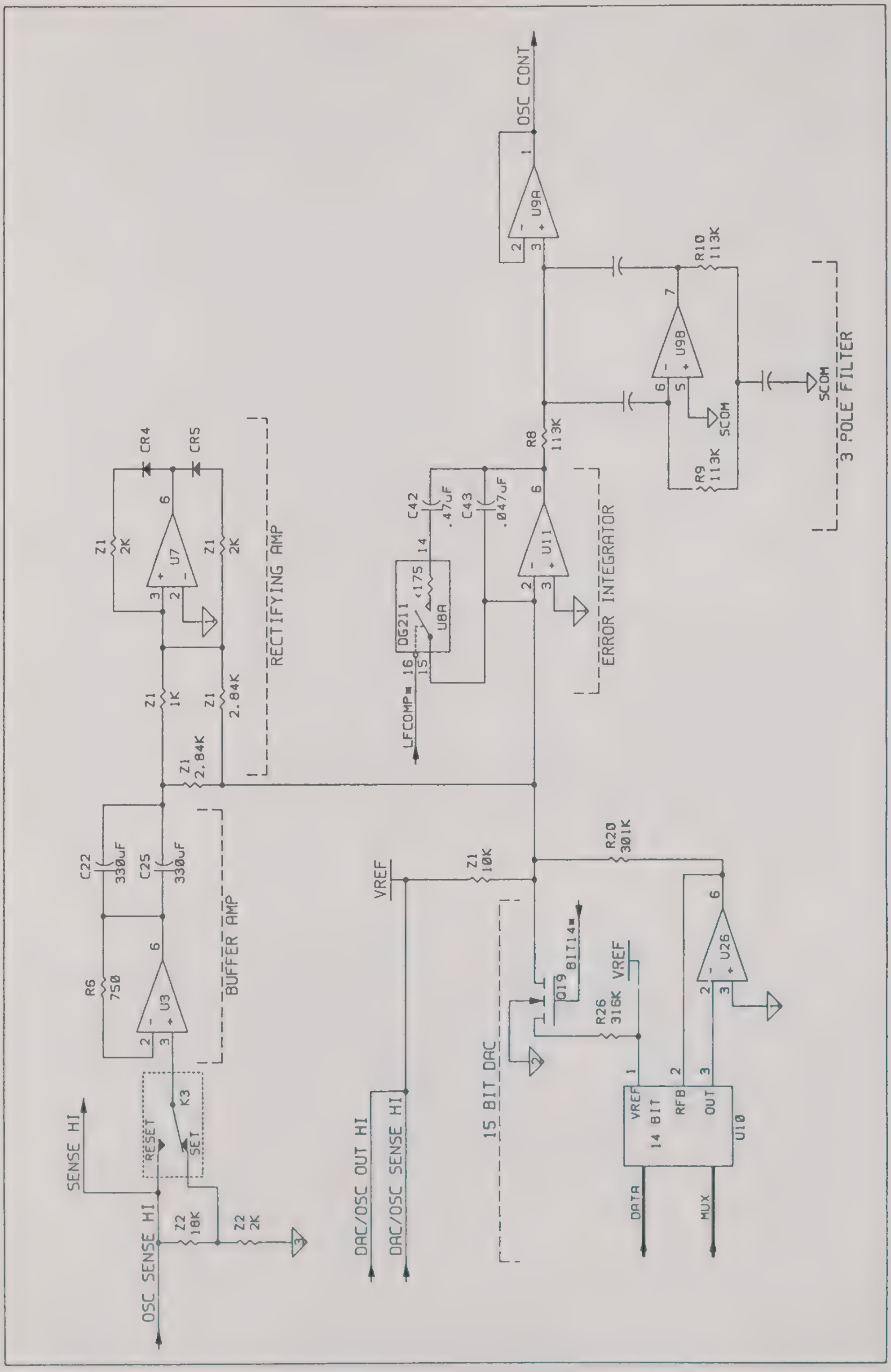

OSC CONT
U9A
1
2
3
R10
113K
7
U9B
6
5
SCOM
SCOM
R9
113K
R8
113K
3 POLE FILTER
C42
.47uF
C43
.047uF
6
U11
2
3
14
<175
DG211
U8A
16
15
LFCOMP=
ERROR INTEGRATOR
CR4
CR5
Z1
2K
U7
6
3
2
Z1
2K
Z1
1K
Z1
2.84K
Z1
2.84K
RECTIFYING AMP
C22
330uF
C25
330uF
R6
750
U3
6
2
3
BUFFER AMP
K3
RESET
SET
SENSE HI
OSC SENSE HI
Z2
10K
Z2
2K
3
VREF
Z1
10K
DAC/OSC OUT HI
DAC/OSC SENSE HI
R20
301K
15 BIT DAC
Q19
BIT14=
R26
316K
VREF
2
U26
6
2
3
1
2
3
VREF
RFB
OUT
14 BIT
U10
DATA
MUX

Figure 2-18. Oscillator Control Analog Control Loop

2-126. ANALOG AMPLITUDE CONTROL LOOP

This loop is comprised of the averaging converter, error integrator, three-pole filter, and the agc amplifier on the Oscillator Output assembly (A13). It stabilizes the 5700A output voltage in the presence of load changes. This loop by itself is very stable but does not have the conversion accuracy or gain flatness necessary to meet the precise amplitude specifications of the 5700A. Thus this circuit is used only to provide quick load regulation recovery and short term output stability.

2-127. AC/DC THERMAL TRANSFER CIRCUIT

Refer to Figure 2-19 for the following discussion. The ac/dc thermal transfer circuit achieves basic mid-band amplitude accuracy. This is done by first applying the reference voltage (VREF) to the thermal rms sensor (U14) and measuring the output. Next, the ac voltage is applied to the thermal rms sensor and the dc output is compared to the previous reading. The sensor detects the difference between the ac and dc input voltages to within a few ppm.

If there is an ac/dc difference, the dc reference current applied to the error integrator of the analog control loop is adjusted via the 15-bit dac until the ac/dc difference is zero. The ac/dc thermal transfer circuit that performs this function is further described in detail. It contains the the dc sense buffer, ac sense buffer, ac/dc thermal sensor, and the square-root amplifier and 15-bit dac as outlined on the schematic.

As previously mentioned, the input to the thermal rms sensor is either the dc reference voltage (VREF) buffered by the dc sense buffer or the ac voltage (SENSE HI) buffered by the ac sense buffer.

The dc sense buffer circuit uses op amp U30 as a buffer amplifier. Enhanced-mode FET Q10 provides feedback for U30 while FETs Q8 and Q9 are off. During a dc transfer, control line AC*/DC and comparator U21C turn on the FETs, applying the output of the dc sense buffer to the input of thermal rms sensor U14.

The ac sense buffer circuit contains op amps U12A, U12B, U13; FETs Q6, Q7, Q11, Q12; relay K4, and associated components. Relay K4 selects the input resistance to amplifier U13, which has a nominal inverting gain of 0.316 in the 22V range and 3.16 in the 2.2V range.

During operation in the 22V range, relay K4 is set, feeding the input, SENSE HI, through the 20 kilohm resistor in Z3. When operating in the 2.2V range, the 2.22 kilohm and 20.0 kilohm resistors in Z3 are put in parallel by K4 in the reset position, reducing the input resistance to 2 kilohm.

During an ac transfer, control line AC*/DC and comparator U21D turn on FET Q12 so the output of amplifier U13 is applied to the input of thermal rms sensor U14. At this time, FET Q11 is turned off and the feedback path for U13 is through the 6.32 kilohm resistor in Z3.

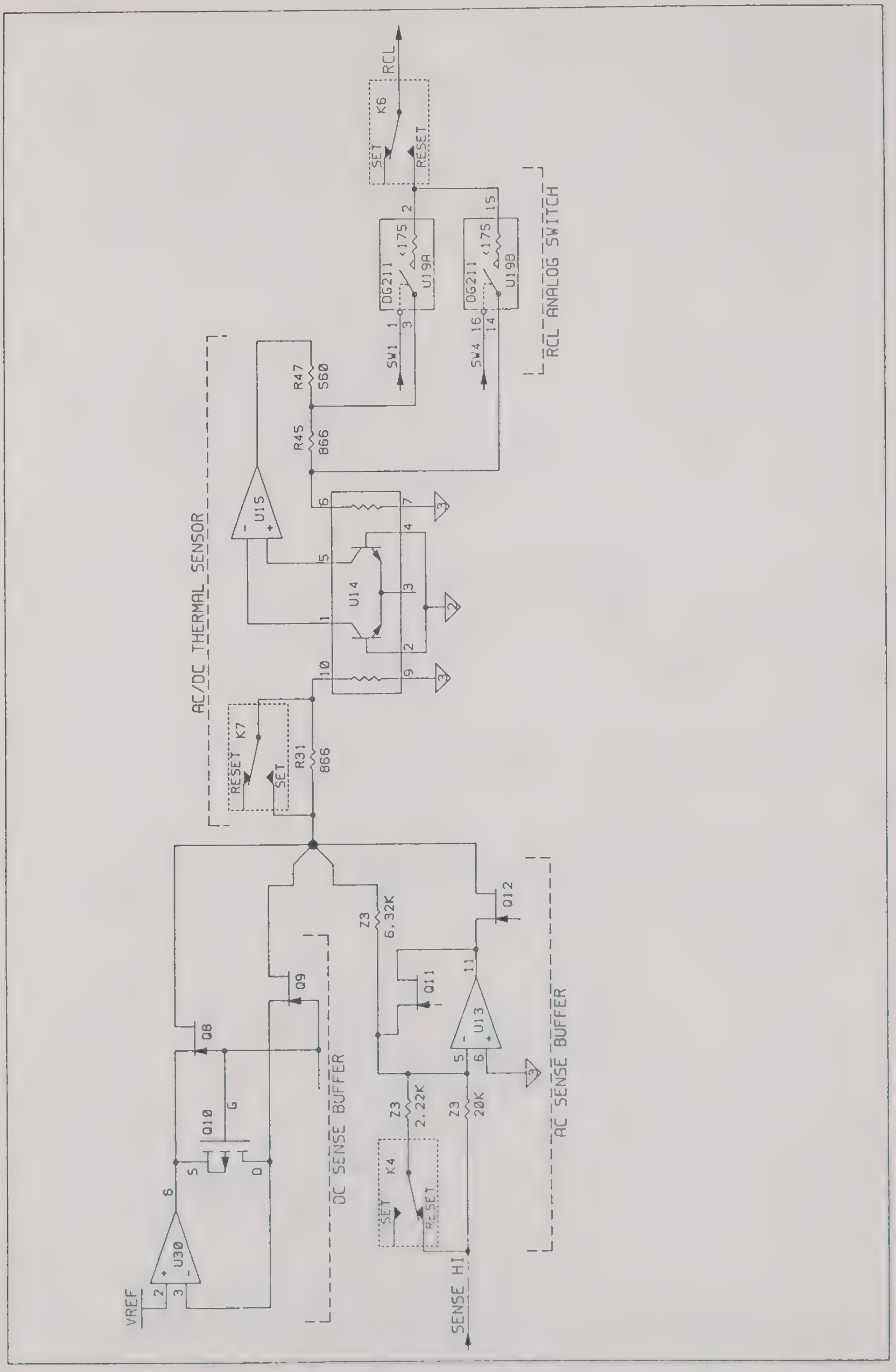

RCL
K6
SET
RESET
2
15
DG211
<175
U19A
U19B
1
3
16
14
SW1
SW4
RCL ANALOG SWITCH
R47
560
R45
866
U15
AC/DC THERMAL SENSOR
U14
6
7
4
5
3
1
2
10
9
K7
RESET
SET
R31
866
Q12
Z3
6.32K
Q9
Q11
11
U13
5
6
Q8
Q10
G
S
D
6
U30
VREF
2
3
DC SENSE BUFFER
AC SENSE BUFFER
Z3
2.22K
Z3
20K
K4
SET
RESET
SENSE HI

Figure 2-19. AC/DC Thermal Transfer Circuit

During a dc transfer, Q12 is off and comparator U21B turns on FET Q11, providing the feedback path for U13. Op amps U12A and U12B provide low offset and increase the gain. Control line HFCOMP and comparator U22C turn on FETs Q6 and Q7 during operation in the 1 MHz range.

The output of either the dc sense buffer or the ac sense buffer becomes the input of thermal rms sensor U14. During operation from 0.22V to 0.7V in the 2.2V range, or 2.2V to 7V in the 22V range, relay K7 is set, directly connecting the input signal to the sensor. The input to the thermal sensor is through R31 by K7 in the reset position during operation from 0.7V to 2.2V in the 2.2V range, or 7V to 22V in the 22V range.

Comparator U21A provides protection for thermal rms sensor U14. If the junction temperature of the sensor goes above 200 oC, the voltage at pin 3 increases, driving the output of U21A negative. This turns off the FETs controlling the output of the dc sense buffer and ac sense buffer, removing the input to the thermal sensor.

The ac/dc thermal sensor and square-root amplifier, as outlined on the schematic, contain the thermal sensor U14, op amp U15 and transistor array U17. The dc voltage from the thermal sensor is connected to U15B configured as an integrator. Comparator U22B is used to control FETs Q18 and Q20. These FETs are turned on, adding C84 and C62 to the integrator, by control lines LFCOMP* and AC*/DC both at logic low. The output of integrator U15B is used by the square-root amplifier contained in U15A, U15C and U17. This circuit keeps the settling time of the sensor constant when its input is varied between full and 1/3 scale. The output of the sensor is connected to the RCL line by relay K6 and CMOS analog switch U19A and U19B. During operation from 0.22V to 0.7V in the 2.2V range, or 2.2V to 7V in the 22V range, sensor output is connected to the RCL line through buffer U31, U19B, and K6 in the set position. During operation from 0.7V to 2.2V in the 2.2V range, or 7V to 22V in the 22V range, sensor output is connected to the RCL line through U19A and K6. Control lines SW1 and SW4 control U19A and U19B respectively. The RCL line is routed to the DAC assembly (A11) where its amplitude is measured by the adc circuit.

To do an ac/dc transfer, the dc sense buffer is connected to the thermal sensor and the sensor output is connected to the +input of the DAC's adc circuit. The -input of the adc circuit is connected to the DAC output (VREF), and the difference between the two is measured and stored in memory. Next, the output of the ac sense buffer is connected to the sensor and the sensor output is connected to the +input of the DAC's adc circuit. The difference is measured and compared to the previous reading. The difference between these two readings is the difference in rms value of the ac and dc input voltages. If there is an ac/dc difference, the dc reference current applied to the error integrator of the analog control loop is adjusted via the 15-bit dac until the ac/dc difference is zero.

The 15-bit dac contains an AD7534 dac IC (U10), FET Q19 and op amp U26. The first 14 bits (bits 0-13) are generated by the dac IC U10, and bit 14 is generated by Q19, R26, and control line BIT14. Control busses DATA and MUX from the digital control circuit select the data and address for U10. The output is inverted by U26 to create 14 BIT DAC OUT, which is applied to the summing node of the error integrator by R20. This output is also monitored by the diagnostic circuit.

2-128. OSCILLATOR CALIBRATION

Calibration consists of determining the offset and gain errors of the ac/dc switching circuitry. Errors are measured at dc using the calibrator DAC and the 6.5V reference as the primary sources of accuracy. This characterization is valid for frequencies up to 1 kHz. Above 1 kHz, ac/ac characterization is used to insure the output accuracy.

The DAC assembly (A11) is set to 0V with its output connected to the ac sense buffer (via SENSE HI) by relay K1 in the set position. The output of the ac sense buffer is connected to the RCL line by K6 in the set position and by control line GCAL and comparator U22A turning on Q13. The 0V input is stored as Vin1. The output measured by the adc circuit on the DAC assembly is stored as Vout1.

Relay K1 ties 6.5V reference BRF6 and BSRF6 to VREF, where it is measured at the output of the thermal sensor in the same manner as a dc transfer. This measured output is stored in memory.

The DAC output is set to 20V or 2V and is measured at the output of the thermal sensor in the same manner as an ac transfer. The DAC is then adjusted until this measured output is the same as stored in the previous step. The DAC setting is stored as Vin2 and the 6.5V reference is Vout2. The gain can now be calculated with the formula: (Vout2 - Vout1)/(Vin2 - Vin1).

2-129. AC/DC FREQUENCY RESPONSE CHARACTERIZATION

Characterization is accomplished by first performing an ac/dc transfer with the Oscillator Output set to a low frequency. The ac/ac thermal sensor circuit, containing the thermal sensor U16 and op amp U15D, characterizes the frequency response of the main ac/dc thermal sensor. This sensor has no active circuitry at its input, and all switching is done by relays to insure a flat frequency response.

In the 20V range, the Oscillator Output is switched through R34 to the ac/ac thermal sensor via SENSE HI, K5, and K9 in the set position. In the 2.2V range, R34 is bypassed by K9 in the reset position. The output of this sensor is routed to the RCL line via U19C and K6. A reading is taken and stored in memory as ACref.

The output frequency of the Oscillator Output is changed to the first cal point and the 15-bit dac is adjusted until the reading from this ac/ac thermal sensor is the same as ACref.

The RCL line is then switched back to the ac/dc thermal sensor. A reading is taken stored in memory as ACdif. The gain constant is calculated using the formula (ACdif + Vdac)/Vdac, where Vdac is the DAC assembly (A11) voltage.

This ac/ac transfer function is also performed for the 220V range and the 1100V range. These ranges are generated by the Power Amplifier assembly (A16) and the High Voltage/High Current assemblies (A14 and A15). High voltage ac signals are attenuated and connected to AC CAL, where they are connected to the sensor though relay K5 in the reset position. In the 220V range, the output of the sensor is divided by Z4 and connected to the RCL line by U19D and K6.

Protection for this thermal sensor is provided by comparator U22D, FET Q14, zener diodes VR5, VR6, resistor network Z10, and diodes CR12 and CR13. During normal operation, U22D keeps Q14 off. If the junction temperature of the sensor goes above 200 oC, the voltage at pin 3 increases, driving the output of U22D positive. This turns on Q14, shunting the input of the sensor to common through CR12 and CR13.

2-130. Oscillator Output Assembly (A13)

The Oscillator Output assembly is controlled by the Oscillator Control assembly. Refer to Figure 2-20 and the schematic diagram for the following discussion.

The Oscillator Output assembly generates an ac sine wave from 0.22V to 22V with a frequency range of 10 Hz to 1.1999 MHz. There are five frequency ranges (100 Hz, 1 kHz, 10 kHz, 100 kHz and 1 MHz) and two voltage ranges (2.2V and 22V). The output signal is either routed to the OUTPUT binding posts, or it is used internally by the Power Amplifier, High Voltage, Wideband AC Module (Option -03), Current, or Switch Matrix assemblies, or it is routed to an Auxiliary Amplifier for generation of voltages and/or functions outside this range. Output sensing is available for all voltage ranges above 220 mV at the SENSE binding posts.

The Oscillator Output assembly contains a fixed-amplitude quadrature RC oscillator, a 0.22-22V digital/linear gain-controlled amplifier, a fixed-amplitude variable phase-shifting network, phase-locked loop control circuitry for phase locking to an external signal or the PLOCK signal from the Current/Hi-Res assembly (A7), and digital control circuitry.

All power supplies used by this assembly except the -12S supply are generated by the Guard Crossing/Regulator assembly (A17). The -12S supply is generated on this assembly by a three-terminal -12V regulator (U2) using the -17S supply as its input.

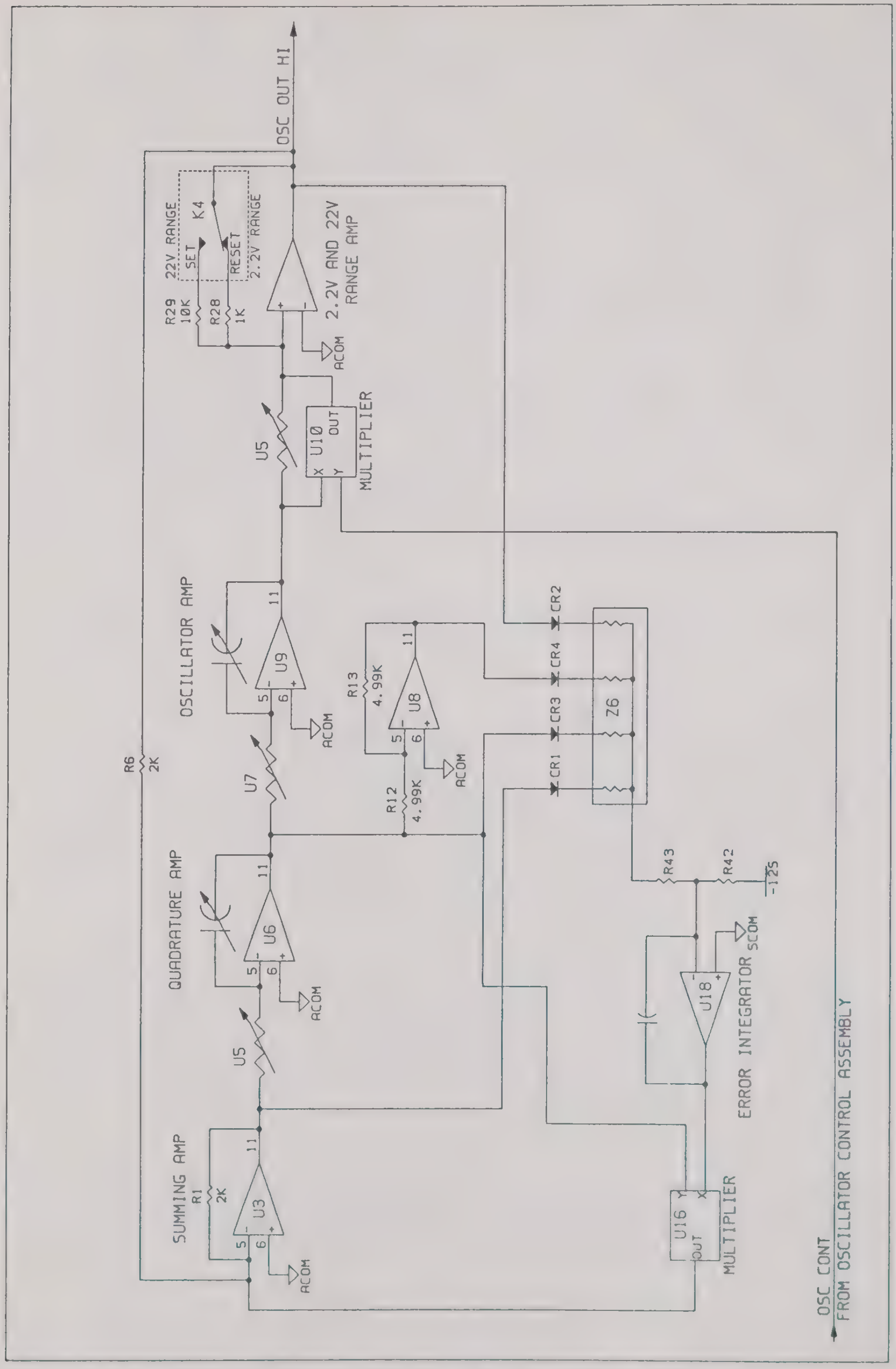

OSC OUT HI
22V RANGE
SET
K4
RESET
2.2V RANGE
R29
10K
R28
1K
2.2V AND 22V
RANGE AMP
ACOM
U5
U10
X
Y
OUT
MULTIPLIER
OSCILLATOR AMP
U9
11
5
6
ACOM
R13
4.99K
U8
11
5
6
ACOM
R12
4.99K
CR2
CR4
CR3
CR1
Z6
R6
2K
U7
QUADRATURE AMP
U6
11
5
6
ACOM
U5
R43
R42
-12S
SCOM
U18
ERROR INTEGRATOR
SUMMING AMP
R1
2K
U3
11
5
6
ACOM
U16
Y
X
OUT
MULTIPLIER
OSC CONT
FROM OSCILLATOR CONTROL ASSEMBLY

Figure 2-20. Quadrature RC Oscillator Circuit

2-131. OSCILLATOR OUTPUT DIGITAL CONTROL

The digital control circuit consists of an 82C55 Programmable Peripheral Interface (U26), a 5801 Latching Relay Driver (U24), and three HC374 Octal D-Type Flip Flops (U12, U32, U33). The Programmable Peripheral Interface (U26) is under software control via the guarded digital bus and has three ports which generate 24 outputs. Port A (PA0-PA7) is a common input bus for U24, U12, U32, U33, and U28. Latching relay driver U24 controls the four latching relays K1-K4. Relays K1-K3 select the frequency range and K4 selects the voltage range. This IC is strobed by PC3 of port C and enabled by PC6 of port C. To insure that the relays are latched properly the driver must be enabled for 10 ms.

Latch U32 is clocked by PC0 and generates the data bus FREQ DATA for controlling 8-bit resolution hybrid resistive dacs U5 and U7. Latch U12 is clocked by PC1 and generates the data bus AMPL DATA for controlling U11, which is identical to U5 and U7. Latch U33 is clocked by PC2 and generates control bus PHASE, which controls multiplexer U27 in the phase shifter circuit and control bus MUX, which controls the SDL multiplexer U25 in the diagnostic circuit. This diagnostic circuit monitors the ±44S supplies, ±15S supplies, INTEGRATOR OUT, LOOP FILTER OUT, and AMP1 which is from U30, the A13A1 assembly. These voltages are divided by Z2 and Z3 and connected to the SDL line by multiplexer U25, where they are measured by the adc circuit on the DAC assembly (A11).

PB0-PB2 of port B generates control bus PLOCK RNG which is used in the phase-locked loop circuit. PB4 is control line 0/180 to control FET Q7 via comparator U31B in the phase-locked loop circuit. PB6 is control line LFCOMP* to control FET Q6 via comparator U20A in the integrator circuit. PB7 is control line HFCOMP*, which is routed to the Oscillator Control assembly (A12). PC4 and PC5 are control lines DAC STRB and DAC SEL respectively, which control the dual 8-bit dac U28 in the phase shifter circuit. PC7 is control line INH to enable the multiplexer U25 in the diagnostic circuit.

2-132. QUADRATURE RC OSCILLATOR

The quadrature oscillator is a double integrator type. It contains two op amp RC integrators and a unity-gain inverting summing amplifier. The integrators are identical and use relay-switched feedback capacitors to select five frequency ranges. An 8-bit resolution resistive dac selects frequency within a range.

The summing amplifier uses op amp U3 to provide a 180° phase shift in the oscillator loop at unity gain. Its exact phase shift and gain are adjusted by the amplitude control and phase-locked loop circuits to satisfy the conditions required for amplitude stable oscillation: exactly 360° loop-phase and unity gain. This amplitude control circuit uses an integrator and multiplier as outlined on page 1 of the schematic. These two circuits are described in detail later.

The two op amp RC integrators are the quadrature amplifier and the oscillator amplifier. Their purpose is to provide -90° each to the loop phase with an amplitude slope of -20dB/decade. The quadrature amplifier contains op amp U6, 8-bit resolution resistive dac U5, and relays K1B, K2B, and K3B. The relays select feedback capacitors C25, C24, C22, and C21 for frequency ranges 100 Hz, 1 kHz, 10 kHz and 100 kHz respectively. For the 1 MHz range, all the above capacitors are removed from the loop, and the only feedback path is C19. The input resistor is the 8-bit resolution resistive dac U5 which is under the control of the FREQ DATA bus from the digital control circuit. Its equivalent resistance is R = (256/X)*2 kilohm, where X is the digital code on the FREQ DATA bus. The oscillator amplifier contains op amp U9 and performs the same function as the quadrature amplifier. Its input resistance is controlled by resistive dac U7. Relays K1A, K2A, and K3A select the feedback capacitance. Since their phase shift is constant with frequency and the sum of the phase shifts around the loop is zero for all frequencies, we have satisfied one half of the requirement for oscillation. In summing the gain in dB around the loop it is apparent that unity gain occurs at only one frequency. This happens when the closed loop gains of the integrators are unity. This corresponds to F = 1/(2 x PI x R x C), which is the frequency of oscillation.

2-133. OSCILLATOR AMPLITUDE CONTROL

Since small excess phase shifts exist in all three amplifiers and the gain of the summing amplifier cannot be made exactly one, it is impossible to generate an amplitude-stable sinusoidal waveform from just these elements. A control circuit consisting of an error integrator and a linear four-quadrant multiplier is used to sense the output amplitude and stabilize it by adjusting the loop phase shift slightly.

To do this, a fourth oscillator signal is generated using U8 to invert the output of the quadrature amplifier. The Oscillator now has four equal-amplitude signals all spaced 90° apart. These signals are rectified and summed by CR1-CR4 and Z6 in such a way that a dc representation of the output amplitude is created. This dc signal is summed with a -12V reference voltage by the error integrator circuit which contains op amp U18. If there is a magnitude difference between the rectified dc and the reference, the output of the error integrator changes. This in turn controls the amplitude of the oscillation. This is done via multiplier U16, a linear-variable resistance with a value inversely proportional to the error integrator output voltage.

If the control input (x input) to the multiplier is zero, the equivalent resistance from the signal input (y input) is infinite. If the control input is negative, the equivalent resistance is negative. The Y signal input of the multiplier is the quadrature amplifier output. Any nonzero control voltage changes the phase shift of the loop by injecting a small amount of out-of-phase current into the summing amplifier. This negative feedback is used to stabilize the amplitude of the oscillating signal by allowing one output amplitude only to satisfy the required conditions of oscillation. During operation in the 100 Hz range, control line LFCOMP* and comparator U20A turn off FET Q6.

2-134. PHASE-LOCKED LOOP

The Oscillator Output assembly is phase locked to an external frequency to increase frequency accuracy. This external frequency comes from the High-Resolution Oscillator on the Current/Hi-Res assembly (A7) or from an external source connected to the rear-panel PHASE LOCK IN jack.

The frequency capture range is approximately ±5% of the nominal output frequency range. This is done by comparing the oscillator output frequency SUMMING AMP OUT or INT OSC OUT against the external frequency source P LOCK HI with a phase detector. The P LOCK HI signal is referenced to P LOCK LO. The phase-locked loop circuit locks SUMMING AMP OUT to the external frequency when the calibrator is in the 22V range or less. The phase-locked loop circuit locks INT OSC OUT, which is 180° out of phase from SUMMING AMP OUT, during calibrator operation at higher voltages. This occurs because the output from the Power Amplifier and High Voltage assemblies (which are used to generate the higher voltage ranges) are 180° out of phase from the Oscillator output. When the 5700A is in the higher voltage ranges, control line 0/180 and op amp U31B turn on Q7, which selects INT OSC OUT to the Zero Crossing Detector.

Since the phase detector circuit requires digital inputs, both signals are converted to square waves using U23A/B as dual zero crossing detectors. Square waves from the zero crossing detector circuitry are fed to the phase detector circuit containing U22A/B and U21. The phase detector circuit looks for the falling edge of both signals. The first signal that makes a positive to negative transition causes the phase detector to turn on either the positive (CR5, CR6) or the negative (CR7, CR8) charge pump, depending on which signal is first. The Charge Pump is turned off when the other signal makes its transition. Thus the signal with the highest frequency has its respective charge pump pulsed on and off while the other charge pump remains off.

The accumulated charge is integrated by the loop filter circuit, which contains op amp U31A, multiplexer U17, Z1, and C75-C84. Multiplexer U17 is controlled by the PLOCK RNG control bus from the digital control circuit. This multiplexer changes the cross-over point of the loop filter by selecting C83 and C84 for feedback in the 100 Hz range. Capacitors C81 and C82 are used for the 1 kHz range, C79 and C80 for the 10 kHz range, C77 and C78 for the 100 kHz range, and C75 and C76 for the 1 MHz range.

The output of the loop filter controls two multipliers (U15 and U19) similarly to the amplitude control section. The only difference is that the signal input is derived from the in-phase signal. In the case of U15, the input signal is QUADRATURE AMP OUT, which changes the unity-gain frequency of the oscillator amplifier. In the case of U19, the input signal is SUMMING AMP OUT, which changes the unity-gain frequency of the quadrature amplifier. The new frequency of oscillation is the new unity gain frequency of the integrators. Under phase-locked conditions, neither charge pump is allowed to turn on because neither signal reaches the phase detector first.

2-135. 2.2V AND 22V RANGE OUTPUT AMPLIFIER

The 2.2V and 22V range output amplifier is an inverting wide-band low-distortion amplifier that provides output signal OSC OUT HI at the OUTPUT binding posts in the 2.2V and 22V ranges. OSC OUT HI is used by the Power Amplifier and High Voltage assemblies to generate the higher voltage ranges.

This amplifier uses a surface-mount gain block (U30) called the Oscillator Wideband SMD PCA (A13A1) and a complementary Darlington emitter follower bootstrapped output stage. Relay K4 selects feedback resistor R28 for the 2.2V range and R29 for the 22V range. It also changes the open-loop frequency response for each voltage range. Its gain within a range is controlled by the gain control multiplier circuit and the dac gain control circuit.

The dac gain control circuit contains the same 8-bit resolution resistive dac (U11) as in the oscillator with the exception that it is controlled by the AMPL DATA control bus from the digital control circuit. This resistive DAC provides the coarse gain control. The gain control multiplier circuit contains a multiplier U10, which provides a small linear control range of several dac counts. The control input to the multiplier, OSC CONT, comes from the Oscillator Control assembly (A12). This allows the output amplitude to be adjusted as required by the Oscillator Control Assembly. The theory of operation for the rest of the output stage is described following the A13A1 theory.

2-136. Oscillator Wideband SMD Assembly (A13A1)

The A13A1 is a surface-mount assembly on the Oscillator Output assembly (A13) that provides the 22V output signals of the 5700A. It is essentially an operational amplifier built using discrete components to provide the necessary speed, power output and breakdown voltage required for such a high output signal.

The input stage is a differential pair (Q2 and Q3) that is buffered by a source follower Q1. The transconductance is determined by R3, R4 and R26. The inherent input offset voltage of this stage is corrected by U1 and U2 and related components. The output of Q3 is level-shifted by VR5-VR7 before being applied to the mid stage. Transistor Q4 serves as a high-impedance current sink used to bias the input stage to approximately 10 mA. Potentiometer R30 adjusts the dc zero at the output of U2.

The mid stage is a common-emitter, Miller-compensated gain stage (Q5) that drives a common-base level shifter (Q13) on the Oscillator Output assembly. This stage is current limit protected by R12 and Q4. The dominant pole is set with the Miller capacitor C5 and the input stage transconductance. The mid stage is biased to 10 mA by Q6 and related components.

The output stage of the amplifier is a bootstrapped complementary Darlington pair. The only parts of the output stage on this A13A1 assembly are the input transistors Q7 and Q8. The output bias current is set by R17 and CR4-CR5 to be approximately 40 mA. This keeps the output stage class A for all normal output conditions.

2-137. OUTPUT STAGE

The output stage circuit is a complementary Darlington emitter follower bootstrapped buffer amplifier. The input transistors are Q7 and Q8 on the A13A1 assembly. These transistors drive the output transistors Q8 and Q14 respectively. Transistors Q10 and Q11 in the positive side and Q16 and Q17 in the negative side are parallel transistors bootstrapped by VR3 and VR4. Current sources CR13, CR14, CR17, CR18, CR15, CR16, CR11, and CR20 provide the bias current for their respective bootstrapped transistors. Current limiting for the positive side is provided by Q9 and R91. During an overcurrent condition, the voltage drop across R91 turns on Q9, which draws current away from the base of Q11. Current limiting is done in the same manner for the negative side with Q15 and R99.

Switch S1 can be switched to pull the input of the A13A1 output stage low for troubleshooting the output stage. Refer to the Oscillator Output troubleshooting section for more information.

2-138. PHASE SHIFTER

The phase shifter circuit provides a fixed amplitude variable phase auxiliary signal at the rear panel of the calibrator. This signal is the same frequency as the output, but can be phase shifted over a 360° range. The four phases (each 90° apart) for the oscillator circuit are divided by Z4 and Z5. These signals are connected to the dual four-channel multiplexer (U27), which is under the control of the PHASE control bus from the digital control circuit. This multiplexer selects any two adjacent oscillator phases (e.g. 0° and 90°) that are connected to the input of a dual monolithic DAC U28. These signals are then scaled by the dac (U28), also under the control of the digital control circuit. The two outputs of this dac are summed by op amp U29. Using this method, the output of U29 is a phase shifted signal between 0 and 360°, where the scaling of the signals controls the phase shift within a 90° range.

2-139. Power Amplifier Assembly (A16)

The Power Amplifier assembly outputs dc voltages from ±22V to ± 219.99999V and ac voltages from 22V to 219.99999V rms. The frequency limit for 220V ac output is 100 kHz. Output voltage limits are derated at frequencies above 100 kHz. At 1 MHz, the maximum output voltage is 22V rms. The Power Amplifier drives the High Voltage assemblies (A14, A15) in all high voltage and high current functions.

This assembly also contains calibration circuitry that enables the internal calibration system to determine exact Power Amplifier ac and dc gain, offsets and frequency response.

The main sections of this assembly are the input stage, mid stage, output stage, sense-current cancellation circuit, the dc and ac gain calibration circuits, and the Power Amplifier Digital Control SIP assembly (A16A1), which is mounted on the Power Amplifier assembly.

2-140. POWER AMPLIFIER DIGITAL CONTROL SIP ASSEMBLY (A16A1)

Digital control for the Power Amplifier assembly is contained on the SIP assembly (A16A1) mounted at the bottom of the Power Amplifier. This assembly configures the Power Amplifier assembly for its various modes of operation. (Also see "±PA Supplies Digital Control" in the Power Amplifier Supply theory of operation.)

The heart of the Digital Control assembly is an 82C55 Programmable Peripheral Interface IC (U11) operating under software control via the guarded digital bus. This IC has three ports that generate 24 outputs. These outputs control two 5801 relay driver ICs (U10, U12), two LM339 Comparators (U13, U15) and an analog multiplexer (U14) used for diagnostics.

Relay driver U10 generates eight control lines (LC0*-LC7*) that control four latching relays (K1-K4). Relay driver U12 generates eight control lines (C0*-C7*) for non-latching relays K10-K17. C0* also controls FETs Q57 and Q58. Port A (PA0-PA7) from U11 provides an input bus common to relay drivers U10 and U12. Each driver has separate strobe and enable lines from port C of U11. Driver U10 is strobed by PC7 and enabled by PC5. Driver U12 is strobed by PC4 and enabled by PC6. When a STROBE line is selected, data on the bus (PA0-PA7) is strobed into the respective driver chip. When an ENABLE is selected, this strobed data appears at the output, thereby energizing the appropriate relays. Latching relays only need to be energized for 10 ms; non-latching relays need to be energized continuously.

As an example, the following steps are taken to set up latching relays controlled by relay driver U10.

1. Write the proper data for these relays to port A of the 82C55 (U11).
2. Write hex A to PC4-PC7 to strobe the data into U10.
3. Write hex 0 to PC4-PC7, wait 10 ms and write hex 2 to PC4-PC7. This takes U10's output out of tri-state and energizes the proper relay coils for 10 ms. Since PC4 and PC6 are always low, U12 is undisturbed.

Two LM339 quad comparators (U13 and U15) get their data from port B of U11 (PB0-PB7) and generate control lines SW0-SW7. SW0-SW2 are inputs to decoder U9, which generates eight additional control lines (CONT0*-CONT7*) for controlling FETs and solid state switches. Control line SW3 controls FETs Q50 and Q51. Control lines SW4-SW7 are routed through the Motherboard to the Filter/Power Amplifier Supply assembly (A18) to control the +PA and -PA supplies.

The diagnostic circuit enables the 5700A to monitor eight diagnostic (MUX) signals on the Power Amplifier assembly. A 4051 analog multiplexer (U14) is controlled by PC0-PC3 from U11. This multiplexer selects of the eight MUX signals to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11). Resistor network Z2 and various resistors and zener diodes on the Power Amplifier assembly divide these MUX signals down to a proper level for measurement by the adc circuit. The eight monitored points are:

o MUX0	Output of U7; indicates the status of the amplifier loop
o MUX1	+PA Supply
o MUX2	-PA Supply
o MUX3	Power Amplifier output
o MUX4	Indicates the temperature of the Power Amplifier assembly
o MUX5	Power Amplifier dc input
o MUX7	Diagnoses the state of the hybrid heater-control circuit

2-141. PA COMMON CIRCUITRY

Common circuitry consists of the +PA and -PA supplies, input stage, mid stage, and the output stage. These four circuits are described under the next four headings.

Power Amplifier input node, gain, and feedback are different for dc and ac operation. Power Amplifier gain is -20 in the dc function, determined by the ratio of resistor network bonded to the HR8 assembly (500 kilohm/25 kilohm). Gain in the ac function is -10, which is determined by the ratio resistors [(R11 + R12 + R13)/R17]. This is described in more detail under "DC Voltage Function" and "AC Voltage Function".

2-142. +PA AND -PA SUPPLIES

The ±PA supplies are high voltage supplies generated by the Filter/PA Supply assembly (A18). These supplies can be controlled by the Digital Control SIP assembly (A16A1) and are switched between the two modes shown in Table 2-13.

- o ±185V
- o ±365V

Theory of operation for the Filter/PA Supply assembly (A18) describes how these voltages are generated and selected.

Table 2-13. +PA and -PA Supply Settings at Different Outputs

CALIBRATOR OUTPUT	+PA	-PA
Less than 22V ac or dc	+185V	-185V
22 to 110V dc	+185V	-185V
110 to 220V dc	+365V	-185V
-220 to -110V dc	+185V	-365V
22 to 101V ac (freq < 120 kHz)	+185V	-185V
22 to 85V ac (freq > 120 kHz)	+185V	-185V
Other voltages	+365V	-365V
220 to 550V dc or ac	+185V	-185V
550 to 1100V dc or ac	+365V	-365V
220 mA to 2.2A	+365V	-365V

2-143. PA INPUT STAGE

The input stage consists of a heater-controlled hybrid HR8, op amp U7, transistor Q6, and JFET Q2. The HR8 assembly consists of an op amp mounted on a heated-substrate hybrid, with a resistor network bonded to it. Hybrid HR8 provides the input stage with excellent dc characteristics of low offset, noise and drift. The hybrid heater-control circuit (on page 3 of the schematic) adjusts the base voltage of Q38 to deliver the correct current to the heater resistor. This maintains the hybrid assembly at a constant temperature in spite of environmental temperature variations. Transistor Q35 protects the hybrid in case Q38 fails. Input of the hybrid op amp is protected by CR13 and CR14. Output of the hybrid op amp is connected to the input of a faster op amp (U7), which provides additional dc gain and a higher slew rate. JFET Q2 and transistor Q6 combined with these two op amps complete the input stage. Q2 is a very low-bias-current, high-frequency JFET.

In mid to high-frequency operation, Q2 is effectively the only path for the input stage signal. HR8 and the U7 op amps are bypassed at these frequencies by R89, C42, R24, and C12. As a result, the base of Q6 is at ac ground. In dc to mid-frequency operation, the gate of Q2 is at ground potential. At any frequency, the potential difference between the gate of Q2 and the base of Q6 results in a current through Q6 as determined by the network consisting of R22, R145, and L11 and by the transconductance of Q2 and Q6. The input stage is called a transconductance stage because an input voltage results in a current output at the collector of Q6.

This current output is coupled to the mid stage (Q12, Q14, and Q16) by Q8, Q9, Q13 and C15, where it results in a voltage across the base-emitter of Q16 (the input of the mid stage). Current source Q9 determines bias current in Q2 and Q6. Variations of Q6 output current become voltage variations at the base of Q16. This transfer is through Q8 and Q13 at dc and low frequencies, and through C15 at high frequencies.

The input stage operates with low voltage supplies (±17V) whereas Q16 of the mid stage is connected to the -PA supply, which can be as high as -365V. This potential difference is dropped across level shifter Q13.

2-144. PA MID STAGE

The mid stage (Q12, Q14, and Q16), biased by the 8 mA current source (CR53, Q31, Q32 and R87 on page 2 of the schematic), is a voltage amplifier providing additional gain. The base of transistor Q16 is the input to the mid stage. MOSFETs Q12 and Q14 are biased by R41 and R53 respectively. Components CR21, CR23, and VR22 protect Q12 from excessive source-to-gate voltage, and R112 prevents Q12 from oscillating. Components CR25, CR29, VR28, and R113 perform the same function for Q14. A signal at the base of Q16 appears amplified at the drain of Q12. Total impedance from the drain of Q12 to ground, divided by R58, determines gain at dc and low frequencies. At high frequencies, the effective drain to ground impedance is R53. Relay K12A parallels C18 and C57 during dc operation for a lower bandwidth. Capacitors C18 and C57 provide the Miller capacitance for the amplifier.

Transconductance gain of the input stage and the Miller capacitance determine Power Amplifier frequency response at high frequencies. All the voltage gain of the Power Amplifier comes from the input and mid stages.

2-145. PA OUTPUT STAGE

The Output Stage is an emitter follower that provides current gain but no voltage gain. It is needed because the mid stage cannot drive the rated load by itself.

Voltage across R74 and R35 determines the bias current through the output stage. This voltage equals the voltage across Q7, minus the value (4 x Vbe) (for each transistor Q4, Q5, Q10, and Q11). Transistor Q7 is configured as a Vbe multiplier, the voltage across which (and thus the output stage bias current) is the value (1 + (R23+R26)/R32). The output bias current is 50 mA.

NMOSFETs Q1, Q3, and transistor Q5 source current, while PMOSFETs Q15, Q17, and transistor Q10 sink current from the load. This output stage can drive up to 50 mA of load current as determined by the current limit circuit on ±PA supplies on the Filter/PA Supply assembly (A18).

Zener diodes VR15 and VR18 bootstrap NMOSFETs Q3 and Q15 respectively, and provide the power supplies SC+ and SC- to op amp U1 in the sense current cancellation circuit. Two stacked NMOSFETs (Q1, Q3) on the top end (+PA side), and two stacked PMOSFETs (Q15, Q17) on the bottom end (-PA side) withstand the high voltage drops between ±PA supplies and output. NMOSFETs Q1 and Q3 are biased by R15 and R19 respectively. PMOSFETs Q15 and Q17 are biased by R52 and R57 respectively. Components CR5, CR7 and VR6 protect Q1 from excessive source-to-gate voltage and R108 prevents Q1 from oscillating. Protection is also provided for remaining MOSFETs in the output stage. Output of this stage, called PA OUT HI, is the output of the Power Amplifier assembly. Components R120 and L10 isolate capacitive loads.

2-146. PA SENSE CURRENT CANCELLATION CIRCUITRY

During dc operation of the Power Amplifier, sense current in the 500 kilohm feedback resistor (on the resistor network in the HR8 assembly) can cause an output error because of the finite resistance path of the connection to the load. Op amp U1 eliminates this error by feeding an equal and opposite current in this path. The magnitude of this current is determined by PA OUT HI, which is connected to the non-inverting input of U1. This circuit generates a current through R8, which is equal to current flowing through the 500 kilohm feedback resistor. Sense-current cancellation is active only in dc 220V range.

2-147. PA IN STANDBY

The Power Amplifier schematic shows all relays and DG211 FET switches in the standby condition. The Power Amplifier 25 kilohm input resistor and R17 are tied to OS COM through Q39 and R118. Power Amplifier output is close to zero and the whole loop is stabilized.

To better understand Power Amplifier configuration in the ac/dc 220V range, refer to Figure 2-21.

2-148. PA OPERATION: 220V DC RANGE

During dc operation, Power Amplifier gain is -20, as determined by the 500 kilohm/25 kilohm resistor network on the HR8 assembly. Control line SW3, inverted by U8, turns on Q51. This references the +input of the precision op amp in the input stage to R COM. The DAC assembly is set to the negative 11V range and its outputs, DAC OUT HI and DAC SENSE HI, are connected to pin 2 of the resistor network on the HR8 assembly by relay K2. The sense current cancellation circuit is active during dc operation. Its output, SIG1, is connected to the resistor network feedback resistor pin 1 by relay K15A. The amplifier has a much lower bandwidth in this mode because of the much higher Miller capacitance in C57. Lower bandwidth results in lower amplifier noise.

The output signal, PA OUT HI, is routed to the High Voltage Control assembly (A14), where it goes through relay K10 and becomes PA OUT DC. PA OUT DC is routed to the Switch Matrix for connection to the OUTPUT HI binding post. The sense signal, PA SENSE DC from the Sense Current Cancellation circuit, is routed to the Switch Matrix assembly (A8) for connection to the OUT/SENSE HI or SENSE HI binding posts, thus making the binding post the sense point in internal sense and allowing for external sense through the SENSE HI binding post.

2-149. PA OPERATION: 220V AC RANGE

During ac operation, Power Amplifier gain is -10 as determined by the 4.99 kilohm input resistor R17, and 49.9 kilohm feedback resistors (R11 + R12 + R13). Control line SW3 turns Q50 on, which references the +input of the precision op amp in the input stage to OS COM. The Oscillator assembly (A13) is set to the 22V range and its output OSC OUT HI is connected to the input resistor R17 by relay K10A. The Power Amplifier output is connected to the feedback resistors R11-R13 by relay K12B.

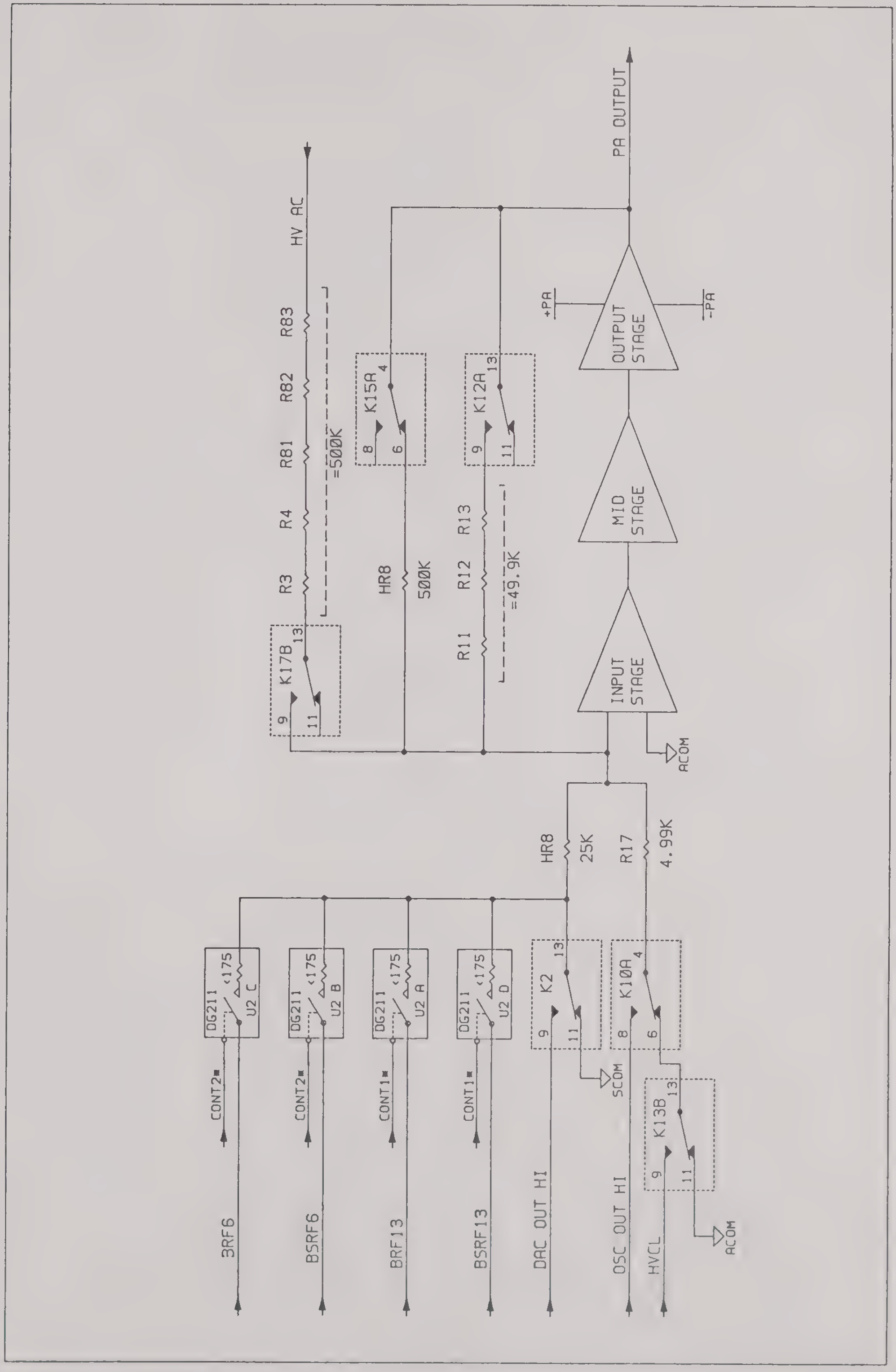

PA OUTPUT
HV AC
R83
R82
R81
R4
R3
=500K
K17B
9
11
13
K15A
8
6
4
HR8
500K
K12A
9
11
13
R11
R12
R13
=49.9K
+PA
-PA
OUTPUT STAGE
MID STAGE
INPUT STAGE
ACOM
HR8
25K
R17
4.99K
DG211
<175
U2 C
DG211
<175
U2 B
DG211
<175
U2 A
DG211
<175
U2 D
CONT2*
CONT2*
CONT1*
CONT1*
K2
9
11
13
K10A
8
6
4
SCOM
K13B
9
11
13
ACOM
BRF6
BSRF6
BRF13
BSRF13
DAC OUT HI
OSC OUT HI
HVCL

Figure 2-21. Power Amplifier Simplified Schematic

The Power Amplifier output is attenuated by a precise 1/100 by 220V range ac attenuator. The attenuated signal is connected to OSC SENSE HI, where it is sent to the Oscillator Control assembly (A12). The Oscillator Control assembly regulates the Oscillator Output so that an exact calibrated ac signal appears at OSC SENSE HI. Since the 220V range ac attenuator is completely characterized (as explained below), the exact desired signal appears at PA SENSE AC and hence at the appropriate sense point at the output.

The 220V range ac attenuator circuit contains op amp U4, a 400 kilohm/4 kilohm resistor network Z1, and transistor Q54. PA SENSE AC, which is connected to PA OUT HI at the load, is connected to the 400K input resistor (pin 1) of Z1 by relay K16. The 400 kilohm/4 kilohm node (pin 3) of Z1 is connected to the inverting input of U4.

During ac operation, control line CO* is inverted by U8, which turns on Q58 to connect the non-inverting input to OSC RCOM. Transistor Q54 supplies current gain for the output of U4 to drive the capacitance of the OSC SENSE HI line. This voltage is connected to the 4 kilohm feedback resistor (pin 4) of Z1. The output is connected to OSC SENSE HI by relays K10B and K11. The dc feedback 500 kilohm/25 kilohm resistor network and the sense-current cancellation circuitry are disconnected by energizing K15.

The sense signal, PA SENSE AC, and the output signal, PA OUT HI, are routed to the High Voltage Control assembly (A14), where relays K10, K13, and K3 connect them to HV SNS and HV OUT. HV SNS and HV OUT are connected to the binding posts by the Motherboard relays in the same manner as in the 1100V high voltage mode. Refer to the High Voltage assembly theory of operation for more information.

2-150. HIGH VOLTAGE ASSEMBLY SUPPORT MODE

2-151. High Voltage AC 1100V Range

During high voltage ac operation, the output of the Power Amplifier is routed to the input of a step up/down transformer on the High Voltage Control assembly (A14). Overall gain from the Oscillator Output to the High Voltage Output is -100 as determined by the 4.99 kilohm input resistor R17, and 500 kilohm feedback resistor (R3 + R4 + R81 + R82 + R83). Relay K10A connects the ac signal OSC OUT HI from the Oscillator Output assembly to input resistor R17. Relay K12 remains open as shown on the schematic, while K15 is energized to remove feedback used in 220V-dc operation.

Output from the High Voltage Control assembly, called HVAC on the schematic, is connected to the feedback resistors. Relay K17B is energized to close the feedback loop. Relay K13A is energized to enable U3 and its associated circuitry to provide dc feedback around the Power Amplifier. This maintains the dc level at the High Voltage-transformer input at zero. Control line SW3 is high, which turns Q50 on and turns Q51 off. Because sensing back to the Oscillator Control assembly is done by the High Voltage/High Current assembly, the output of the 220V range ac attenuator is disabled from OSC SENSE HI by relay K11.

Because sensing to the Oscillator Control assembly is done by the High Voltage assembly, the output of the 220V range ac attenuator is disabled from OSC SENSE HI by relays K10B and K11.

2-152. High Voltage DC 1100V Range and Current 2.2A Range

Operation of the Power Amplifier is the same for the 1100V dc and the 2.2A current functions. In these functions, the output of the Power Amplifier is routed to a step up/down transformer on the High Voltage Control assembly (A14). The Power Amplifier is configured the same as for 220V ac operation, except that the input is the square-wave signal HVCL from the High Voltage Control assembly, rather than OSC OUT HI, through relays K13B and K10A.

2-153. 220V DC INTERNAL CALIBRATION NETWORK

The 220V dc internal calibration network is used to determine the exact gains and offsets of the power amplifier. This circuit uses part of the resistor network HR8 as the input attenuator, and uses op amp U9, and zener diodes VR57 and VR58. Relay K4 connects the output of this circuit to the RCL line.

Zener diodes VR57 and VR58 reduce the power supplies for chopper-stabilized amplifier U9, which is used as a voltage follower.

2-154. PA CALIBRATION

The following paragraphs explain internal calibration taken by the Power Amplifier assembly. These steps include calibrating the offset, gain, and frequency characteristics of the Power Amplifier.

The first step is to measure the offset of the Main Amplifier (220V range). The DAC output is amplified by the Power Amplifier, which is configured for the dc 220V range, and its output connected to the internal cal zero amplifier located on the Switch Matrix assembly. Output of this internal cal zero amplifier is channeled to the DAC's adc amplifier circuit by the RCL line. Input of the internal cal zero amplifier is first connected to R COM where a checkpoint reading is taken by the DAC's adc circuit. The output of the Power Amplifier is then connected to the input of the internal cal zero amplifier and the DAC output is adjusted to the checkpoint reading out of the zero amplifier. This adjusted DAC output is a measure of the offset of the Power Amplifier. Also, refer to the Switch Matrix theory of operation.

The 175 kilohm/25 kilohm (internal cal) resistor network located on HR8 is calibrated next. This is illustrated in Figure 2-22. Offset of the 220V dc internal cal amplifier U9 is measured first. This is done by connecting pin 6 of 175 kilohm/25 kilohm resistor network to RCOM by relay K1, and pin 7 to ACOM by U5C and relay K3. ACOM is connected to RCOM through 051 during this step. Output of this internal cal amplifier is connected to the RCL line by relay K4, where it is measured by the adc circuit on the DAC assembly. As before, the DAC's output needed to obtain the checkpoint for this step represents the offset of the internal calibration amplifier.

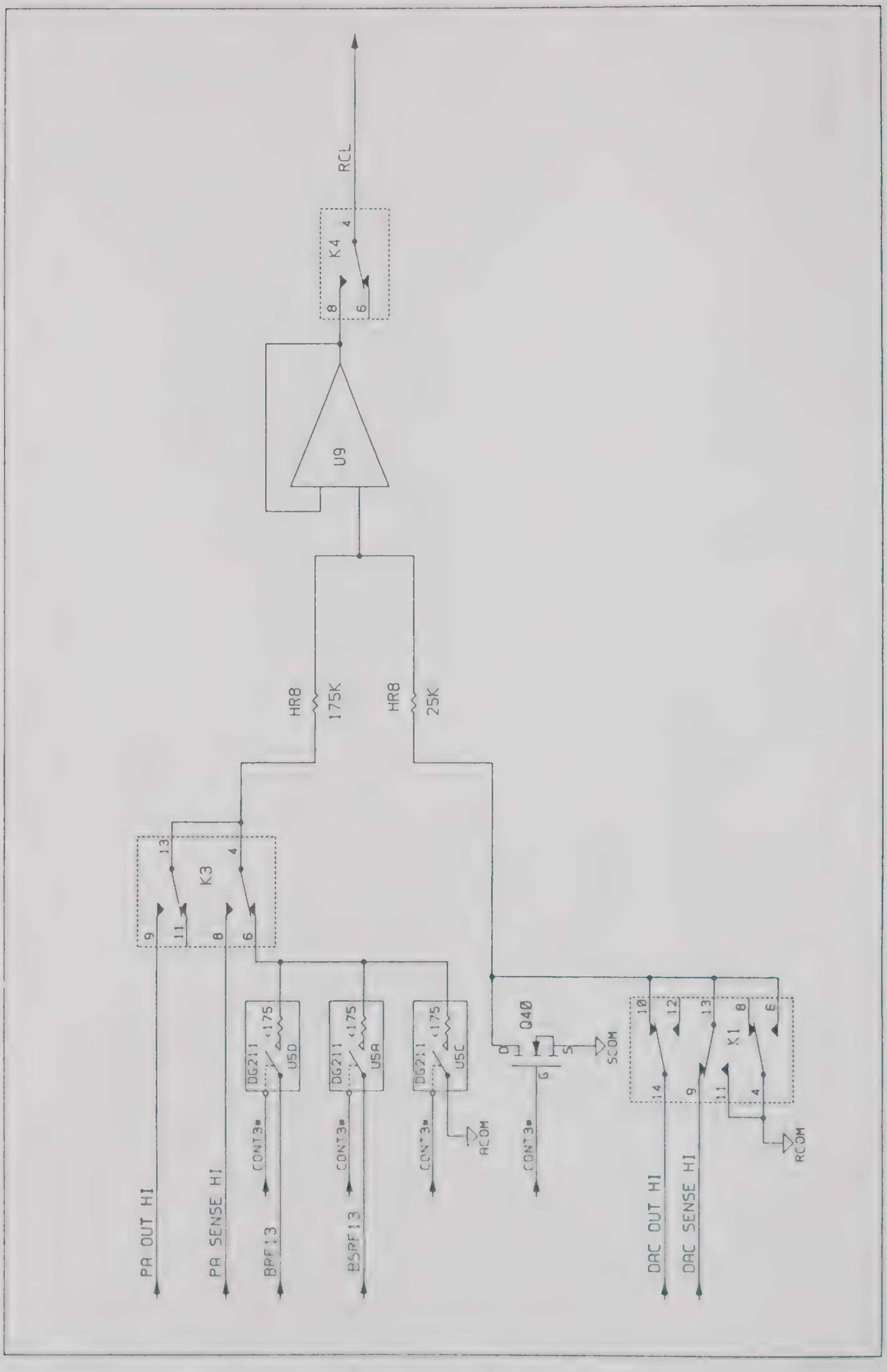

RCL
K4
4
8
6
U9
HR8
175K
HR8
25K
K3
13
4
9
11
8
6
DG211
<175
U5D
DG211
<175
U5A
DG211
<175
U5C
Q40
D
S
G
SCOM
K1
10
12
13
8
6
14
9
11
4
RCOM
RCOM
CONT3
CONT3
CONT3
CONT3
PA OUT HI
PA SENSE HI
BPF13
BSRF13
DAC OUT HI
DAC SENSE HI

Figure 2-22. Power Amplifier DC Calibration Network

Resistor network attenuation is calibrated next. Components U5A, U5D and K3 connect BSRF13 and BRF13 to the 175 kilohm end, while K1 connects R COM to the 25 kilohm end of the resistor network. The resulting 1.625V at the output is connected to the RCL line by relay K4, where it is connected to the +input of the adc amplifier circuit on the DAC assembly. The DAC output is connected to the adc circuit -input, and adjusted until the checkpoint reading is obtained. The exact value of this voltage is now known, so the system software computes the exact attenuator ratio from this known voltage, BSRF13 value, and the previous offset measurement.

Power Amplifier dc gain of approximately -20 is calibrated next. The Power Amplifier is configured as in the 220V dc operation, except the input is connected to the DAC's 6.5V reference BRF6 and BSRF6 by U2C and U2D respectively. The resulting -130V at the Power Amplifier output is connected to the 175 kilohm end of the internal cal resistor network by relay K3. The 25 kilohm end of this network is connected to DAC OUT HI and DAC SENSE HI by relay K1. The output of the internal cal amplifier is connected to the DAC's adc circuit as in the previous steps, and the DAC OUTPUT is adjusted until checkpoint is measured by the adc circuit. Since the exact attenuation of the resistor networks is already known, the exact Power Amplifier output voltage can be calculated. This in turn gives the exact Power Amplifier dc gain, since the exact value of 6.5V reference BSRF6 is known.

Attenuation of the 220V range ac attenuator (U4 and 396 kilohm/4 kilohm resistor network Z1) is calibrated next. This is illustrated in Figure 2-23. First, the offset of the attenuator circuit is measured by connecting the non-inverting input of U4 to ACOM through Q57 and thus to RCOM through Q51. Then, the Power Amplifier is configured for the 220V dc range with its inputs connected to the DAC's 6.5V reference BRF6 and BSRF6 by U2B and U2C respectively. The resulting -130V is connected to the 400 kilohm input resistor (Z1) of the 220V range ac attenuator by relay K16. RCOM (ACOM) is connected to the non-inverting input of U4 by Q58.

The +1.3V from the output of the attenuator circuit is connected to the RCL line by relays K10B and K11. This voltage on the RCL line is connected to the +input of the adc amplifier circuit on the DAC assembly. The DAC output is connected to the -input of the adc amplifier circuit, and is adjusted until a null is achieved. The exact value of this voltage is now known so the system software can compute the exact attenuator ratio.

The 220V range ac attenuator's attenuation ratio can vary over the frequency range. This variation can be accounted for if the frequency response of this network is characterized at a few spot frequencies. This is done by connecting the Power Amplifier output, which is set to 22V, to the AC CAL line by relay K14. The AC CAL line goes into the AC/AC CAL thermal sensor located on the Oscillator Control assembly. The Power Amplifier output of 22V is also attenuated through the AC Attenuator and sensed by the Oscillator Control via OSC SENSE HI. The Oscillator adjusts its output, and hence the Power Amplifier output,

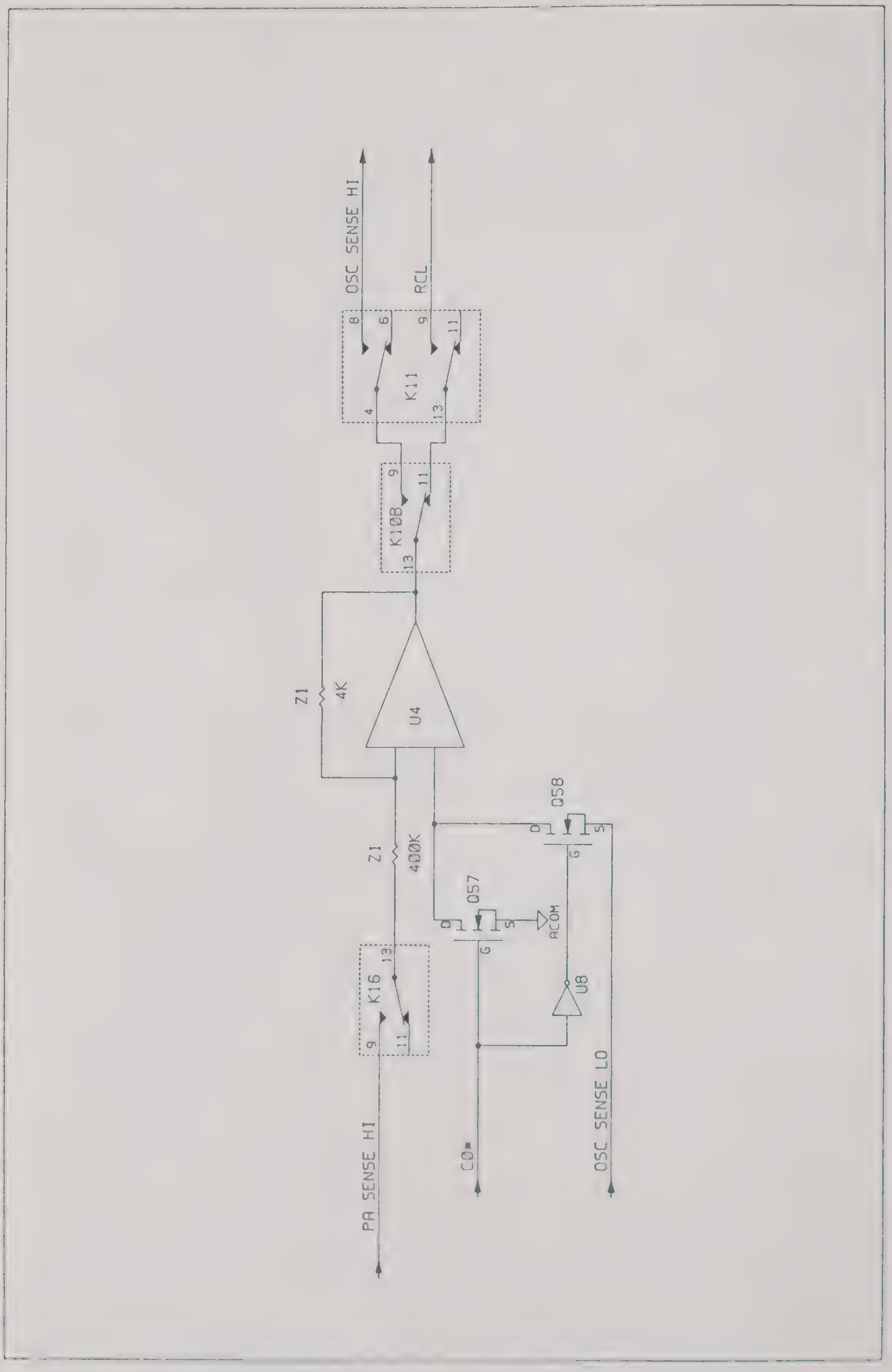

OSC SENSE HI
RCL
8
6
9
11
K11
4
13
9
11
K10B
13
Z1
4K
U4
Q58
D
S
G
Z1
400K
Q57
D
S
G
ACOM
U8
K16
13
9
11
PA SENSE HI
C0*
OSC SENSE LO

Figure 2-23. Power Amplifier Calibration AC Attenuator

until the ac/ac cal thermal sensor measures the same ac level for all these spot frequencies. The signal levels at OSC SENSE HI are stored in software at all such points.

The ac/ac cal thermal sensor located on the Oscillator Control assembly has a flat frequency response. The change in the ac attenuator's output at various frequencies for a constant thermal sensor output defines the frequency response of the Power Amplifier ac attenuator. These computed ac attenuator factors are stored in the system memory and are taken into account when the calibrator is configured to output ac voltages from the Power Amplifier.

Output stage current is limited to about 250 mA; Q60 limits the current sourced by the output stage, and Q61 limits the current sinked by the output stage. Transistor Q62 limits the current flowing through the middle stage. These current limits both protect the power amplifier circuitry and improve power amplifier transient response. Diode CR64 is a current source that maintains a current flow of at least 5 mA through the output devices at all times.

2-155. High Voltage Assemblies (A14 and A15)

The High Voltage/High Current assembly (A15) and the High Voltage Control assembly (A14) are used in with conjunction with other assemblies in the calibrator to generate the ±1100V dc, 1100V ac, and the 2.2A ranges. The two assemblies work together in generating these ranges. This theory of operation explains how these ranges are generated and discusses the individual circuits on each assembly. Refer to the High Voltage/High Current assembly simplified schematics (Figures 2-24 through 2-28) or the schematic diagram to understand this theory of operation better.

2-156. 1100V AC RANGE

Refer to Figure 2-24 for the following discussion. The ac signal generated by the Oscillator Output assembly (A13) is amplified by the Power Amplifier assembly (A16). The output of the Power Amplifier, PA OUT DC, is routed to the High Voltage Control assembly (A14), where it is further amplified by transformer T1 to generate the 1100V ac range. This high voltage signal from T1 is also the feedback signal to the Power Amplifier assembly. Relays K14-K16 connect the transformer windings in series during operation below 120 Hz.

Line PA OUT DC is connected to one side of the primary winding of step-up transformer T1 by relay K1 on the High Voltage Control assembly (A14). The other side of the primary winding is tied to PA COM through R67. One side of the secondary winding is tied to PA COM by relays K9 and K6. The other side of the secondary winding, the high voltage ac signal, is connected to HV OUT by relays K5, K12 and K3. Line HV OUT is connected to the OUTPUT HI binding post by relays K9 and K1 on the Motherboard.

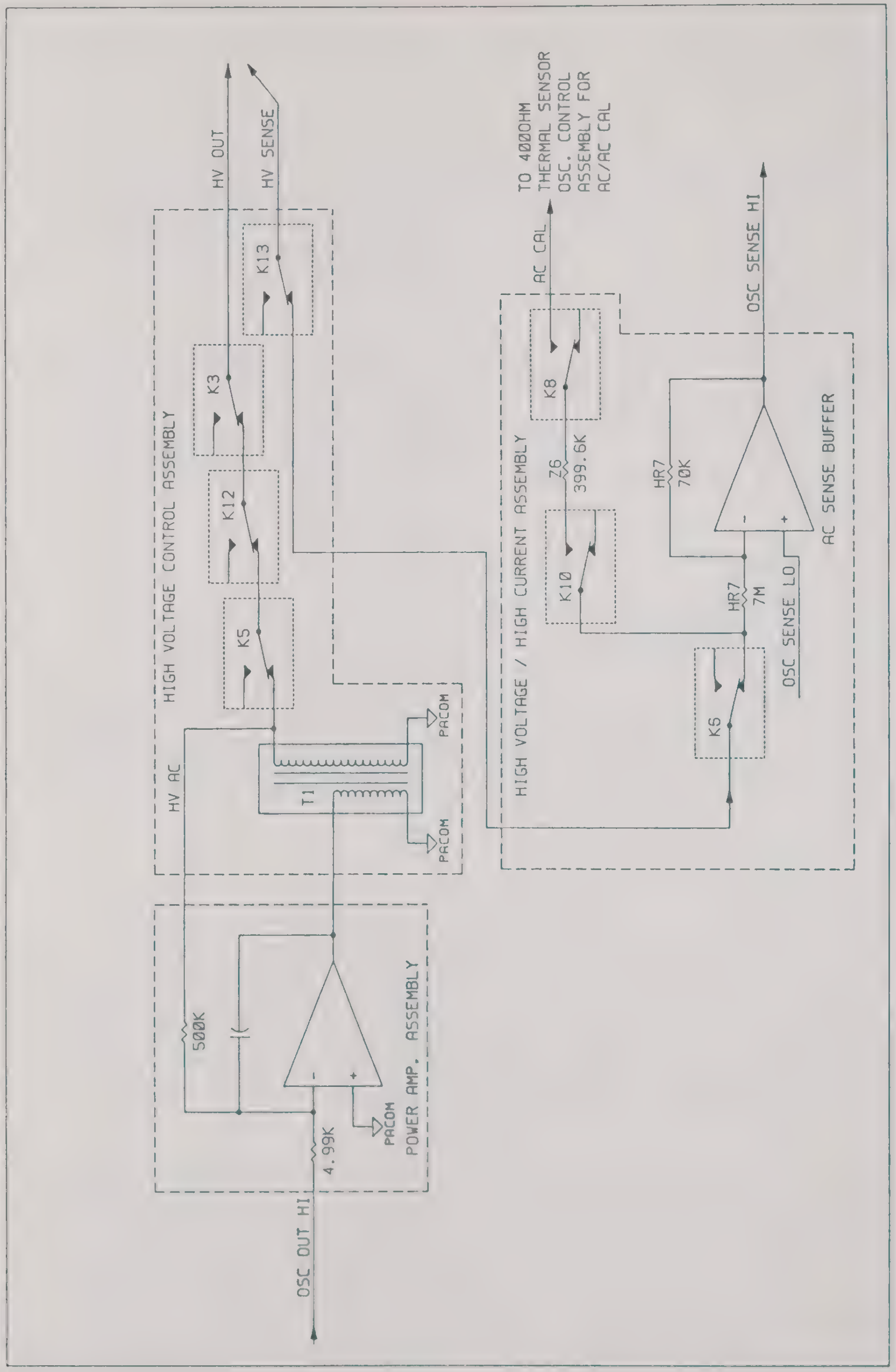

HV OUT
HV SENSE
K13
K3
K12
K5
HIGH VOLTAGE CONTROL ASSEMBLY
HV AC
T1
PACOM
PACOM
500K
4.99K
PACOM
POWER AMP. ASSEMBLY
OSC OUT HI
TO 400OHM
THERMAL SENSOR
OSC. CONTROL
ASSEMBLY FOR
AC/AC CAL
AC CAL
K8
Z6
399.6K
K10
HIGH VOLTAGE / HIGH CURRENT ASSEMBLY
OSC SENSE HI
HR7
70K
HR7
7M
K6
OSC SENSE LO
AC SENSE BUFFER

Figure 2-24. High Voltage/High Current Assembly 1100V AC Range

This high voltage ac signal is also connected to HVAC by relay K5. Line HVAC is the feedback signal to the Power Amplifier assembly. During high voltage operation, the input resistor of the Power Amplifier assembly is 5 kilohms. Line HVAC is connected to the feedback resistance, which is a series of resistors totaling 500 kilohm. This creates a gain of 100 to the Oscillator Output.

The SENSE HI binding post is connected to HV SENSE by relays K3, K2, and K10 on the Motherboard. HV SENSE, which is tied to HV OUT at the load, is connected to INT HV SNS by relay K13 on the High Voltage Control assembly (A14). INT HV SNS is routed to the High Voltage/High Current assembly (A15), where it is connected to the ac sense buffer circuit by relay K6. This circuit attenuates the high voltage signal by 100 and connects it to OSC SENSE HI through relay K4B. The level of attenuation is determined by the 7 megohm input and 70 kilohm feedback resistors on the HR7 assembly. OSC SENSE HI is used by the Oscillator Output assembly, which adjusts its output signal to maintain an exact feedback signal level. HV OUT and HV SENSE are routed to the High Voltage assembly (A15) where components CR9, CR10, and R33-R35 keep the voltage difference between them at 0.7V should they become disconnected at the load. Relay K11 connects HV OUT to HV SENSE during calibration in the ac function.

2-157. 1100V DC RANGE

Refer to Figure 2-25 for the following discussion. The High Voltage assembly (A15) amplifies the output of the DAC assembly (A11), set to the 11V range, by a gain of -100 to generate the 1100V dc range.

For operation in the 1100V dc range, DAC OUT HI and DAC SENSE HI from the DAC assembly, set to the 11V range, are tied together and connected to the input of the dc HV amplifier circuit by relay K1. The dc HV amplifier circuit, the HV dc output series pass and current limit circuit, and the HV dc power supply circuit on the High Voltage Control assembly (A14) constitute an overall amplifier with an inverting gain of 100. This gain is determined by the 70 kilohm input and 7 megohm feedback resistors on the HR7 assembly.

High voltage dc output, generated on the High Voltage Control assembly (A14), is obtained by filtering an approximate trapezoidal wave. The overall loop gain of this amplifier divides this ripple so the high voltage dc output is clean and stable.

Signal routing to the front panel binding posts is done in the same manner as the ac 1100V range.

2-158. HVDC POWER SUPPLY FILTER CIRCUIT

The high voltage dc power supplies are generated by the High Voltage Control assembly (A14) in conjunction with the Power Amplifier assembly (A16). The High Voltage Control assembly generates an amplitude-controlled square wave, SQ OUT, from the magnitude control circuitry. The magnitude control circuit contains all the circuitry on page 2 of the High Voltage Control assembly schematic.

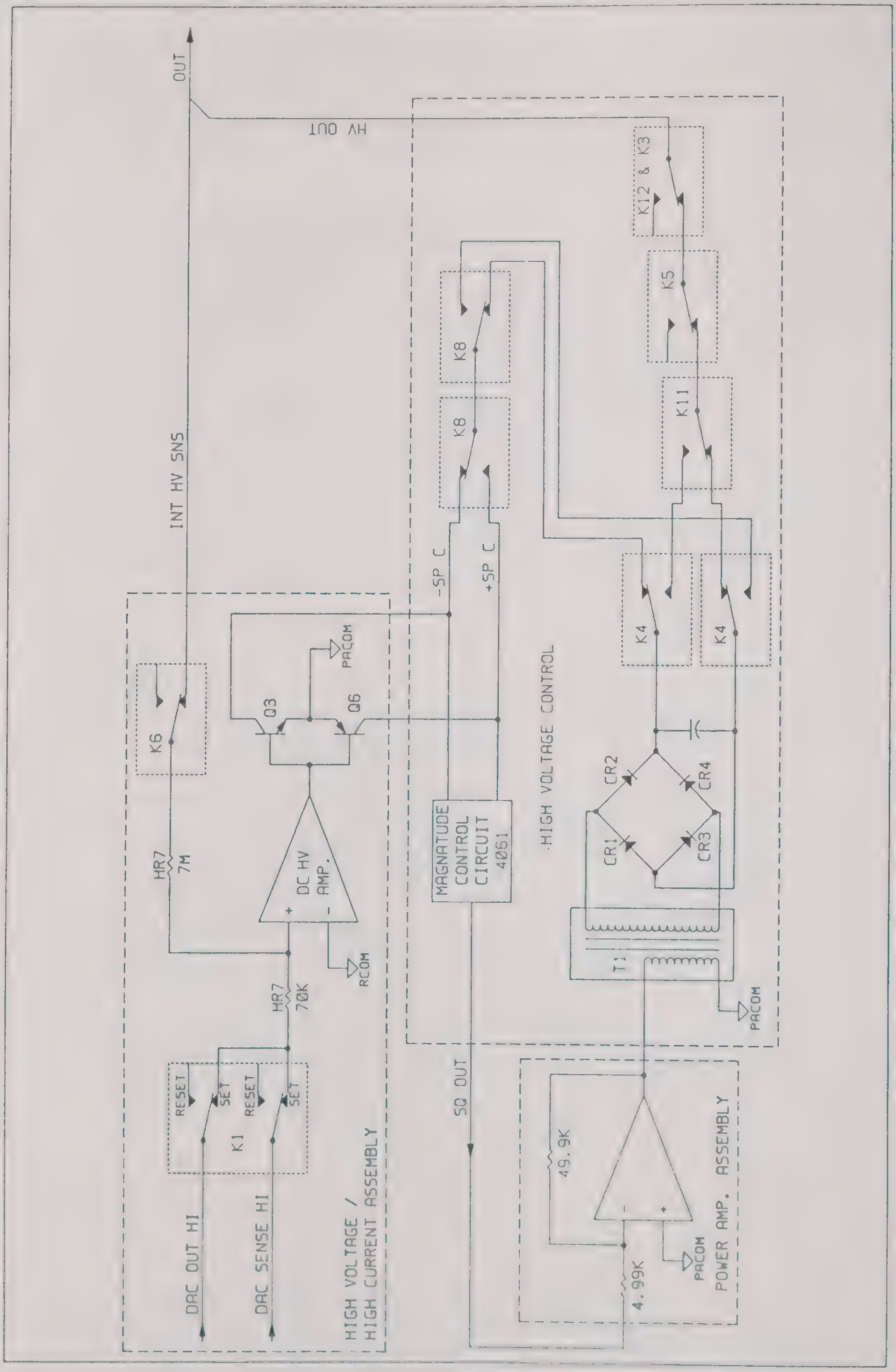

OUT
HV OUT
INT HV SNS
K12 & K3
K5
K11
K8
K8
-SP C
+SP C
K4
K4
HIGH VOLTAGE CONTROL
PACOM
Q3
Q6
K6
CR2
CR4
CR1
CR3
MAGNATUDE CONTROL CIRCUIT 4061
DC HV AMP.
+
-
HR7 7M
RCOM
HR7 70K
T1
PACOM
RESET
SET
RESET
SET
K1
SQ OUT
49.9K
+
-
4.99K
PACOM
POWER AMP. ASSEMBLY
DAC OUT HI
DAC SENSE HI
HIGH VOLTAGE / HIGH CURRENT ASSEMBLY

Figure 2-25. High Voltage/High Current Assembly 1100V DC Range

Signal SQ OUT is amplified by the Power Amplifier assembly with its output, PA OUT DC, connected to one side of the primary winding of transformer T1 by relay K1. The other side of the primary is connected to PA COM by R67. The secondary windings of T1 are connected to a bridge rectifier, CR1-CR4, by relays K9 and K6. The dc voltage from this rectifier is called +HVDC and -HVDC. Resistors R3-R5 form a 600 kilohm bleeder resistor for C1. Line HVDC is selected between +HVDC and -HVDC by relays K4 and K11. Line HVDC is connected to HV OUT by relays K5, K12 and K3.

During operation with a negative DAC voltage and a positive output from the High Voltage/High Current assembly, +HVDC is connected to HV OUT by relays K4, K11, K5, K12 and K3. +SP C is created from -HVDC by relays K4 and K8. During operation with a positive DAC voltage and a negative output from the High Voltage/High Current assembly, -HVDC is connected to HV OUT by relays K4, K11, K5, K12 and K3. -SP C is created from +HVDC by relays K4 and K8. Zener diodes VR4 and VR5 keep -SP C and +SP C, respectively, from exceeding 16V. The dc voltage level of +SP C and -SP C is controlled by the HV dc output series pass and current limit circuit on the High Voltage/High Current assembly. This in turn controls the magnitude of SQ OUT which sets the level of HVDC.

2-159. HV DC OUTPUT SERIES PASS AND CURRENT LIMIT CIRCUIT

The HV dc output series pass circuit controls the level of +SP C when the high voltage output is positive, and -SP C when the high voltage output is negative. Typically +SP C and -SP C are approximately ±6.8V dc with ripple equal and opposite polarity from the HVDC ripple.

When the DAC assembly is set to the +11V range, the output from the High Voltage assembly (with a gain of -100) is in the -1100V range. In this mode, -SP C is connected to the collector of transistor Q3. The output from the dc HV amplifier follows a change in the output voltage from the DAC assembly. This change controls how much Q3 is turned on or off. As the DAC voltage is increased, Q3 turns on pulling -SP C to PACOM. This causes the magnitude control circuit to increase the amplitude of SQ OUT which increases the output from the Power Amplifier assembly, thus increasing the HVDC until the overall loop is stable.

Operation in the +1100V range is basically the same, with transistor Q6 controlling +SP C in the same manner as above.

Current limiting is provided by Q4 if more than 35 mA is drawn from the output. If this condition occurs, Q4 pulls down CUR LIM, which is routed to the High Voltage Control assembly. (CUR LIM is also called RST.) When CUR LIM (RST) is pulled low, PS OFF goes high to turn off the square wave, SQ OUT, which shuts down the HVDC supplies. The generation of SQ OUT is described under the heading, "Magnitude Control".

2-160. DC HV AMPLIFIER/AC SENSE BUFFER

The dc HV amplifier and the ac sense buffer are basically the same circuit. The configuration is changed to provide the 100:1 amplification of dc voltage and the 100:1 attenuation of the high voltage ac signal. This is defined by the way the HR7 resistor network is configured in the circuit. This configuration is described in the 1100V ac range and 1100V dc range theory.

This circuit contains the HR7 resistor network and the circuitry contained in detail 1 as shown on page 1 of the High Voltage (A15) schematic. It is used in both the ac and dc voltage modes. Detail 1 contains the HR7 hybrid assembly which is an op amp mounted on a heated substrate hybrid bonded to a resistor network. The HR7 assembly gives this circuit excellent dc characteristics of low offset, noise and drift. The hybrid heater control circuit adjusts the base voltage of Q8 to deliver the proper power to the heater resistor. This maintains the HR7 assembly at a constant temperature in spite of environmental temperature variations. Transistor Q9 protects the hybrid in case Q8 fails. The output of the HR7 op amp is connected to a faster op amp (U2), which provides additional gain and a high slew rate. The output of U2 is called HVAMP OUT on the schematic.

In the dc voltage function, the output of this circuit, configured as a dc HV amplifier, is connected to the series pass circuit by relay K5B. Relays K5A, K7 and K14 add C4 in parallel with the 7 megohm feedback resistor in the HR7 assembly to filter the noise. ACOM is connected to RCOM by relay K3.

During operation in the ac voltage function relays are positioned as shown on the schematic. Components VR7 and VR8 provide input protection for the op amp on the HR7 assembly. Op amp U1 is added to the circuit by relays K9, K8B and K6. This op amp inverts HVAMP OUT so that the signal to OSC SENSE HI is in phase with the output of the Oscillator assembly. ACOM is connected to OSC RCOM by relays K3 and K4A.

2-161. 2.2A RANGE

Refer to Figure 2-26 for the following discussion. Most of the same circuitry is used to create the ac and dc 2.2A current ranges. The Current assembly (A7) is configured to the 22 mA range and connected to the IHV line which drives the 2.2A amplifier circuit on the High Voltage assembly (A15). This 2.2A amplifier provides a gain of 100 to the 22 mA range from the Current assembly to create the 2.2A range.

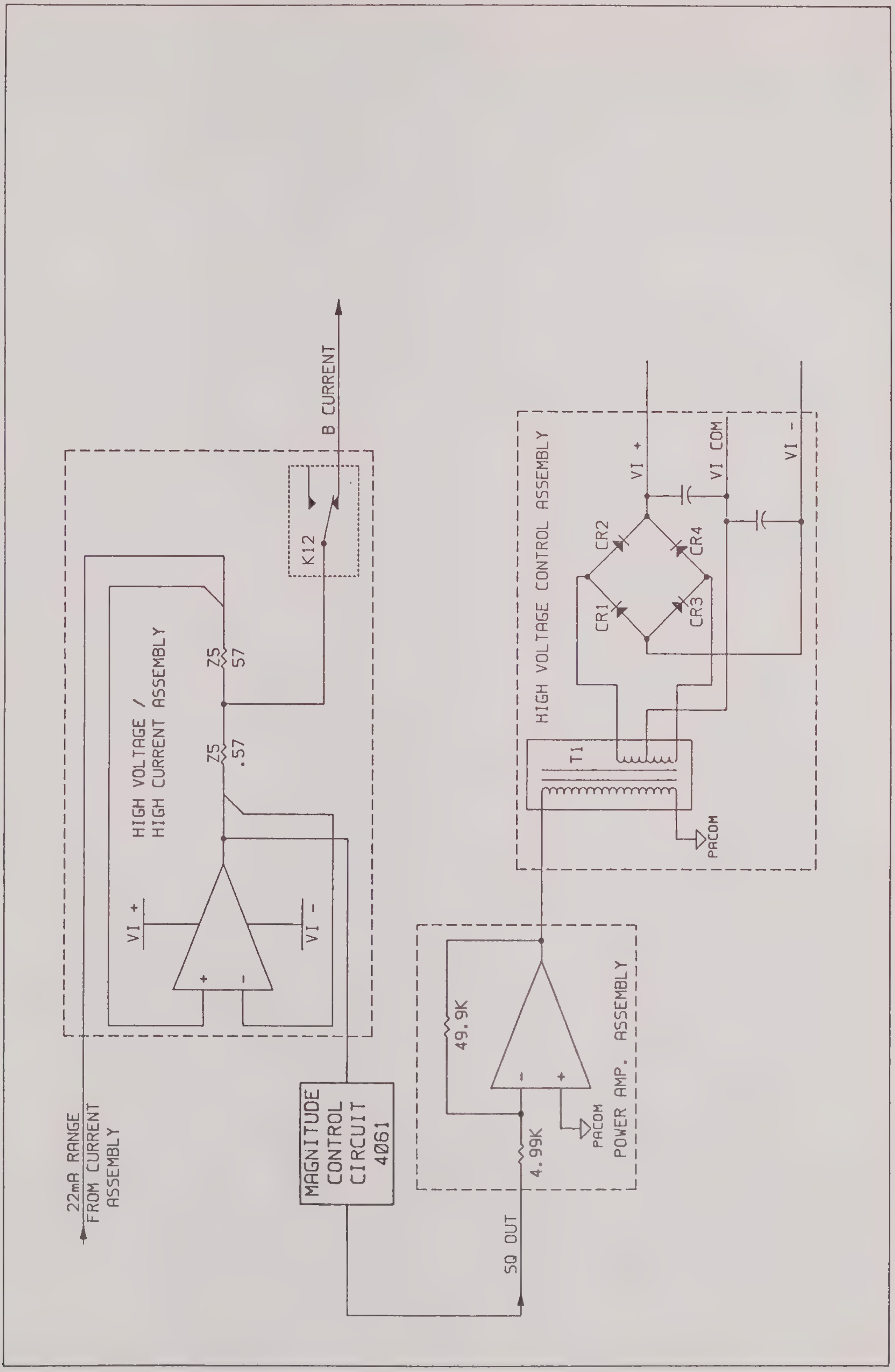

22mA RANGE FROM CURRENT ASSEMBLY
HIGH VOLTAGE / HIGH CURRENT ASSEMBLY
VI +
VI -
Z5 .57
Z5 57
K12
B CURRENT
MAGNITUDE CONTROL CIRCUIT 4061
SQ OUT
4.99K
49.9K
PACOM
POWER AMP. ASSEMBLY
T1
PACOM
HIGH VOLTAGE CONTROL ASSEMBLY
CR1
CR2
CR3
CR4
VI +
VI COM
VI -

Figure 2-26. High Voltage/High Current Assembly 2.2A AC and DC Ranges

Resistor network Z5 and hybrid H4 determine the performance of the 2.2A range. Current from the A7 assembly develops a voltage across the 57 ohm portion of Z5. The 2.2A current amplifier circuit forces the same voltage across the 0.57 ohm portion of Z5. Because the ratio of these resistors is 100, the current through 0.57 ohm resistor is 100 times that coming from the Current assembly (A7). Relay K12 connects this 2.2A range current to B CUR where it is routed to the Current assembly (A7), which provides the proper relay switching to the front panel binding posts.

The 2.2A amplifier circuit contains the heater-controlled hybrid H4, op amps U3-U5, and transistors Q11-Q16. This circuitry is outlined as detail 2 on page 2 of the High Voltage/High Current assembly schematic. The H4 hybrid consists of an op amp mounted on a heated substrate. The heater control circuit adjusts the base voltage of Q18 to deliver the proper power to the heater resistor. This maintains the hybrid at a constant temperature in spite of environmental temperature variations. Transistor Q19 protects the hybrid in case Q18 fails.

The output of the H4 hybrid is a voltage directly proportional to the current output G OUT. Q22 and R72-R76 form a high-frequency path for loop stability. In the ac current function, op amp U3A and its associated circuitry create a half-wave signal equal to the positive peaks of the ac signal from H4. Resistor R47 keeps this half-wave signal approximately 0.7V above 0V. This half-wave signal is then subtracted from the ac signal coming from H4 by op amp U3B and its associated circuitry. This creates a half-wave signal equal to the negative peaks of the ac signal from H4. Resistor R45 keeps this half-wave signal approximately 0.7V below 0V. Transistor Q15 and resistor R50 generate a current from the negative peaks created by U3B. Transistor Q16 and R48 generate a current from the positive peaks created from U3A. The current from Q15 and R50 develops a voltage across the 191 ohm resistor (R69). This voltage is used by op amp U4 which drives transistors Q11 and Q12 in the Darlington configuration for current gain. Resistor R67 is the feedback path for U4. The voltage across 191 ohm resistor R69 is the same as across the 0.1 ohm resistors R68 and R78. Since the value of R68 and R78 is 1000 times less than R69, the current through R68 is 1000 times greater. The current from Q16 and R48 is increased by 1000, in the same manner as previously stated, with op amp U5, resistors R56 and R57, and Darlington-configured transistors Q13 and Q14.

Only half of the circuitry is used, since the output current is either positive or negative in the dc current function. When outputting a positive current, the voltage from H4 is negative. Since there is no positive voltage, the output of U3A is zero, thus no current is developed by R48 and Q16. At this time the negative voltage from U3B generates an output current in the same manner as in the ac current function. The opposite occurs when outputting a negative dc current.

2-162. 2.2A POWER SUPPLY FILTER CIRCUIT

The 2A range power supply filter circuit on the High Voltage Control assembly (A14), operating in conjunction with the Power Amplifier assembly (A16), generates the VI ±supplies used by the 2.2A amplifier circuit on the High Voltage/High Current assembly (A15). The High Voltage Control assembly generates an amplitude controlled square wave, SQ OUT, from the square wave generator and square wave amplifier circuits. This SQ OUT is amplified by the Power Amplifier assembly (A16), which is set for a gain of 10. This amplified output, PA OUT DC, is connected to the primary side of transformer T1 by relay K1. The stepped-down secondary voltage is full-wave rectified by CR5 and filtered by C3 and C4 to generate the VI+ and VI- supplies respectively. VI± are low-voltage, high current supplies. These supplies, along with the secondary center tap VI COM, are routed to the High Voltage assembly.

VI+ supplies the output current when sourcing while VI- sinks it. To minimize power dissipation, the magnitude of the VI± supplies is controlled to minimize the emitter to collector voltage on the output stage transistors (Q11, Q14). This is done by controlling the magnitude of the SQ OUT signal. The controlling function is described later in the Magnitude Control theory.

2-163. HIGH VOLTAGE DIGITAL CONTROL

Digital control circuitry on the High Voltage Control assembly (A14) also contains the control for the High Voltage/High Current assembly (A15). The heart of the digital control circuitry is an 82C55 Programmable Peripheral Interface IC (U9), which is under software control via the guarded digital bus. This IC has three ports which generate 24 outputs. These outputs are used to control four 5801 driver ICs (U10-U13), and an analog multiplexer (U14) for self diagnostics.

All relays on both HV assemblies are controlled by drivers U10, U11, U12, and U13. Driver U12 controls relays K14-K16, and generates seven control lines for controlling various FETs and CMOS Analog Switch ICs contained on both assemblies. Port A (PA0-PA7) of U9 provides a common input bus for all drivers. Port C (PC0-PC5) of U9 provides the strobe and enable lines for these drivers. Driver U10, which controls the non-latching relays (K1-K6, K8-K13) on the High Voltage Control assembly, is strobed by PC1. PC0 is inverted by U8C to provide the enable. Driver U11 controls latching relay K7 on the High Voltage Control assembly and latching relays K1-K3 on the High Voltage/High Current assembly. This driver is strobed by PC3. PC2 is inverted by U8D to provide the enable. Driver U13, which controls the non-latching relays on the High Voltage/High Current assembly (K4-K12 and K14), is strobed by PC5 and enabled in the same manner as U10. Driver U12, which generates the Control Lines, is strobed by PC4 and enabled in the same manner as U10. Control line RST, from this driver, is inverted by U8E to create PS OFF. This control line is used by the magnitude control circuit described later.

The diagnostic circuit enables the 5700A to monitor seven points on either the High Voltage/High Current assembly (A15) or the High Voltage Control assembly (A14). A 4051 analog multiplexer (U14) is controlled by PB4-PB7 of port B of U9. This multiplexer selects which one of these seven voltages are to be applied to the SDL line where it is measured by the adc circuit on the DAC assembly (A11). HV MUX0-HV MUX3 are points on the High Voltage/High Current assembly. HV MUX0 and HV MUX1 monitor the oven temperature of the H4 and HR7 hybrids respectively. The output of the dc HV amplifier/ac sense buffer circuit is divided by R18 and R19 to generate HV MUX2. HV MUX3 monitors the current draw through the HV dc output series pass circuit to detect an overcurrent condition in the high voltage dc mode. Resistors R28 and R27 sense the current for a positive high voltage output and a negative high voltage output respectively. MUX5-MUX7 are points on the High Voltage Control assembly. MUX5 monitors the high voltage output. HV OUT is divided by R9-R13 and R64.

This divided output is connected to the output peak measure circuit which uses op amp U1B. In the dc V function, this circuit is a voltage follower. In the ac voltage function, this circuit is a peak detector.

The output of U1B charges C5 with R17 being the discharge path. This provides a positive dc voltage at MUX5. The output of the absolute value circuit is divided by R55 and R56 to generate MUX6. The output of the reference and error amplifier circuit is divided by R46 and R47 to generate MUX7.

2-164. HIGH VOLTAGE CALIBRATION

Refer to Figure 2-27 for the following discussion. The resistor network, (70 kilohm and 7 megohm) which is part of the HR7 hybrid/resistor network assembly, determines the accuracy of both 1100V ac and dc ranges. Calibration involves determining its offset and gain constants.

To determine the offset, DAC outputs are connected to 70 kilohm input resistor by K1. The output of the dc HV amplifier is inverted by U1 and its output is connected to the 7 megohm feedback resistor by K9, K8B, and K6. This configuration creates an inverting amplifier with a gain of 100. Relay K9 connects the output of this amplifier to the RCL line, where it is measured by the adc circuit on the DAC assembly (A11). The DAC's adc circuit first connects both its +input and -input to RCOM and takes a checkpoint reading. The +input is then connected to the RCL line, which at this time is the amplifier output, and adjusts the DAC output to obtain the same reading as the previous check point. This offset cal constant is stored in nonvolatile memory.

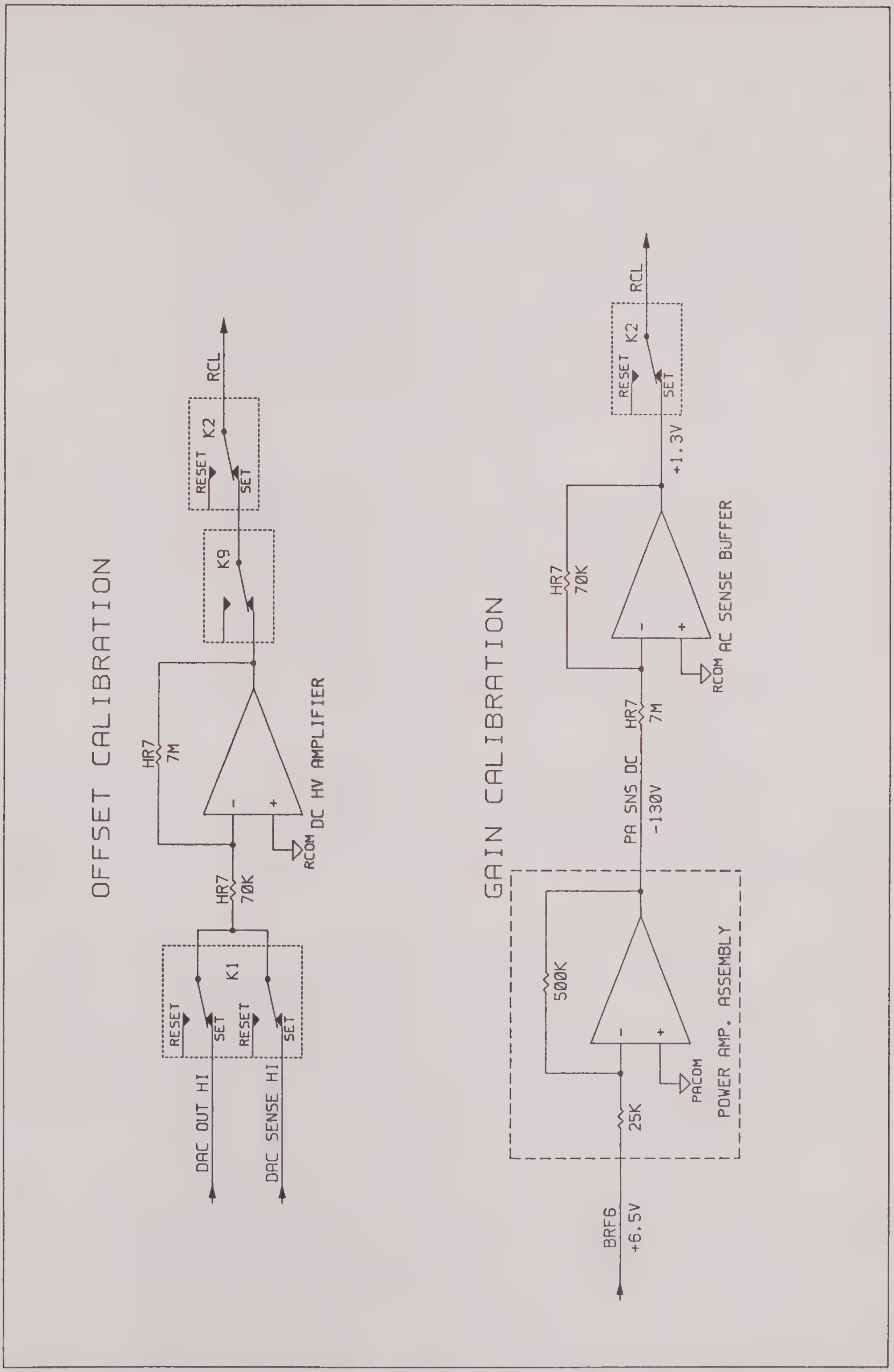

OFFSET CALIBRATION
DAC OUT HI
DAC SENSE HI
K1
RESET
SET
RESET
SET
HR7
70K
HR7
7M
DC HV AMPLIFIER
RCOM
K9
K2
RESET
SET
RCL
GAIN CALIBRATION
BRF6
+6.5V
25K
500K
PACOM
POWER AMP. ASSEMBLY
PA SNS DC
-130V
HR7
7M
HR7
70K
AC SENSE BUFFER
RCOM
+1.3V
K2
RESET
SET
RCL

Figure 2-27. High Voltage/High Current Assembly Calibration

To determine the gain, the High Voltage/High Current assembly is configured in the ac 1100V range, except PA SNS DC is connected directly to the 7 megohm input resistor of the ac sense buffer by relays K8 and K6 instead of going through step-up transformer T1. The 6.5V reference (BRF6) is connected to the Power Amplifier assembly (A16) which is configured for an inverting gain of 20 to create a -130V output. The ac sense buffer circuit attenuates this signal by 100 to generate 1.3V at its output. This 1.3V is connected to the RCL line by relay K2 where it is connected to the +input of the adc circuit on the DAC assembly. DAC OUT HI, which is connected to the -input, is adjusted until a null is achieved. The gain can be determined by using this and the previous offset reading. This determines the exact ratio of 70 kilohm and 7 megohm resistor network on the HR7 assembly. This known ratio can then be used to output very accurate dc voltages in 1100V dc range.

2-165. CALIBRATION OF THE AC FUNCTION

The HR7 resistor network, previously calibrated at dc, is further characterized for its frequency response. The 5700A is placed in the ac 1100V range, except with HV OUT and HV SENSE tied by relay K11 on the High Voltage/High Current assembly (A15) instead of being tied at the load. The Oscillator Output assembly is set so the output of the High Voltage/High Current Voltage assembly is approximately 695V at 130 Hz. This high voltage output (INT HV SNS) is connected to the AC CAL line, through 399.6 kilohm resistor Z6, by relays K10 and K8A on the High Voltage assembly. The AC CAL signal is routed to the Oscillator Control assembly (A12) where it is measured by a 400 ohm rms sensor.

Since the voltage is approximately 700V and it is applied through a 399.6 kilohm resistor (Z6) to the 400 ohm rms sensor, approximately 1.75 ma of current flows through the rms sensor on the Oscillator Control assembly. A dc reading of the sensor, which is approximately 0.7V (1.75 mA x 400 ohms), is taken and then stored in memory with the Oscillator Output level.

The Oscillator Output frequency is then increased to 500 Hz. The Oscillator Output level is adjusted so the dc reading from the rms sensor is the same as for 130 Hz, and stored in memory. This step is again repeated at 1 kHz. This characterizes the HR7 resistor network's frequency response. An accurate ac voltage can now be obtained at any frequency between 50 Hz and 1 kHz. The theory of operation for the rms sensor is contained in the Oscillator Control (A12) theory.

2-166. CALIBRATION OF THE CURRENT FUNCTION

Refer to Figure 2-28 for the following discussion. The resistor network Z5 determines the accuracy of the 2.2A current range. Calibration involves determining its offset and gain constants. The 5700A is configured as in the 2.2A dc function, except that the Current assembly (A7) is set to the 2.2 mA range.

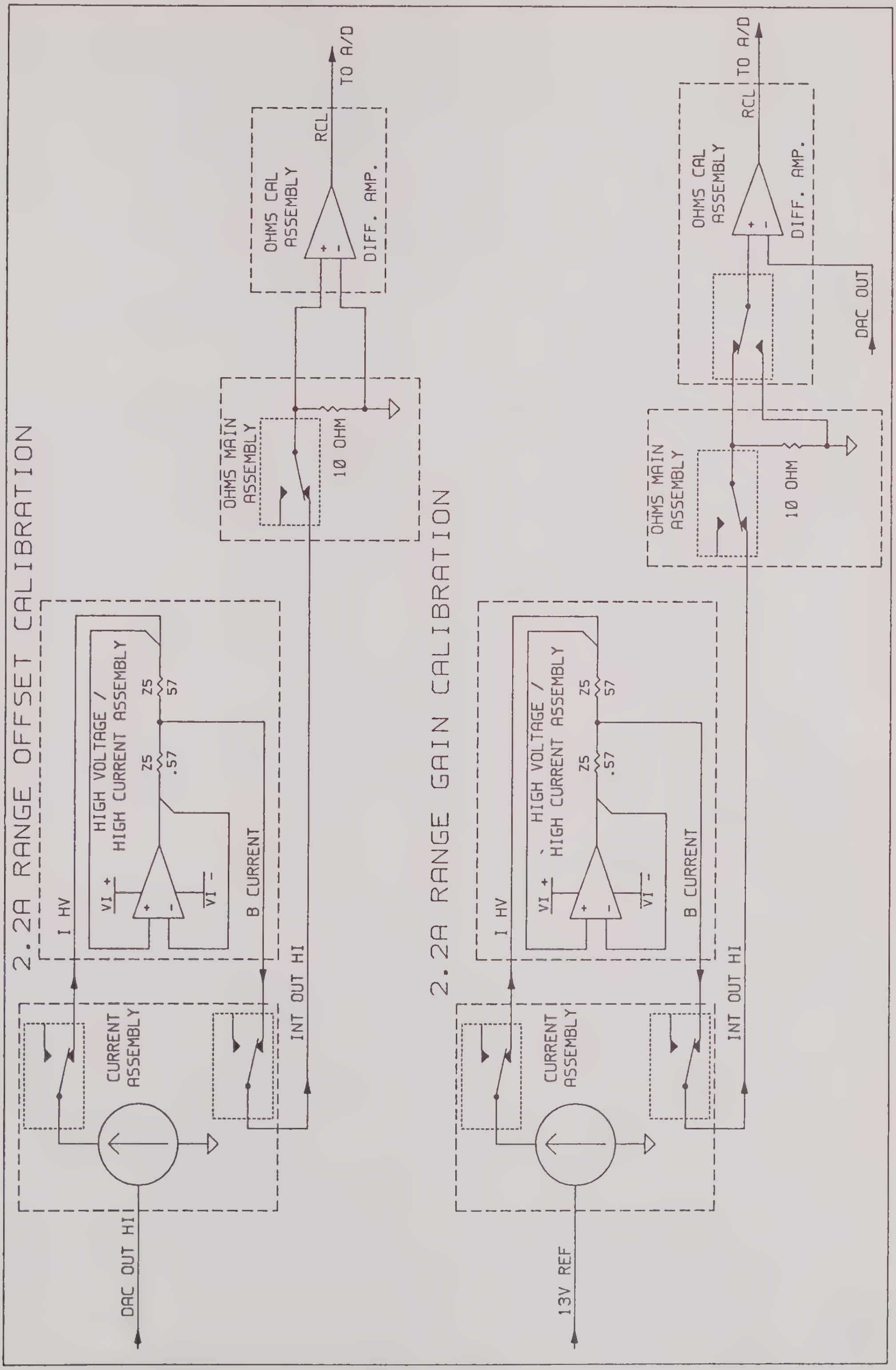

2.2A RANGE OFFSET CALIBRATION
DAC OUT HI
CURRENT ASSEMBLY
I HV
B CURRENT
INT OUT HI
HIGH VOLTAGE / HIGH CURRENT ASSEMBLY
VI +
VI -
Z5
.57
Z5
57
OHMS MAIN ASSEMBLY
10 OHM
OHMS CAL ASSEMBLY
DIFF. AMP.
RCL
TO A/D
2.2A RANGE GAIN CALIBRATION
13V REF
CURRENT ASSEMBLY
I HV
B CURRENT
INT OUT HI
HIGH VOLTAGE / HIGH CURRENT ASSEMBLY
VI +
VI -
Z5
.57
Z5
57
OHMS MAIN ASSEMBLY
10 OHM
OHMS CAL ASSEMBLY
DIFF. AMP.
RCL
TO A/D
DAC OUT

Figure 2-28. High Voltage/High Current Assembly 2.2A Range Calibration

To determine offset, the output (B CUR) is routed back to the Current assembly where it is connected to INT OUT HI. INT OUT HI is routed to the Ohms Main assembly (A10), where it is connected to a previously calibrated 10 ohm resistor. The voltage generated across this 10 ohm resistor is routed to the differential amplifier on the Ohms Cal assembly (A9). The output of the differential amplifier is routed to the DAC assembly (A11) where it is measured by its adc circuit. A checkpoint reading is first taken by removing INT OUT HI from the 10 ohm resistor and measuring the voltage across the resistor. The offset is then measured by connecting INT OUT HI to the 10 ohm resistor. The DAC assembly, which controls the output of the Current assembly, is adjusted until the adc circuit measures the same as the previous checkpoint reading.

To determine gain, the 5700A is configured as in the previous step, except with the Current assembly outputting 1.3 mA generated from the 13V reference (BRF13 and BSRF13) from the DAC assembly. This 1.3 mA is amplified 100 times by the 2.2A amplifier. The resulting 130 mA is connected to the 10 ohm resistor on the Ohms Main assembly by the same path as for the offset calibration. The resulting 1.3V across this 10 ohm resistor is routed to the Ohms Cal assembly (A9), where it is connected to the -input of the differential amplifier. The +input of the differential amplifier is connected to the output of the DAC assembly. The output of the differential amplifier is connected to the RCL line which is routed to the adc circuit on the DAC assembly. The DAC output, which is the +input of the differential amplifier, is adjusted until a null is measured on the RCL line by the DAC's adc circuit. This step is repeated by changing the -input of the differential amplifier to the other side of the 10 ohm resistor. The software now computes the exact voltage drop across the 10 ohm resistor. Gain is determined by using this and the previous offset reading.

2-167. HIGH VOLTAGE MAGNITUDE CONTROL

The square wave (SQ OUT) used in the previously described functions, is created and amplitude controlled by the High Voltage Control assembly (A14). This circuitry, shown on page 2 of the schematic, contains the absolute value circuit, signal/polarity selection circuit, reference and error amplifier, square wave generator, and the square wave amplifier.

The absolute value circuit contains op amp U2A, U2B, Q3, diodes CR8 and CR9, capacitor C20, and resistors R27-R32. During operation in the ac current function, this circuit creates an absolute value of the G OUT signal from the the collectors of the 2.2A output transistors. Op amp U2A generates a negative half-wave signal equal to the positive peaks of G OUT. Resistors R32 and R27 sum this half-wave signal and the input signal G OUT at the input of U2B. Capacitor C20 averages the voltage so the output of U2B is a dc voltage which represents the positive peak voltage of G OUT. In the high voltage dc function, the 2.2A amplifier circuit is not used, so the output of U2B is 0V.

The signal/polarity selection circuit generates the ERROR SIGNAL used by the error amplifier. It contains op amp U2C, CMOS analog switch U6, and resistor R35-R39. Control line V/I controls U6B and U6C which select the VI± when in the current mode. Control lines ±* and ± control U6A and U6D respectively. These switches, operating in conjunction with U6B and U6C, select between VI±, -SP C or +SP C. In the current function, U2C subtracts the power supply voltage (VI±) from the absolute voltage created by the absolute value circuit to create ERROR SIGNAL. This gives a measure of the emitter to collector voltage of the driving device for each operating function. In the positive dc voltage function, U2C is configured as a unity-gain inverting op amp. In the negative dc voltage function, U2C is configured as a voltage follower.

The reference and error amplifier circuit contains op amp U2D, CMOS analog switch U7B, zener diode VR1, transistors Q2 and Q4, diodes CR10-CR11, capacitor C18, and resistors R40-R45. Zener diode VR1, R40-R45, Q4, and U7B create a reference voltage. Control line V/I controls U7B which switches R43-R45 in or out to change this reference voltage value, depending on the operating function. In the HV dc range, R40 and R41 are used, balancing the error amplifier with the ERROR SIGNAL near 6.8V. In the 2A dc range, U7B and Q4 are on, R43 is paralleled with R41, and R45 is paralleled with R40, so the error amplifier balances when the ERROR SIGNAL is near 3.1V. In the 2A ac function, Q4 is off, R44 is in series with R45, so the error amplifier balances when the ERROR SIGNAL is about 5.2V. The output of U2C, ERROR SIGNAL, is summed with the reference voltage by R40 and R41. This voltage is connected to the error amplifier U2D which, with C18, is configured as an integrator. The error amplifier generates the signal AMPLITUDE, which dynamically controls the amplitude of the square wave. This AMPLITUDE is connected to the input of U7C. -AMPLITUDE, provided by inverting op amp U1A, is connected to the input of U7D. Control line PS OFF provides a soft start of the error amplifier. With this line high, Q2 is turned on, shorting C18, which sets the AMPLITUDE control line to 0V. Once the High Voltage/High Current assembly is set up for proper operation, this line goes low to turn off Q2.

The square wave generator circuit creates a 1 kHz signal QSQB and its complement QSQB*. These signals are generated by R26, C17, and astable multivibrator U4. Control line FREQ controls the CMOS analog switch U7A, which parallels R25 to R26. This changes the frequency of oscillation to prevent beating when putting out 2A ac near 1 kHz. Control line PS OFF goes high to shut down this oscillator when its not required.

The square-wave amplifier contains op amp U3 and CMOS analog switches U7C and U7D. Switch U5C is connected to the AMPLITUDE voltage and is controlled by QSQB from the square wave generator. Switch U7D is connected to AMPLITUDE through inverting op amp U1A and is controlled by QSQB* from the square wave generator. The input signal to the square wave amplifier is the output of U7C and U7D. Since QSQB* is the complement of QSQB, the resulting square wave has a positive peak equal to AMPLITUDE, and a negative peak equal to -AMPLITUDE. This square wave is amplified by U3, which is configured for a gain of 2.6, to create SQ OUT. SQ OUT is the square-wave signal used by the Power Amplifier assembly in the previously described functions.

2-168. Ohms Overview

The Ohms function for the 5700A is provided by two plug in circuit boards, the Ohms Main assembly (A10) and the Ohms Cal assembly (A9). These two assemblies function as one to supply fixed values of resistance from 1 ohm to 100 megohm. Resistance output is available in values of 1×10^n (1, 10, 100, 1k ... 100M) and 1.9×10^n (1.9, 19, 190, ... 19M) from short to 100 megohm. After the ohms function is calibrated, the Output Display shows the true value of the resistance selected.

These assemblies are also used to calibrate the 5700A Current function. The Ohms Main assembly contains all the resistor values except the 1 ohm, 1.9 ohm, and short, which are located on the Ohms Cal assembly. It also contains the relays and their drivers to switch these values as requested under program control.

The Ohms Cal assembly contains all calibration circuits except for one op amp on the Ohms Main assembly. It also contains a circuit to provide accurate calibration of two-wire ohmmeters. In addition, there are relays, relay drivers, and logic to interface the Ohms assemblies to the digital bus.

2-169. Ohms Main Assembly (A10)

The Ohms Main assembly uses three Fluke hermetically-sealed thin film resistor networks (Z1, Z2 and Z3) to obtain values from 10 ohm to 19 megohm. The values are arranged in two strings, one for decade values and the other for the multiples of 1.9. The 100 megohm value is achieved by inserting a 90 megohm film resistor (R1) in series with the decade string.

2-170. SELECTION OF RESISTANCE VALUES

Refer to Figure 2-29 for the following discussion. Relays select the resistance values. All resistor values have four-wire connections except 100 megohm, which is two-wire. The output high and sense high side of a resistance value is connected to INT OUT HI and INT SENSE HI by relays K1 and K2 in the reset position, except 100 megohm, which is connected to INT OUT HI by K5. Relays on the Motherboard connect INT OUT HI and INT SENSE HI to the OUTPUT HI and SENSE HI binding posts.

The low side of the 1x string is connected to OHMS SENSE LO and OHMS OUT LO by relay K27 (A and B) in the reset position. The low side of the 1.9x string is connected to the same lines by relay K39 (A and B). These lines are routed to the Ohms Cal assembly where they are connected via relays to the OUTPUT LO and SENSE LO binding posts.

The 10 megohm value is selected by K7 (reset) and K8 (energized) and the 1 megohm value by K9 and K10 (reset). Selection of decades below 1 megohm is done by K15 and K16 (reset) plus a pair of relays from K17 through K26A. For example, to select 10 kilohm, relays K18A and K20A are reset.

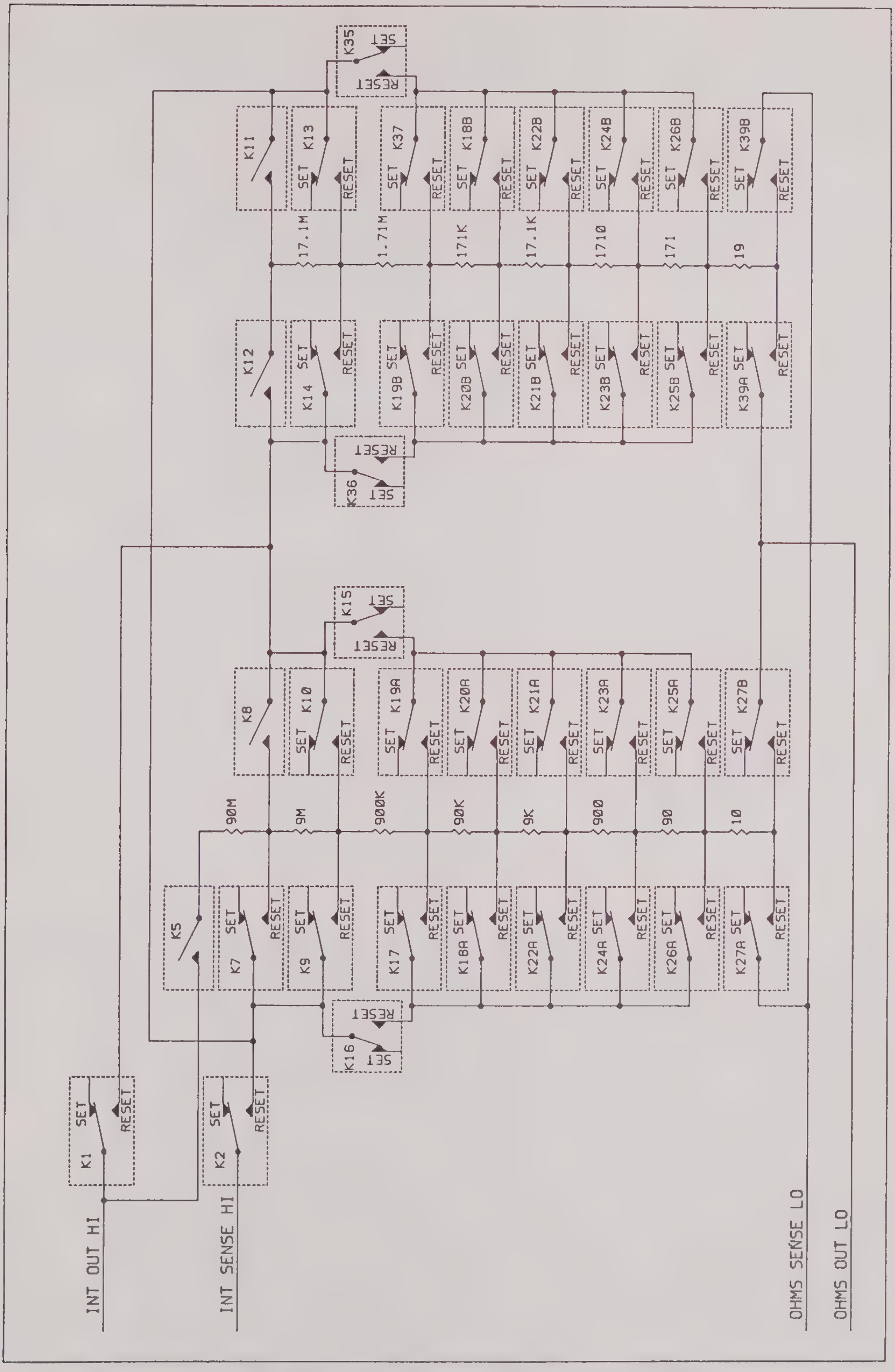

K35
SET
RESET
K11
K13
K37
K18B
K22B
K24B
K26B
K39B
17.1M
1.71M
171K
17.1K
1710
171
19
K12
K14
K19B
K20B
K21B
K23B
K25B
K39A
K36
K15
K8
K10
K19A
K20A
K21A
K23A
K25A
K27B
90M
9M
900K
90K
9K
900
90
10
K5
K7
K9
K17
K18A
K22A
K24A
K26A
K27A
K16
K1
K2
INT OUT HI
INT SENSE HI
OHMS SENSE LO
OHMS OUT LO

Figure 2-29. Ohms Main Assembly Simplified Schematic

The 19 megohm value is selected by K11 and K12 (energized), and the 1.9 megohm value by K13 and K14 (reset). Selection of 1.9 decades below 1.9 megohm is done by K35 and K36 (reset) plus a pair of relays from K18B through K26B and K37.

Two lines, OHMS OUT HI and OHMS SENSE HI, are brought over to the Ohms Cal assembly to connect to 1 ohm, 1.9 ohm, and short. These lines also access resistance values during calibration. Relay K29 connects OHMS OUT HI to the $1x10^n$ string when set, and to the $1.9x10^n$ string when reset. Relay K30 connects OHMS SENSE HI to the $1.9x10^n$ string during calibration.

Relays K3, K28, K31-K34, and op amp U1 and its associated components are only used during calibration. Operation of this circuitry is described in the "Calibration" part of the Ohms Cal theory.

Relays K4 and K6 are used during two-wire compensation. This is described in the "Two-Wire Compensation" part of the Ohms Cal theory.

2-171. OHMS MAIN ASSEMBLY SUPPORT OF CURRENT FUNCTION CALIBRATION

To calibrate the current function, the Current assembly routes output current to the Ohms Main assembly, where it is connected through a resistance. Current is determined by measuring the voltage across this resistance. During calibration, half of K38 connects DAC OUT LO to the SENSE LO side of the $1x10^n$ string (Z1 pin 6). The Current assembly generates approximately 60 uA of current on the DAC OUT LO line, which can cause an error during measurement. To prevent this error, half of relay K38 connects the -17S supply through R6 to the DAC OUT LO line. This generates an opposite-polarity 60 uA current to cancel the current from the Current assembly.

2-172. OHMS DIGITAL CONTROL

The Ohms Main assembly is digitally controlled by the 82C55 Programmable Peripheral Interface IC on the Ohms Cal assembly. This IC, under system software control through the guarded digital bus, has three ports generating 24 outputs. PA0-PA7 of port A, PB0-PB3 of port B, and PC0-PC4 of port C are routed on the Motherboard to the Ohms Main assembly. These lines and two decoders in U9 and U10 control nine relay driver ICs, which in turn control 39 Ohms relays. Relay driver U3 drives non-latching relays K5, K6, K8, K11, K12 and K38. Relay drivers U2, U5-U8, and U11-U13 drive the latching relays.

Port A (PA0-PA7) is a common input bus for all relay drivers. IC U9 decodes PB0-PB3 to strobe the latching relay drivers. This signal causes the contents of the data on the input bus to be latched into the latch portion of the selected device. IC U10 decodes PC0-PC3 to provide four enable lines. Each line goes to two latch/drivers and when true (0V), drives the relay coils on or off according to the contents of the latch. Since these are latching relays, they are pulsed only briefly. The latching relays each have two coils, one to set the relay and one to reset it. When the ohms function is not being used, all relays are set, as shown on the schematic.

PC4 is the strobe line for non-latching relay driver U3. The enable is connected to LH COM so the relays receive constant drive. These non-latching reed relays are shown in the non-energized state.

2-173. Ohms Cal Assembly (A9)

The Ohms Cal assembly (A9) contains the 1 ohm, 1.9 ohm, and short resistance values. It also contains a digital control circuit, and a two-wire compensation circuit to allow accurate calibration of two-wire ohmmeters. A differential amplifier circuit and a 2/5/10V source circuit are used during calibration of the ohms function.

2-174. OHMS CAL DIGITAL CONTROL

The heart of the Ohms Cal assembly digital control circuit is the 82C55 Programmable Peripheral Interface IC (U11) mentioned previously under "Digital Control". This IC has three ports generating 24 outputs. These outputs control seven 5801 latching relay drivers ICs (U14-U20), a 4051 analog multiplexer (U21) for self diagnostics, and several FET switches.

Port A (PA0-PA7) is a common input bus for latching relay drivers and multiplexer U21. These lines also go to the Ohms Main assembly as previously described to control relay drivers there.

Lines PB0-PB3 of port B goes to decoder U12 (PB3 is inverted by U22) and to the Ohms Main assembly. The output of U12 strobes latch/driver ICs to latch data on input bus lines.

Lines PC0-PC3 of port C go to decoder U13 and to the Ohms Main assembly. Decoder U13 enables two latch/driver ICs at a time. Setting the enable true (0V) causes the relay coils to be driven on or off depending on the contents of the latch portion of the selected ICs. Since these are latching relays, they are pulsed only briefly.

The outputs PB4, PB5 and PB6 of U11 are connected to the gates of FETs Q2, Q3 and Q4 respectively. The Programmable Peripheral Interface IC turns them on for a one (5V) and off for a zero (0V). PB7 is connected to the base of Q6 through R31. When PB7 is true (5V), it turns on Q6, which turns on Q5, which in turn supplies +17S to U6. PC4 goes to the Ohms Main assembly where it strobes relay latch/drivers for the non-latching relays.

Line PC6 goes to the diagnostic circuit where it enables and disables output from the multiplexer (U21). Connected to the input of the multiplexer are five voltage dividers made from resistors in Z3 and Z4.

Two inputs to these dividers are connected. One is 10V OUT HI from the 2/5/10V source circuit. The other is 2W COMP from the two-wire compensation circuit. These inputs are connected to the SDL line by the multiplexer, where they are routed to the adc circuit on the DAC assembly and measured during calibrator diagnostics. PC7 is not used.

2-175. 1, 1.9, AND SHORT RESISTANCE

Although located on the Ohms Cal assembly, the 1 ohm value, 1.9 ohm value, and short operate as part of the Ohms Main assembly, filling out the range of values available to the operator. The 1 ohm value is made of four 4 ohm wirewound resistors in parallel (R41). The 1.9 ohm value is made of two 3.8 ohm wirewound resistors in parallel (R42). Relays K4 and K5 connect the 1 ohm and 1.9 ohm values to OHMS OUT HI and OHMS SENSE HI. Relays K6 and K30 connect them to OHMS OUT LO and OHMS SENSE LO. Relays K7 and K8 select the short.

The Ohms Cal assembly contains the relays that switch the low side of the selected resistance onto the output bus. (High sides are connected to the output bus by relays on the Ohms Main assembly.) Relay K24 connects OHMS OUT LO to OUT LO and K25 connects OHMS SENSE LO to INT SENSE LO.

2-176. TWO-WIRE OHMMETER COMPENSATION CIRCUIT

Refer to Figure 2-30 for the following discussion. The Ohms Cal assembly contains a two-wire lead drop compensation circuit that allows accurate calibration of two-wire ohmmeters. The error normally encountered when calibrating a two-wire ohmmeter is due to the voltage drop in the path resistance between the meter and the calibration resistor. This circuit reduces the voltage drop to an insignificant level.

2-177. Two-Wire Compensation Power Supplies

The floating supplies for U7 and U8 consist of a dc-to-dc converter made up of U6, T1 and associated components. Switching-regulator control IC U6 switches +17S through the primary of T1 at about 30 kHz as determined by R27 and C21. The switching creates high-frequency spikes on the +17S line which are filtered out by L2, R25, C18, C19, C20, and C52. When the two-wire compensation circuit is not in use, control line PB7 turns Q5 and Q6 off, which removes +17S, switching off U6. The secondary of T1 is rectified and filtered by CR1, CR2, CR9, CR10, C22, and C23. The voltage is then regulated by 8.2V zener diodes VR1 and VR2. Additional filtering is provided by L3, L4, R43, R44, C24, and C25. Two capacitors (C53 and C54) between A COM and S COM reduce switching noise that would otherwise appear across the calibration resistor.

2-178. High Side Cancellation

The high side voltage drop is eliminated by U7 and U8. Chopper-stabilized op amp U7 and buffer amplifier U8 supply up to 10 mA. The current from the high side of the ohmmeter being calibrated enters at the OUTPUT HI binding post, goes through K1 and K6 on the Ohms assembly, and is routed to the Ohms Cal assembly where it connects to A COM. The A COM connection is a common for the floating supply that powers U7 and U8. The current then flows out of U8 through 500 ohm in Z2 and through K29 to the calibration resistor via the OHMS OUT HI line.

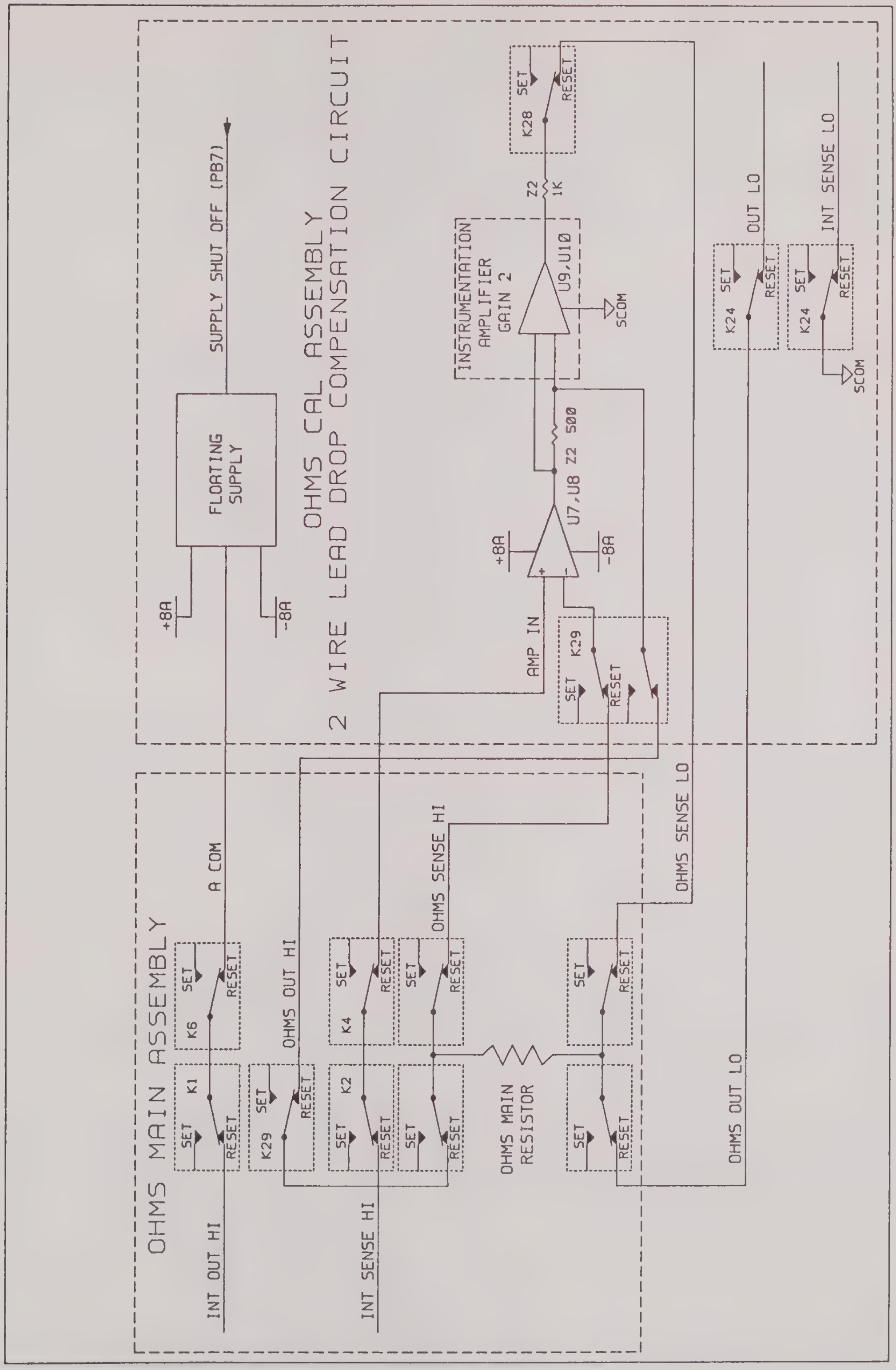

OHMS MAIN ASSEMBLY
INT OUT HI
INT SENSE HI
K1
K6
K29
K2
K4
SET
RESET
A COM
OHMS OUT HI
OHMS SENSE HI
OHMS MAIN RESISTOR
OHMS SENSE LO
OHMS OUT LO
OHMS CAL ASSEMBLY
2 WIRE LEAD DROP COMPENSATION CIRCUIT
FLOATING SUPPLY
+8A
-8A
SUPPLY SHUT OFF (PB7)
AMP IN
U7,U8
Z2 500
INSTRUMENTATION AMPLIFIER GAIN 2
U9,U10
SCOM
Z2 1K
K28
K24
OUT LO
INT SENSE LO

Figure 2-30. Two-Wire Lead Drop Compensation Circuit

K29 connects the -input of U7 to the sense point of the calibration resistance via OHMS SENSE HI. Relays K2 and K4 on the Ohms Main assembly connect the +input of U7, AMP IN, to INT SENSE HI. Relays on the Motherboard connect INT SENSE HI to the OUTPUT HI binding post. Connected this way, U7 controls the voltage at the output of U8 so that the voltage at the input of U7 stays zero. This forces the voltage drop in the path to zero. Diodes CR3-CR6 and resistor R45 provide protection for U7.

2-179. Low Side Cancellation

The voltage drop in the low side path is cancelled by current from high current op amp U9. U9 is driven by dual FET input op amp U10. The two non-inverting inputs of U10 are connected across the 500 ohm resistor in Z2. This enables U10, in conjunction with the four 10K resistors in Z2, to sense the current in the high side path and to supply (through U9 and the 1 kilohm resistor in Z2) a current equal but opposite to the current through the low side path. This cancels the drop in that path. This cancelling current goes through relay K28A to the low sense point of the calibration resistor via OHMS SENSE LO. From there it goes through the output low path to the OUTPUT LO binding post and then through the sense low path back to the Ohms Cal assembly and through K28B to S COM.

2-180. OHMS CALIBRATION

The remaining circuitry is used only for calibration of the resistor values. All values except 1 ohm and 1.9 ohm are calibrated using a single external 10 kilohm resistance standard connected to the binding posts. The 1 ohm and 1.9 ohm values are calibrated using an external 1 ohm standard. How to do the procedure is described in Section 7 of the Operator Manual.

2-181. Calibrating to the External 10 Kilohm Standard

Refer to Figure 2-31 for the following discussion. The first step in ohms calibration is to compare the 10 kilohm standard against the 10 kilohm value on the Ohms Cal assembly. This is done by passing a current through both values and measuring the voltage drop across each. The ratio of the voltages is equal to the ratio of the resistances.

The source of current comes from the 2/5/10V source circuit, which contains U1, Q1, Q2, Q3 and Z1. The buffered 13V reference voltage from the DAC assembly (A11) is switched through K9 to a voltage divider made up of resistors in Z1.

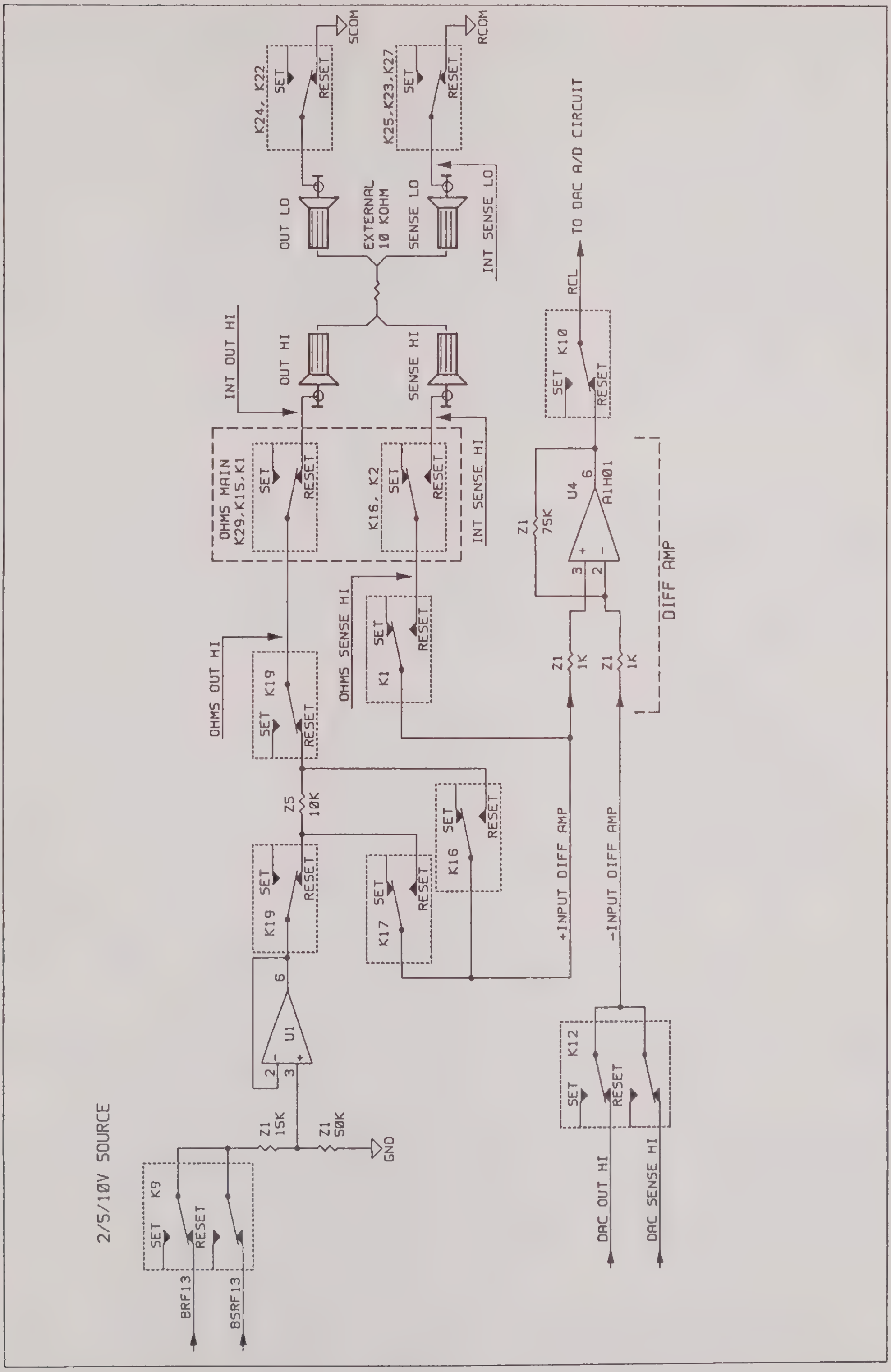

SCOM
RCOM
K24, K22
SET
RESET
K25,K23,K27
SET
RESET
OUT LO
EXTERNAL
10 KOHM
SENSE LO
INT SENSE LO
TO DAC A/D CIRCUIT
RCL
K10
SET
RESET
INT OUT HI
OUT HI
SENSE HI
OHMS MAIN
K29,K15,K1
SET
RESET
K16, K2
SET
RESET
INT SENSE HI
Z1
75K
U4
6
A1H01
3
2
+
-
DIFF AMP
OHMS SENSE HI
K1
SET
RESET
OHMS OUT HI
K19
SET
RESET
Z1
1K
Z1
1K
Z5
10K
K16
SET
RESET
K19
SET
RESET
K17
SET
RESET
+INPUT DIFF AMP
-INPUT DIFF AMP
U1
6
2
3
K12
SET
RESET
2/5/10V SOURCE
K9
SET
RESET
Z1
15K
Z1
50K
GND
DAC OUT HI
DAC SENSE HI
BRF13
BSRF13

Figure 2-31. Calibration to an External 10 Kilohm Standard

To calibrate the 10 kilohm resistance, control lines PB4 and PB5 turn off FETs Q2 and Q3 respectively. In this mode, the output of the divider uses the 15 kilohm and 50 kilohm values to produce an output of 10V. This voltage is buffered by U1 and Q1. The current from this source, 10V OUT HI, is sent through K19 to one side of the 10 kilohm resistance in Z5. 10V SENSE HI is connected to 10V OUT HI by K31A on the Ohms assembly. The other side of the 10 kilohm resistance in Z5 is connected to OHMS OUT HI by K19. This is routed to the Ohms Main assembly where is goes through K29, K15 and K1 to INT OUT HI, which is connected to the OUTPUT HI binding post by relays on the Motherboard. From there it goes through the external 10 kilohm standard and back in through the OUTPUT LO binding post and over to the Ohms Cal assembly where it connects to S COM through K24 and K22.

The voltage drops are measured by comparing each voltage to the DAC assembly output in a differential amplifier circuit made of U2 through U5.

Since the DAC and differential amplifier are referenced to R COM, this line is brought out through K27, K23 and K25 to INT SENSE LO. This is connected to the SENSE LO binding post (which is connected to the sense low point of the standard). Line DAC OUT LO is tied to S COM by relay K31. The high side of the DAC, DAC OUT HI and DAC SENSE HI, are tied together and connected by K12 to U2, which is the differential amplifier -input.

The voltage to be measured is connected to U3, which is the differential amplifier +input. The output of U2 and U3 goes to U4 through gain setting resistors in Z1. These set the gain of the differential amplifier to 75. The differential amplifier generates a current through the 1 kilohm (pins 1-2) and 75 kilohm (pins 2-3) resistors in Z1 to R COM. This current on R COM can cause an error during measurement. Op amp U5, configured as an inverting amplifier, generates an equal current of opposite polarity through 76 kilohm resistor R18 to cancel the current from the differential amplifier. The output of U4 goes through K10 to the RCL line. This line is connected to the DAC assembly, where it goes through an amplifier to the adc circuit.

The calibration program uses the adc circuit to measure the differential amplifier output voltage. First the differential amplifier offset voltage is determined. (This offset is different for each input condition.) Readings are taken to determine each offset voltage by checking the output of the differential amplifier at equal voltages on the inputs. This is done by switching K11 to the reset position to connect the differential amplifier +input and -input together, then measuring the output with the DAC's adc circuit.

Once the offsets are known, the software determines the calibration voltages by adjusting the DAC output until the adc reading is the same as the offset. At that point, the DAC output equals the voltage being measured.

Three readings are required to determine the ratio of the two resistances. For the first reading, K16 connects the differential amplifier +input to the 10 kilohm resistor in Z5. For the second reading, K17 connects the +input to the other side of that resistor. Subtracting the first reading from the second gives the voltage across the internal 10 kilohm. For the third reading, K1 on the Ohms Cal assembly connects the + input to OHMS SENSE HI. OHMS SENSE HI is connected to INT SENSE HI by K16 and K2 on the Ohms Main assembly. INT SENSE HI is connected to the SENSE HI binding post by relay K2 on the Motherboard which is the sense high side of the 10 kilohm external standard. The ratio of this third reading to the difference of the first two readings is proportional to the ratio of the two resistances. Thus by knowing the resistance of the external standard, the software can calculate the value of the internal 10 kilohm resistance value.

2-182. Calibrating 10 kilohm and 19 kilohm

The next step in calibrating the ohms function is to determine the 10 kilohm and 19 kilohm values on the Ohms Main assembly. This is done just like the 10 kilohm value on the Ohms Cal assembly, except the 10 kilohm resistance on the Ohms Cal assembly acts as the standard and is placed in series with 10 kilohm or 19 kilohm on the Ohms assembly.

This is done using K19 on the Ohms Cal assembly and K29, K20A and K27 on the Ohms Main assembly for the 10 kilohm, and K29, K20B and K39 for the 19 kilohm value. The source on the Ohms Cal assembly again outputs 10V. Again three readings are taken. The first and second are the same as previously described. For the third reading, the differential amplifier +input is connected through K1 on the Ohms Cal assembly and through K18A on the Ohms Main assembly for 10 kilohm and K30 and K18B for 19 kilohm. The software then calculates the 10 kilohm and 19 kilohm values using the ratio of readings and the known value of the 10 kilohm on the Ohms Cal assembly.

2-183. Calibrating 100 kilohm

Once the 10 kilohm value is determined, the 100 kilohm value is calibrated by comparing its value against 10 kilohm. The 10V source is connected across 100 kilohm. Since the 10 kilohm resistance is used as part of 100 kilohm, the current goes through both.

Relays K33 and K19A on the Ohms Main assembly connect 10V OUT HI to 100 kilohm. Relays K23 and K27 on the Ohms Cal assembly connects OHMS SENSE LO to RCOM. OHMS OUT LO, DAC OUT LO, and 10V SENSE LO are connected to SCOM. Relay K22 on the Ohms Cal assembly connects OHMS OUT LO to SCOM. OHMS OUT LO is connected to DAC OUT LO by K31 on the Ohms Cal assembly, and to 10V SENSE LO by K31B and K28 on the Ohms Main assembly.

Only two readings are required because this time there is no path resistance to subtract out. DAC OUT HI and DAC SENSE HI are tied together and connected to the -input of the differential amplifier by relay K12.

For the first reading, the +input of the differential amplifier is connected to the sense side of the 100 kilohm point in the string through K1 on the Ohms Cal assembly and K17 on the Ohms Main assembly. For the second reading, the + it is connected to the 10 kilohm point by K18A. The software calculates the 100 kilohm value from the ratio of the readings and the known 10 kilohm value.

2-184. Completion of High Resistance Value Calibration

Once 100 kilohm is determined, 1 megohm and the other values up to 100 megohm are determined in a similar way. Using the same techniques, 190 kilohm is calibrated against 19 kilohm, and so forth up to 19 megohm.

Too much current noise is generated by U3 in the differential amplifier circuit for accurate calibration of resistances above 1 megohm. For these values, U1 on the Ohms Main assembly (a low-bias current FET op amp) is switched ahead of U3.

The 1 kilohm and 1.9 kilohm resistance values are determined from the 10 kilohm and 19 kilohm respectively. The resistance values of the 100 ohm and 190 ohm use the same technique, but using 5V instead of 10V from the 2/5/10V source circuit. To get 5V, Q2 is turned on to parallel the 11.535 kilohm value in Z1 with the 50 kilohm value.

The 10 ohm and 19 ohm resistance values are determined using 2V from the 2/5/10V source and using internal 10:1 divider (Z5) in conjunction with the DAC. To get 2V, Q2 and Q3 are both turned on, which parallels both the 11.535 kilohm value and the 3.846 kilohm value with the 50 kilohm value. The lower voltage is required to lower the power dissipation in the resistors.

Using 2V presents a problem for the DAC. Instead of working at 10V and 1V, it would be working at 2V and 0.2V. This level is too low to get accurate results from the DAC. To solve this problem, the DAC is used only at 2V and the 0.2V level is achieved using a 10:1 divider. The DAC calibrates this 10:1 divider at 10V and 1V. The divider is made of a 90 kilohm and a 10 kilohm resistor in Z5. To calibrate the divider, 10V is applied to the top of the divider through K18. The low side of the divider is connected to R COM (K21 and K27), DAC OUT LO (K21) and S COM through K20 on the Ohms Cal assembly, K27A/B on the Ohms Main assembly and K22 on the Ohms Cal assembly. Two readings are taken. Their ratio is equal to the division ratio of the divider. The -input of the differential amplifier is connected to the DAC output by K12. For the first reading, K15 connects the top of the divider to the +input of the differential amplifier. For the second reading, K16 connects the divider point to the +input of the differential amplifier. The exact ratio of this divider can now be determined by these two readings.

Refer to Figure 2-32 for the following discussion. To calibrate the 10 ohm resistor, the DAC output is connected to the top of the divider by K14. The 2V source is connected across 100 ohm on the Ohms Main assembly. This is done by 10V OUT HI, set to 2V, connected to the high side of the 100 ohm string by K33 and K23A on the Ohms Main assembly. Line 10V SENSE HI is also connected to this point by K31A and K32A on the Ohms assembly. Line OHMS OUT LO and OHMS SENSE LO are connected to the low side of the 100 ohm string by K27B and K27A respectively. Line OHMS OUT LO is connected to SCOM by K22 on the Ohms Cal assembly and is also connected to 10V SENSE LO by K32B and K31B on the Ohms Main assembly. OHMS SENSE LO is connected to the low side of the internal divider by K20 on the Ohms Cal assembly. The Ohms Cal assembly also connects RCOM to the low side of the divider by K27 and K21. Relay K21 also connects this point to DAC OUT LO.

Two measurements are taken. The first is with the +input of the differential amplifier connected to the DAC output through K15. The -input is connected to the sense point of the 100 ohm resistance by K24A on the Ohms Main assembly and K2 on the Ohms Cal assembly. The DAC is adjusted until its value is the same as the voltage across 100 ohms. Then the inputs of the differential amplifier are moved. The +input is connected to the divider output on the Ohms Cal assembly by K16. The -input is connected to the sense point of the 10 ohm resistance by K26A on the Ohms Main assembly and K2 on the Ohms Cal assembly. The DAC is again adjusted until the voltages are equal. The differential amplifier sees 0.2V on each input for this measurement but the DAC is at 2V. The value of 10 ohm is determined from the two DAC settings and the division ratio of the divider on the Ohms Cal assembly. The same procedure is used to determine the 19 ohm value from the 190 ohm value.

2-185. Calibrating to the External 1 ohm Standard

The 1 ohm and 1.9 ohm resistor values are calibrated by comparing them against a 1 ohm external standard. The technique used is different from that used for the 10 kilohm external standard.

The Current assembly supplies a 130 mA (65 mA for 1.9 ohm calibration) current through both resistors. This current goes out the OUTPUT HI binding post to the 1 ohm standard. It comes back in through the OUTPUT LO binding post and through the internal 1 ohm resistance by K26 and K6, or 1.9 ohm by K26 and K30 before going to S COM through K22.

For the first reading, the inputs to the differential amplifier are connected across the sense points of the 1 ohm standard. Relay K1 connects the differential amplifier +input to OHMS SENSE HI, which is connected to INT SENSE HI by K16 and K2 on the Ohms Main assembly. INT SENSE HI is connected to the SENSE HI binding post by relays on the Motherboard. Relay K13 connects the differential amplifier -input to INT SENSE LO which is connected to SENSE LO binding post by relays on the Switch Matrix assembly.

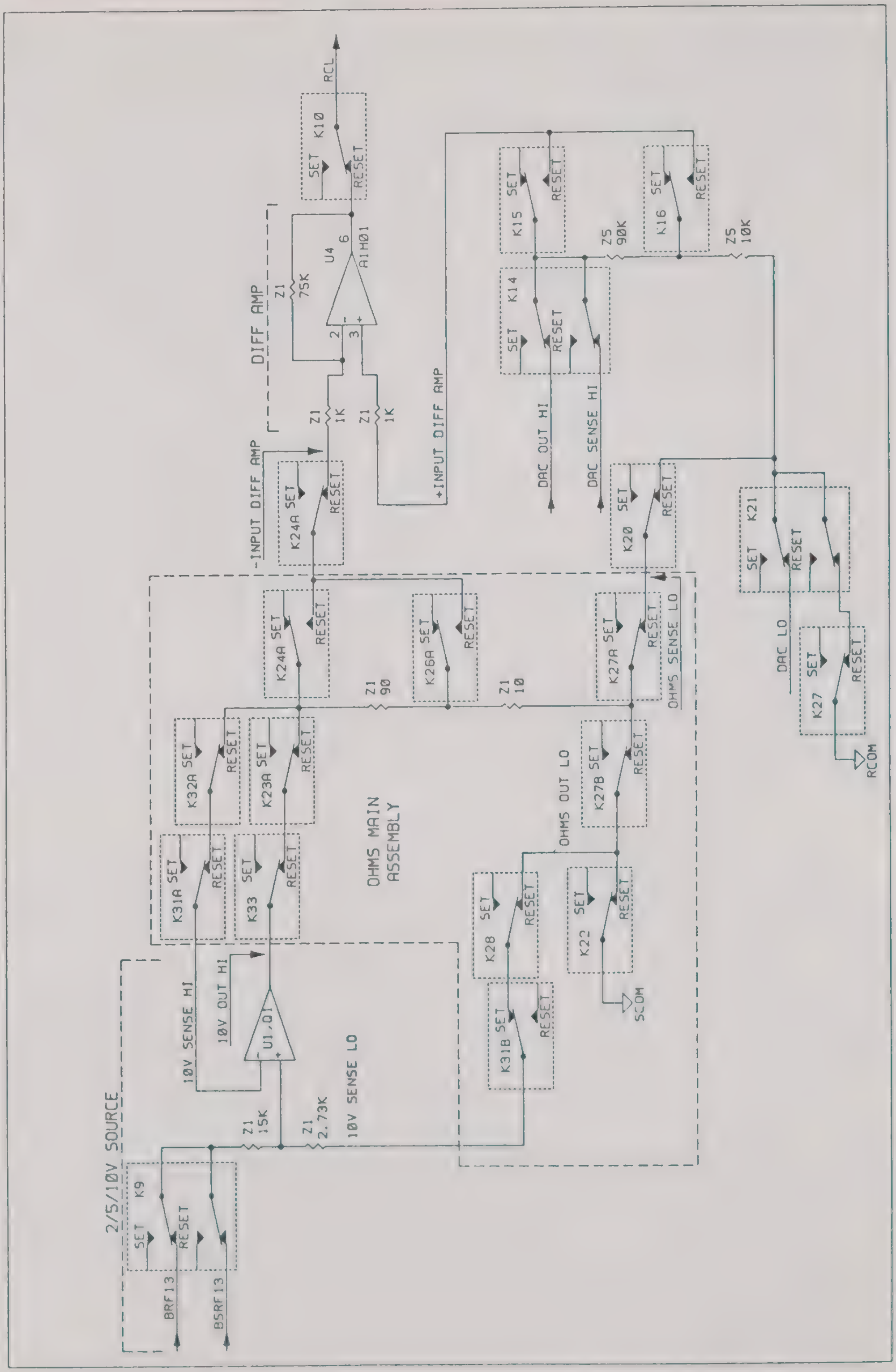

RCL
K10
SET
RESET
DIFF AMP
Z1
75K
U4
6
A1H01
2
3
Z1
1K
Z1
1K
-INPUT DIFF AMP
+INPUT DIFF AMP
K24A
K15
K16
K14
Z5
90K
Z5
10K
DAC OUT HI
DAC SENSE HI
K20
K21
DAC LO
K27
RCOM
K24A
K26A
K27A
Z1
90
Z1
10
OHMS SENSE LO
K32A
K23A
K31A
K33
OHMS MAIN ASSEMBLY
K27B
OHMS OUT LO
K28
K22
SCOM
K31B
10V SENSE HI
10V OUT HI
U1,Q1
10V SENSE LO
Z1
15K
Z1
2.73K
2/5/10V SOURCE
K9
BRF13
BSRF13

Figure 2-32. Ratio Calibration, 10 ohm From 100 ohm

The voltage between the inputs is 0.13V, which is amplified by 75 by the differential amplifier to approximately 9.75V and sent to the DAC assembly on the RCL line. Another differential amplifier on the DAC assembly compares the 9.75V to the DAC output. Before the reading is taken, however, amplifier offsets are determined.

When the DAC output equals the output of the differential amplifier on the Ohms Cal assembly, the reading is stored and a second reading is taken. For this reading, the inputs to the differential amplifier on the Ohms Cal assembly are connected across the 1 ohm or 1.9 ohm on the Ohms Cal assembly. The +input of the differential amplifier is connect through K1 and K4 and the -input is connected through K2 and FET Q4. The second reading is taken the same way as the first. The ratio of the two DAC settings are equal to the ratio of the values of the two resistors. The value of the 1 ohm and 1.9 ohm resistors are determined from this ratio and the value of the external standard.

2-186. Current/High Resolution Oscillator Assembly Overview (A7)

The Current/Hi-Res (High-Resolution Oscillator) Assembly combines two functions on one circuit board. The Current section generates dc and ac currents in the range of 20 uA to 220 mA. The Hi-Res section generates a high-resolution signal accurate in frequency to 4-1/2 digits, which is used by the phase-locked loop circuit on the Oscillator Output assembly (A13). These two functions are independent circuits except for the sharing of some digital controlling and self-diagnostic monitoring. The following theory describes the digital control circuitry used by both circuits, then independently covers the Current and Hi-Res functions.

2-187. CURRENT/HI-RES DIGITAL CONTROL

The heart of the Current/Hi-Res assembly digital control circuitry is a 82C55 Programmable Peripheral Interface IC (U7), which is under software control via the guarded digital bus. This IC has three ports which generate 24 outputs. These outputs control three UCN5801 latching relay drivers ICs (U8-U10), a UCN5800 relay driver (U11) for controlling non-latching relays, a 4051 analog multiplexer (U12) for self diagnostics, and several FET switches throughout the assembly. Port A (PA0-PA7) is a common input bus called CONTROL BUS on the schematic. This CONTROL BUS transmits the desired state of all the relays (K1-K17) in the Current section, and also to control two synthesizer ICs (U16, U17) in the Hi-Res section.

Four relay driver ICs drive latching controlling relays K1-K13 and K16. The CONTROL BUS (port A of U7) is a common input bus. Port C of U7 (PC0-PC5) provides the strobe and enable lines for these relay drivers. PC0 enables U8, while PC1 enables U9 and U10. PC2, PC3, PC4, and PC5 strobe U11, U8, U9, and U10 respectively.

Relay driver U11 controls the three non-latching relays K14, K15, and K17 on this assembly. It also generates control line RLY11* to control K11 on the Motherboard. Relay K11 routes I-GUARD, described later, to the rear panel for operation when the rear-panel binding posts are in use.

The diagnostic circuit allows the calibrator to monitor five points on the assembly. Points DUMMY LOAD, OVEN TEMP, and CUR/COMP MONITOR are from the Current section. Points HI-RES LOOP and HI-RES CLOCK come from the Hi-Res section. Outputs PB0-PB2 select which point the multiplexer U12 monitors. PC6 enables the output of U12 to the SDL line, where it is measured by the adc circuit on the DAC assembly (A11).

Outputs PB3-PB5 generate control lines FET3, FET1, and FET2 respectively, which are used by the Current section. FET1 controls NMOSFETs Q21 and Q22, FET2 controls Q20 and Q23, and FET3 controls quad CMOS analog switch U5.

Outputs PB6 and PC7 generate control lines HI-RES RANGE and HI-RES ON/OFF respectively, which are used by the Hi-Res section. These lines control quad CMOS analog switch U18 and comparator U13.

2-188. Current Section (A7)

The current section of the A7 assembly uses dc voltage from the DAC assembly and ac voltage from the Oscillator Output assembly to generate both ac and dc current outputs.

Four ranges of output current are generated:

	DC Current	AC Current
220 uA Range:	0 - 219.9999 uA	9.000 uA - 219.999 uA
2.2 mA Range:	0.220000 mA - 2.199999 mA	0.22000 mA - 2.19999 mA
22 mA Range:	2.20000 mA - 21.99999 mA	2.2000 mA - 21.9999 mA
220 mA Range:	22.0000 mA - 219.9999 mA	22.000 mA - 219.999 mA

Each range provides dc or ac current. AC current is available from 40 Hz to 10 kHz.

A 2.2A range is generated on the High Voltage/High Current assembly (A15) and routed to this assembly for switching to the OUTPUT binding posts. This is further described under the heading, "2.2A Range."

The transconductance amplifier, shunt resistors, feedback loop, and complementary drive circuits form a loop to create the output current. In addition to these circuits, the Current assembly contains input switching, output switching, a current guard, and a current/compliance voltage monitor. Each of these circuits is described in detail.
To better understand the theory of operation, refer to Figure 2-33 and the schematic.

2-189. CURRENT INPUT SWITCHING

Relay K1, CMOS analog switch U5B, and FETs Q20-Q23 select the input source voltage. For dc operation, the 22V range of the DAC assembly (A11) is brought in on the B IN and B FB lines from the Switch Matrix assembly (A8). For ac operation, the 22V range of the Oscillator Output assembly (A13) is brought in on the B IN and B FB lines. During calibration of the current functions, the 13V buffered dc reference BRF13 and BSRF13 are selected when K1 is set and U5B is closed.

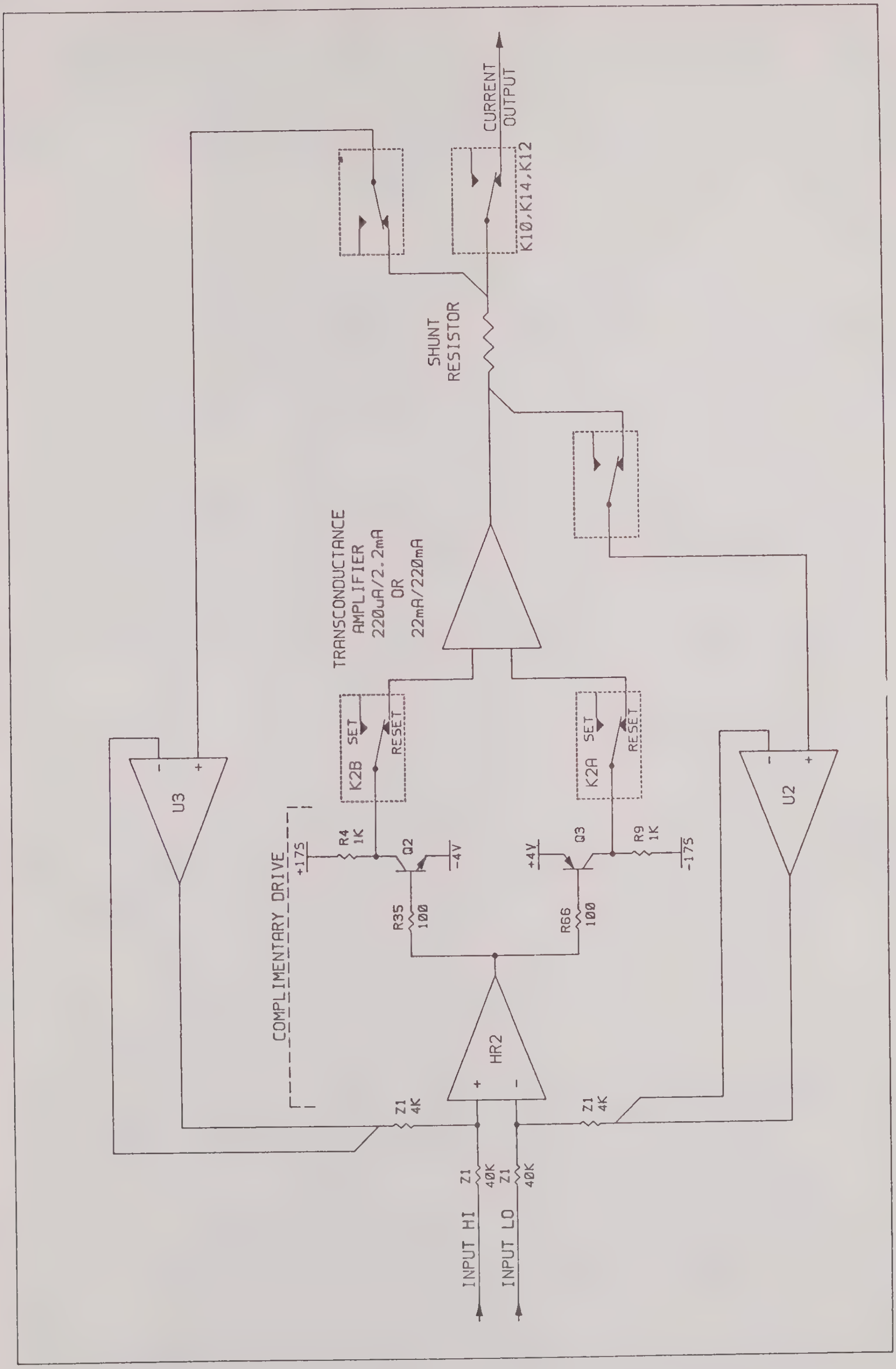

CURRENT OUTPUT
K10,K14,K12
SHUNT RESISTOR
TRANSCONDUCTANCE AMPLIFIER 220uA/2.2mA OR 22mA/220mA
K2B
SET
RESET
K2A
SET
RESET
U3
U2
COMPLIMENTARY DRIVE
+175
R4 1K
Q2
-4V
+4V
Q3
R9 1K
-175
R35 100
R66 100
HR2
+
-
Z1 4K
Z1 4K
Z1 40K
Z1 40K
INPUT HI
INPUT LO

Figure 2-33. Current Output Simplified Schematic

The input signal return paths are selected for ac or dc operation by control lines FET1 and FET2, and NMOSFETs Q20-Q23. With a dc or 13V reference input, control line FET1 goes high, turning on Q21 and Q22, connecting RCOM and DAC OUT LO to the respective circuit. For ac current input, control line FET2 goes high, turning on Q20 and Q23, connecting OSC SENSE LO and OSCOM to the respective circuit.

2-190. COMPLEMENTARY DRIVE CIRCUIT

The circuitry containing transistors Q2, Q3, Q18 and Q19 provides the complementary drive to the output transconductance amplifiers from the single-ended output dc amplifier on hybrid HR2. Transistors Q2 and Q18 provide the drive during a positive input, while Q3 and Q19 provide the drive during a negative input. Relay K2 switches the drive to the 220 uA/2.2 mA transconductance amplifiers when reset, or to the 22 mA/220 mA transconductance amplifier when set.

The HR2 assembly consists of an op amp mounted on a heated-substrate hybrid, bonded to the shunt resistor network. The HR2 assembly gives this circuit excellent dc characteristics of low offset, noise and drift. The hybrid heater control circuit, outlined on page 2 of the schematic, adjusts the base voltage of Q1 to deliver the proper power to the heater resistor. This maintains the HR2 assembly at a constant temperature in spite of environmental temperature variations. Transistor Q14 protects the hybrid in case Q1 fails.

2-191. TRANSCONDUCTANCE AMPLIFIERS

The transconductance amplifiers are the 220 uA/2.2 mA range amplifier and the 22 mA/220 mA range amplifier circuits. The 220 uA and 2.2 mA ranges are provided by the 220 uA/2.2 mA range transconductance amplifier, containing transistors Q4, Q5, and relay K3. With relay K3 reset as shown on schematic, the amplifier is in the 220 uA range. To place the amplifier in the 2.2 mA range, relay K3 is set so emitter resistors R10 and R12 are shunted by R11 and R13 respectively.

The the 22 mA/220 mA range transconductance amplifier contains transistors Q6-Q13 and relay K4. It provides the 22 mA and 220 mA ranges. In the 22 mA range, the transconductance amplifier is composed of Q6-Q9 with K4 in the reset position. In the 220 mA range, the transconductance amplifier is composed of Q6-Q13 with K4 in the set position. In this range, Q10-Q13 are in the Darlington configuration with Q6-Q9 respectively. This provides the additional current gain needed for the 220 mA range.

2-192. SHUNT RESISTORS

A resistor network is used to sense the output current in each of the four current ranges. This network is composed of four four-terminal resistors attached to the heated substrate of HR2. The shunt resistors are 10 kilohm for the 220 uA range, 1 kilohm for the 2.2 mA range, 100Q for the 22 mA range, and the 10 ohm for the 220 mA range. Relays K5-K9 select the INPUT, OUTPUT, and SENSE binding posts for each of the four ranges as Table 2-14 shows:

Table 2-14. Relay Settings for Current Range Selection

RELAY	RANGE			
	220 uA	2.2 mA	22 mA	220 mA
K5	R	S	S	S
K6	R	S	R	R
K7	R	S	R	R
K8	R	R	S	R
K9	R	R	R	S

S=SET R=RESET

2-193. FEEDBACK LOOP

The output current develops a 2.2V full-scale voltage across the appropriate shunt resistors. Buffer amplifiers U2 and U3 isolate the shunt from the remaining feedback circuit. The negative feedback buffer is op amp U2 configured as a voltage follower. The positive feedback buffer is made of U3 configured as a voltage follower.

Both the feedback voltage from U2 and U3, and the input voltage from K1 and Q20-Q23 are applied to the precision dual 10:1 matched voltage divider network Z1. Any voltage difference between the two halves of the network is amplified by the dc amplifier on the heated substrate hybrid HR2. This amplified dc is applied to the complementary drive circuit and in turn to the transconductance amplifiers to complete the feedback loop.

Therefore, with a 22V full scale input and the 10:1 divider, the voltage across the shunt network is forced to 2.2V by the feedback loop. The 2.2V across the shunt is developed by the full-scale output current on any of the four ranges. By programming the input voltage over a 10:1 range, the output current follows with a 10:1 range. By switching the shunt resistors, four 10:1 ranges give a total output range of 20 uA to 220 mA.

2-194. CURRENT OUTPUT SWITCHING

Relays K10-K15 switch the output current for the various modes of operation required by this assembly. When K13 is reset, it switches in a dummy load (R14) to prevent transients during switching, and also for use during diagnostics. Non-latching relay K15 connects the return lines to the output whenever an output is called for. Non-latching relay K14 connects the output signal to latching relay K12. Relay K12 switches the output to the AUX CURRENT OUTPUT binding post while in the reset position, or to the OUTPUT HI binding post while in the set position.

The four ranges of output current can be connected to the B CUR line by relay K11. B CUR is routed to the rear-panel 5725A connector. This allows all current ranges to be available from the binding posts on the 5725A Amplifier if so selected by the operator.

2-195. GENERATION OF THE 2.2A RANGE

To generate the 2.2A range, the Current assembly is set to the 22 mA range with its output directed to the High Voltage/High Current assembly (A15). This connection is made via the IHV line by relay K10 in the set position. The High Voltage/High Current assembly amplifies current by 100 to create the 2.2A range. This high current output is returned to the Current assembly via the B CUR line. Relay K11 in the set position directs it to the output relays, K12-K15, of the Current assembly.

During internal calibration of the 2.2A range, the Current assembly is set to the 22 mA or 2.2 mA range and directed to the High Voltage assembly in the same manner as previously described.

Internal calibration of the 2.2A range and gain of the High Voltage/High Current assembly is discussed further in the theory for the High Voltage assemblies.

2-196. CURRENT GUARD BUFFER

Buffer amplifier U4, configured as a voltage follower, is used to provide a guard voltage equal to the output voltage across the external load. The guard voltage, if used, prevents any output current from being shunted away from the load due to leakage or shunt capacitance in the system cabling.

2-197. COMPLIANCE LIMITER

A compliance limiter circuit consisting of Q24, Q25, and associated components clamps the output to ±11V during an over-compliance condition.

2-198. CURRENT/COMPLIANCE VOLTAGE MONITOR

The current/compliance voltage monitor circuit, which contains CMOS analog switch U5A, U5C, U5D, op amp U6, and associated components, measures the voltage on either side of the current shunts. This allows the 5700A to detect an over-current or over-compliance condition. A logic low on control line FET3 closes U5A to connect the monitor circuit to the input side of the shunt resistor. The measurement at this point is the sum of the output compliance voltage and voltage drop across the shunt, which is proportional to the output current. A logic high on control line FET3 opens U5C, which allows pull-down resistor R36 to close U5D. This connects the monitor circuit to the output side of the shunt resistor, which gives the output compliance voltage.

Op amp U6 and associated components create an absolute value circuit whose output, CUR/COMP MONITOR, is always a positive dc voltage. During operation in the ac current function U6B generates a negative half-wave signal equal to the positive peaks of its input. Resistors R31 and R30 sum this half-wave signal and the input signal at the input of U6A. Capacitor C14 averages the voltage so the output of U6A is a dc voltage which represents the average value of the selected input.

The diagnostic circuit connects CUR/COMP/ MONITOR to the SDL line, on which it is routed to the DAC assembly (A11) to be measured by the adc circuit. The calibrator software computes the difference between the two measurements and divides the result by the shunt value to determine the output current.

2-199. CURRENT ASSEMBLY CALIBRATION

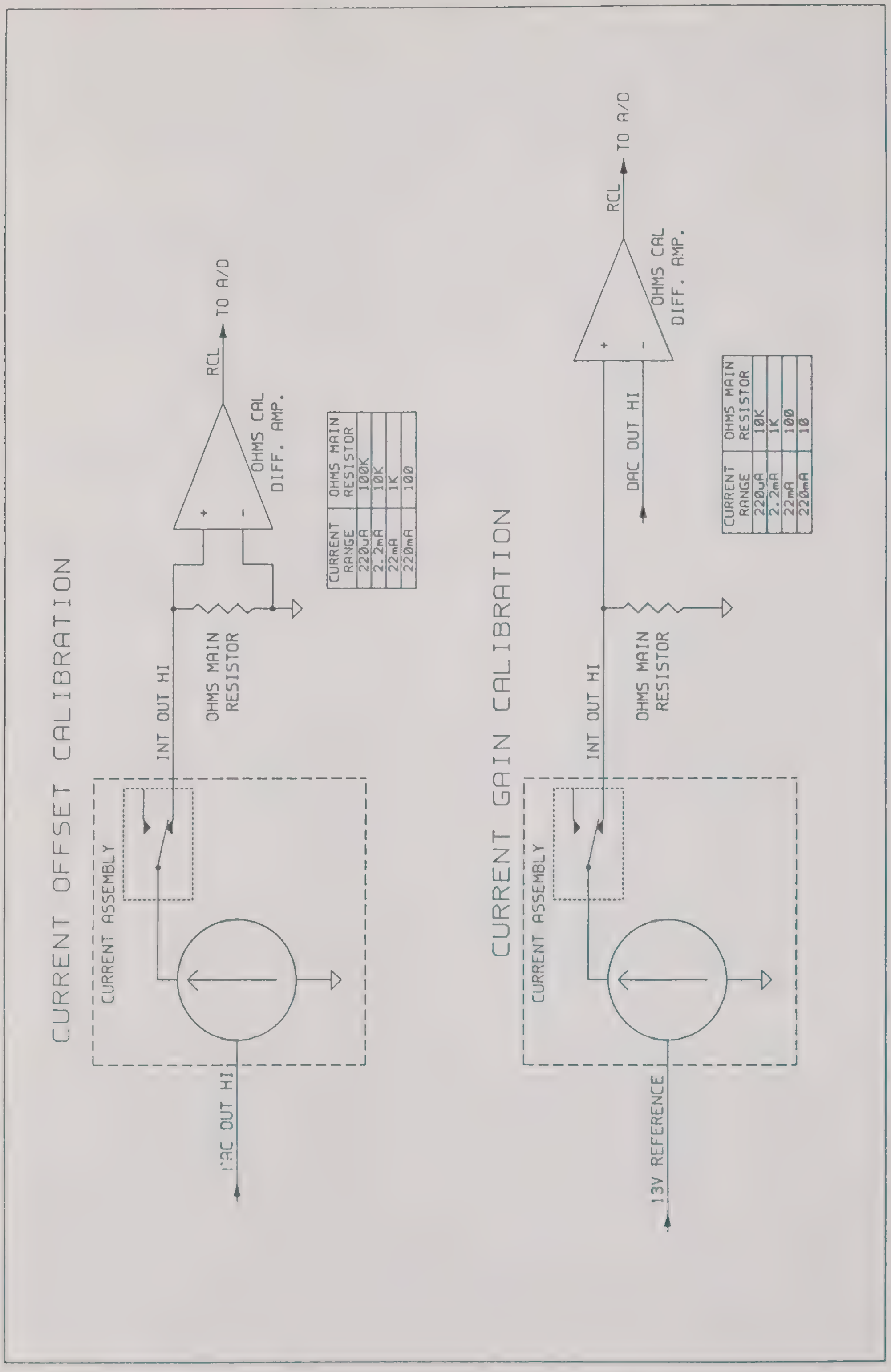
Refer to Figure 2-34 for the following discussion. Internal calibration of the Current assembly is a process of determining the offset and gain constants for each of the four current ranges.

To determine the offset of the 220 mA range, the Current assembly is set to the positive dc 220 mA range with its input from the DAC assembly set to 0V. The output of the Current assembly is routed to the Ohms Main assembly (A10), via INT OUT HI, where it is connected to the previously calibrated 100 ohm resistor.

To get a checkpoint reading, the Current assembly output is removed from the 100 ohm resistor on Ohms (via the output switching relays). The 100 ohm resistor is connected to a differential amplifier on the Ohms Cal assembly (A9). The output of this differential amplifier is connected to RCL, which is routed to the adc circuit on the DAC assembly. The adc circuit measures the voltage, which is the drop across the 100 ohm resistor with no current applied through it. This value is the checkpoint reading and is stored in memory.

The output of the Current assembly is reconnected to the 100 ohm resistor. Next, the DAC assembly, which is the Current input, is adjusted until the adc circuit measures the same reading as the check point.

Gain is determined by connecting the input of the Current assembly to the 13V reference BRF13 and BSRF13 via relay K1. The resulting 130 mA from the Current assembly is routed via INT OUT HI to a previously calibrated 10 ohm resistor on the Ohms Main assembly. The +input of the differential amplifier, located on the Ohms Cal assembly, is connected to one side of this 10 ohm resistor and the -input of the differential amplifier is connected to the output of the DAC assembly. The output of the differential amplifier is connected to the adc circuit in the DAC assembly via the RCL line, and the DAC output is adjusted until a null is achieved. This determines the exact voltage drop across the 10 ohm resistor. The exact gain can now be calculated using this and the previous offset reading.


CURRENT OFFSET CALIBRATION
CURRENT ASSEMBLY
DAC OUT HI
INT OUT HI
OHMS MAIN RESISTOR
+
-
OHMS CAL DIFF. AMP.
RCL
TO A/D
CURRENT GAIN CALIBRATION
CURRENT ASSEMBLY
13V REFERENCE
INT OUT HI
OHMS MAIN RESISTOR
DAC OUT HI
+
-
OHMS CAL DIFF. AMP.
RCL
TO A/D

CURRENT RANGE	OHMS MAIN RESISTOR
220uA	100K
2.2mA	10K
22mA	1K
220mA	100

CURRENT RANGE	OHMS MAIN RESISTOR
220uA	10K
2.2mA	1K
22mA	100
220mA	10

Figure 2-34. Current Assembly Calibration

The current output, now calibrated at dc, is further characterized for its frequency response. The Current assembly is configured to the ac current function with input from the Oscillator Output assembly (A13) set to 20V at a low frequency. The output side of the appropriate shunt resistor is connected to SCOM by relay K17B, and the resulting 2V on the input side of the shunt resistor is connected to the AC CAL line through U22 by relay K17A. The AC CAL signal is routed to the Oscillator Control assembly (A12) where a 400 ohm rms sensor measures the ac voltage on this line. A dc reading of the sensor is taken. It and the Oscillator Output level are stored in memory. The Oscillator Output frequency is then increased and the Oscillator Output level is adjusted, and stored in memory, so the dc reading from the rms sensor is the same as the previous reading. This is repeated at various frequencies up to 10 kHz to characterize the entire frequency response of the ac current output.

2-200. High-Resolution Oscillator Assembly (A7)

The High-Resolution Oscillator supplies a square-wave signal (HI-RES) in the range of 10 Hz to 1.2 MHz with a frequency resolution of 4-1/2 digits. The output signal is routed on the Motherboard P LOCK HI line to the Oscillator Output assembly, where it phase-locks the oscillator.

During calibrator operation using an external phase-lock signal, or during a non-ac operation, the Hi-Res Oscillator is shut off by control line HI RES ON/OFF from the digital control circuit. The hi-res circuitry uses a phase-locked loop circuit containing the reference frequency amplifier/divider, phase detector/divider, loop filter, and vco circuit as outlined on the schematic. A 5-500k divider and output switching circuitry creates the final output frequency. These circuits are described in the following paragraphs.

The Hi-Res Oscillator output is divided into five ranges as shown below:

o	Range 1:	10.00 Hz	to	119.99 Hz
o	Range 2:	0.1200 kHz	to	1.1999 kHz
o	Range 3:	1.200 kHz	to	11.999 kHz
o	Range 4:	12.00 kHz	to	119.99 kHz
o	Range 5:	0.1200 MHz	to	1.1999 MHz

Note that the frequency resolution on each range changes from four digits for outputs of 12 to 99 to five digits for outputs of 100 to 119. For example, the output of range 1 has four digits of resolution from 10.00 Hz to 99.99 Hz and five digits resolution from 100.00 Hz to 119.99 Hz. The range 2 output has four digits resolution from 120 Hz to 990 Hz and five digits resolution from 1000.0 Hz to 1.1999 kHz. The resolution break points are similar for the other ranges.

2-201. REFERENCE FREQUENCY AMP/DIVIDER

A 2 MHz reference frequency is generated by the reference frequency amp/divider circuit as outlined on the schematic. This circuit uses the 8 MHz system clock lines CLK and CLK*, generated by the Guard Crossing assembly (A17). This 8 MHz signal is a low-level clock (200 mV p-p) and it is amplified to 5V p-p by comparator U13A. This 5V 8 MHz clock is turned off when the Hi-Res Oscillator is not being used by control line HI-RES ON/OFF from the digital control circuit and nor gate U15D. The 8 MHz clock is then divided to 2 MHz by flip-flops U14A and U14B to generate 2 MHz REF, which is the reference frequency for synthesizer IC U16. It is filtered by R63 and C49 to generate HI-RES CLOCK, which is monitored by the diagnostic circuit.

2-202. PHASE-LOCKED LOOP

The phase-locked loop circuit contains the phase detector/dividers, loop filter, and vco (voltage-controlled oscillator) circuits as outlined on the schematic.

The phase det/dividers circuit contains synthesizer IC U16. This IC contains two programmable divide-by-n counters and a phase detector. The divide-by-n counters are controlled by inputs from the control bus, which are latched into internal latches on the IC. Information on the control bus is entered and latched into U16 by NOR gate U15A and control lines CS7* and WR*. The first divide-by-n counter is programmed to divide 2 MHz REF by 2000 to give 1 kHz, which is applied to one input of the internal phase detector. The other divide-by-n counter is used to divide the feedback frequency at pin 3, which is generated by the VCO circuit, by 6,010 to 12,000 in one-digit steps, and then apply it to the second input of the phase detector. The loop is locked when the two inputs to the phase detector are the same frequency and phase.

With the 1 kHz reference frequency and the feedback divider programmed between 6,010 and 12,000, the input frequency at pin 3 of U16 must be between 6.010 MHz and 12.000 MHz (1 kHz x 6010 = 6.010 MHz and 1 kHz x 12000 = 12.000 MHz).

Phase detector (U16) outputs ("OV" on pin 14 and "OR" on pin 15) are used by the loop filter circuit, which controls the VCO circuit.
If the divided feedback frequency is greater than the 1 kHz reference frequency, or if the phase of the divided feedback frequency is leading the output, OV pulses low and output OR remains high. If the divided feedback frequency is less than the 1 kHz reference frequency, or if the phase of the divided feedback frequency is lagging the output, then OR pulses low and output OV remains high. When the feedback frequency and the 1 kHz frequency are the same and in phase, the outputs OV and OR both remain high except for a short period when both pulse low in phase. This condition occurs when the loop is locked.

Outputs from the phase detector (OV and OR) are connected to the loop filter circuit which contains the two op amps in U20. U20A and U20B amplify and filter, respectively, any phase difference and apply it to varactor diode CR9 in the vco circuit.

The vco circuit contains varactor diode CR9 and a vco IC U19. The vco frequency is controlled by CR9, which gets its bias voltage from amplifier U20. This circuit is designed to always operate over a 2:1 range from 6 MHz-12 MHz. To lock the loop, amplifier U20 changes the bias on varactor diode CR9.until the divided vco frequency has the same frequency and phase as the 1 kHz reference frequency at the input to the phase detector in U16. Once the loop is locked, the output of the phase-locked loop circuit is between 6 and 12 MHz. This output frequency is connected to the 5-500k divider circuit for further division.

Supply voltage is applied to vco U19 whenever the Hi-Res function is used by the circuitry containing analog CMOS switch U18A, transistor Q15, and zener diode VR3. VCO U19 is energized when control line HI-RES ON/OFF goes low to close U18A, which turns on transistor Q15, connecting zener diode VR3 to the -17LH power supply.

R53 and R54 divide the bias voltage input of the vco circuit to generate the HI-RES LOOP line, which is monitored by the diagnostic circuit.

2-203. 5-500K OUTPUT DIVIDER

The 5-500k output divider circuit contains a synthesizer IC U17 which has a reference (R) divider and a divide by N counter. These dividers are controlled by inputs from the CONTROL BUS which are latched into internal latches on the IC. The information on the CONTROL BUS is entered and latched into U17 by nor gate U15B and Control lines CS13* and WR*. With the phase-locked loop output frequency locked at any frequency between 6 MHz and 12 MHz, divider U17 is programmed to divide by some value between 5 and 500,000 as required to give the correct output frequency. The 6 MHz - 12 MHz input from the phase-locked loop circuit is divided by the reference divider to generate the 24 kHz-2.4 MHz frequency range at pin 18. This divided reference frequency is connected to pin 3 which is the input of the divide by N counter. The divide by N counter does further division to generate the 20 Hz-24 kHz frequency range at pin 15. As an example, an output of 6.7 kHz is in range 3 with the loop locked at 6.7 MHz [the internal divider in U16 was programmed to divide by 6,700 (6,700 x 1 kHz = 6.700 MHz)] and the two dividers in U17 are programmed for a total division of 500 (6.7 MHz/500 = 13.4 kHz). This 13.4 kHz signal is divided in half by the output switching circuit to generate the 6.7 kHz output.

2-204. HI-RES OUTPUT SWITCHING

The output switching circuit contains three analog CMOS switches in U18, and flip-flops in U21. Flip-flop U21A divides the reference divider output of U17 by two to create the 12kHz-1.2 MHz range. Flop-flop U21B divides the divide-by-N counter output of U17 by two to create the 10 Hz-12 kHz range. Control line HI-RES RANGE and NOR gate U15C control the analog CMOS switches U18B and U18C. These switches select the 12 kHz-1.2 MHz or the 10 Hz-12 kHz frequency range, respectively, from the flip-flops. Flip-flop U21A divides this frequency by two. Control line HI-RES ON/OFF and switch U18D connect this output square-wave signal to the P LOCK HI line when the variable phase output function is activated by the operator.

Table 2-15 shows how the dividers are set, the total division of the vco frequency, and the vco frequency. To determine the exact vco frequency, multiply the calibrator output frequency by the number in the total division bracket. For example, the output frequency is set to 42 kHz and the vco frequency is 42k x 200 = 8.4 MHz. Note that the total division includes division by two by U21 in the output switching circuit.

Table 2-15. Divider Settings and VCO Frequencies

CALIBRATOR OUTPUT FREQUENCY @ TP16	U17 R DIVIDER SETTING	U17 N DIVIDER SETTING	TOTAL DIVISION OF VCO @TP13	VCO FREQUENCY @TP13
10 Hz-12 Hz	500	1000	1M	10 MHz-12 MHz
13 Hz-15 Hz	400	1000	800k	10.4 MHz-12 MHz
16 Hz-30 Hz	200	1000	400k	6.4 MHz-12 MHz
31 Hz-60 Hz	100	1000	200k	6.2 MHz-12 MHz
61 Hz-120 Hz	50	1000	100k	6.1 MHz-12 MHz
130 Hz-150 Hz	400	100	80k	10.4 MHz-12 MHz
160 Hz-300 Hz	200	100	40k	6.4 MHz-12 MHz
310 Hz-600 Hz	100	100	20k	6.2 MHz-12 MHz
610 Hz-1.2 kHz	50	100	10k	6.1 MHz-12 MHz
1.3 kHz-1.5 kHz	400	10	8k	10.4 MHz-12 MHz
1.6 kHz-3.0 kHz	200	10	4k	6.4 MHz-12 MHz
3.1 kHz-6.0 kHz	100	10	2k	6.2 MHz-12 MHz
6.1 kHz-12 kHz	50	10	1k	6.1 MHz-12 MHz
13 kHz-15 kHz	400	0	800	10.4 MHz-12 MHz
16 kHz-30 kHz	200	0	400	6.4 MHz-12 MHz
31 kHz-60 kHz	100	0	200	6.2 MHz-12 MHz
61 kHz-120 kHz	50	0	100	6.1 MHz-12 MHz
130 kHz-150 kHz	40	0	80	10.4 MHz-12 MHz
160 kHz-300 kHz	20	0	40	6.4 MHz-12 MHz
310 kHz-600 kHz	10	0	20	6.2 MHz-12 MHz
610 kHz-1.2 MHz	5	0	10	6.1 MHz-12 MHz

2-205. Rear Panel Assembly (A21)

Functional circuitry on the Rear Panel assembly includes a relay control circuit, phase lock in/variable phase out I/O circuit, address mapping, clock regeneration circuit, IEEE-488 interface, RS-232-C interface, interfaces for the 5205A, 5215A, and 5220A amplifiers, and a 5725A Amplifier interface. Three amplifiers can be physically connected to the 5700A: 5725A, 5220A with 5205A, or 5220A with 5215A). Only one can be used at a time. Depending on the amplifier's mode of operation, the output of the 5700A is either an ac or a dc voltage. The following theory of operation describes each of these circuits.

2-206. REAR PANEL POWER SUPPLIES

Power supplies are divided into guarded and unguarded. Unguarded supplies +5V LOGIC, +12V, and -12V are referenced to +5V LOGIC COMMON and are generated on the Digital Power Supply assembly (A19). Guarded supplies +5LH and -5LH are referenced to LH COM, and the supply +5RLH is referenced to RLH COM. These supplies are generated on the Regulator/Guard Crossing assembly (A17). Some ICs on the A17 assembly do not have power and ground pins shown on the schematic. This information is included in the table on page 1 of the Rear Panel schematic.

2-207. REAR PANEL ADDRESS MAPPING

The rear panel decodes address lines from the bus connected to the main CPU through connector P91. Decoding is accomplished with a C22V10 PLD (U8) with the following chip selects:

o RPDUARTCS*	D00000-D0001F
o RPIEEECS*	D00020-D0002F
o Y52XXRD*	D00030-D00031
o Y5205WR*	D00032-D00033
o Y5220WR*	D00034-D00035

2-208. CLOCK REGENERATION CIRCUIT

In order to minimize EMI (electro-magnetic interference) inside the 5700A chassis, the rear panel accepts a low-level (~200 mV p-p sinewave) 3.68 MHz clock from the CPU assembly and conditions it to proper TTL clock levels.

This is done by a differential amplifier, U18, which amplifies the incoming signals 3.6864MHZCLK and 3.6864MHZCLK*. The output of U18 is a TTL level 3.68 MHz clock called RP3.68MHZ that is buffered by PLD U8 creating RPCLK for use by DUART (dual universal asynchronous receiver/transmitter) U5, and IEEE interface IC U2.

2-209. IEEE-488 (GPIB) INTERFACE

The IEEE-488 (GPIB) interface circuit provides the interface between the IEEE-488 connector (J1) and the calibrator processor on the CPU (A20) assembly. The circuitry uses a TMS9914 (U2) General Purpose Interface Bus (GPIB) adapter to meet the requirements for talker/listener operation on the IEEE-488 bus. This circuit translates asynchronous 8 bit data and control information, under control of an external controller, and converts this information to an acceptable format for the CPU. responds.

The TMS9914 has internal circuitry which handshakes in the proper GPIB protocol and stores data in an internal buffer. This IC also has the capability of interrupting the CPU. The CPU can then handle the interrupt through its own handler routine. The data lines between U2 and J1 are buffered by a 75160A (U3) data buffer, and the command lines are buffered by a 75162A (U4) command buffer.

J1 is a standard IEEE-488 connector. The shell of this connector is tied to chassis ground for EMI/RFI shielding.

2-210. RS-232C INTERFACE

The RS-232C interface circuit uses a 68C681 DUART (U5), a 1488 line driver (U6), and a 1489 line receiver (U7).

The DUART does the parallel to serial data conversion and provides two channels of serial RS-232C communication.

The first channel is available to RS-232C connector J2 to meet serial interface needs between the 5700A and the external world. The transmit line (*TXDA) is driven by U6D to TX of J2, pin 2. The receive line RX goes from J2, pin 3 through receiver U7C to the receive line *RXDA of the DUART.

The second channel is connected to the 5725A Amplifier interconnect connector (J7) to provide the 5725A digital control interface to the CPU assembly. Transmit line *TXDB is driven by U6B to B-SCT of J7, pin 18. Receive line B-SCR from J7, pin 17 goes through receiver U7B to the receive line *RXDB of the DUART. These lines are also connected to J10, pins 2 and 3, for internal software testing.

The DUART (U5) also has six input lines, four of which are used to monitor CTSA*, B-CINT*, CAL SWA*, and CAL SWB*. The CTS (clear to send) line from J2, pin 5 goes through receiver U7A becoming CTSA*. Line CAL SWA* comes from the rear panel CALIBRATION switch.

The B-CINT* input (5725A cable interlock) is a logic signal used to let the 5700A know that the interface cable to the 5725A Amplifier is connected and the 5725A is energized.

The DUART (U5) generates four output lines. The first, RTSA*, is driven by U6C to the RTS (ready to send) pin 4 of J2. The remaining three are used in the auxiliary amplifier interface logic circuit.

5220EN* is the output enable for octal latch U10. 5220ADIR* is the output enable for buffer U11. 5205EN* is the output enable for octal latch U9.

2-211. AUXILIARY AMPLIFIER INTERFACE

The Auxiliary Amplifier interface connects the 5700A to a 5205A or 5215A Precision Power Amplifier or the 5220A Transconductance Amplifier. The connection to the 5205A or 5215A is closed loop while the connection to the 5220A is open loop.

Three amplifiers can be physically connected to the 5700A: 5725A, 5220A with 5205A, or 5220A with 5215A). Only one can be used at a time. Depending on the amplifier's mode of operation, the output of the 5700A is either an ac or a dc voltage.

Relays on the Switch Matrix assembly connect OUTPUT HI signal to B IN, SENSE HI to B FB, and INT SENSE LO to B SNSLO, the driving signals for the 5205A, 5215A, and 5220A Auxiliary Amplifiers. These signals are routed to the rear panel from the Motherboard through connector J8 and an external cable. The 5205A and 5220A configurations are described later.

2-212. 5205A INTERFACE

The 5205A is a power amplifier with gain of -100 and a bandwidth of dc to 100 kHz. When the 5205A function is selected via the calibrator keyboard, the output of the calibrator is routed to connector J3 (pins 1, 9, 2, and 10) on the rear panel, which is closed-loop interfaced to the 5205A.

NOTE

> Model 5215A is also compatible with the 5205A connector. The 5215A provides the same ac functions of the 5205A, but not the dc functions.

During this mode of operation, the calibrator is configured to the ac 11V range. Relay K1 is energized and relay K3 is set connecting B IN to 5205A INPUT HI, B FB to 5205A SENSE HI2, PA COM to 5205A INPUT LO, and B SNSLO to 5205A SENSE LO. Relay K4 is energized, connecting 5205A SENSE LO to 5205A SENSE L and 5205A SENSE HI to buffer amplifier U13. The output of buffer U13 is connected to K3 pin 9.

Relay K11 connects the 5205A voltage guard signal V-GRD2 to the 5700A voltage guard V GUARD.

In addition to the ac signal, the 5700A/5205A interface is composed of four control lines and logic power. +5V LOGIC provides logic power for the opto-isolators in the 5205A and +5V LOGIC COMMON provides the return. The rear panel data bus, 5205AEN*, and Y5205WR* are used by latches in U9 to create control lines CONTROL and OPERATE to connector J3, pins 14 and 15, respectively.

CONTROL, when asserted low, places the 5205A in the "5200 Control" mode and sets up the 5205A for commands. OPERATE, when asserted low, commands the 5205A to go into operate.

The 5205A generates STATUS and TRIP signals that are connected to buffer U12 where they are monitored, via the DATA BUS and control line Y52XXRD*, by the 5700A.

STATUS, when asserted low, indicates that the 5205A is in the operate mode. TRIP, when asserted low, tells the 5700A that the 5205A has experienced a fault or overload and is no longer in the OPERATE mode.

2-213. 5220A INTERFACE

The 5220A is a transconductance amplifier with a gain of one. Its output range is from 0 to 20A, thus its input voltage is from 0 to 20V.

When the 5220A is selected via the front panel, the output of the 5700A is routed to connector J4 on the rear panel, which is the interface to the 5220A.

The 5220A is designed to be operated with the 5700A in an open loop configuration. In this mode of operation, relays K2 and K3 are reset and relays K1 and K5 are energized.

This configuration ties B IN to B FB and connects them to 5220A INPUT HI. B SNSLO and PACOM are tied together and connected to 5220A INPUT LO. In this mode, the 5700A senses at the rear panel.

In addition to 5220A INPUT HI and 5220A INPUT LO, the interface between the 5700A and 5220A is composed of ten control lines.

Lines BD0-BD3 form a four-bit bidirectional data bus. Data from the 5220A is buffered and read on the DATA BUS by buffer U12 and control line Y52XXRD*. Data to the 5220A is generated from the DATA BUS by latches in U10 and control lines 5220AEN* and Y5220WR*. This data is buffered by U11 and controlled by 5220ADIR* before connecting to J4, pins 4, 12, 3, and 11.

Lines BC0, BC2, BC3, and BC6 form a four bit address bus. This address is generated from the DATA BUS by latches in U10 and control lines 5220AEN* and Y5220WR*.

The 5220A generates status lines ACK* and WR*, which are connected to buffer U12 where they are monitored, via the DATA BUS and control line Y52XXRD*, by the 5700A. ACK* is asserted low when a valid address is accepted by the 5220A. WR* is asserted low when its OK to read the 5220A status.

2-214. 5725A INTERFACE

The 5700A is designed to work in close connection the 5725A Amplifier. The function of the rear panel in this system is to provide relay switching for the 5725A signals. The 5725A performs the same functions as both the 5205A and 5220A amplifiers. All voltage outputs from the 5725A are routed back to the binding posts on the 5700A. All current outputs from the 5725A are sourced at the 5725A OUTPUT binding posts. You can configure the 5700A to also source all its current outputs through the 5725A OUTPUT binding posts for convenience.

Connector J8 and Cable 4406 interface all the 5700A I/O signals between the motherboard and the rear panel. Connector J7 interfaces the 5700A to the 5725A Amplifier. The interface between these two connectors is accomplished through relays K1, K2, and K6-K9. Relays K6-K9 break all the I/O lines except B-SENSE HI, B-OUT HI, V-GUARD, and B-IGRD, and connect them all to V-GUARD when the 5725A is not in use.

During 5725A operation, relays K1, K2, K6, and K7 switch the 5700A analog signals B IN, B FB, B SNSLO, and PACOM to lines BOOST IN, B-FEEDBACK, B-SENSE LO, and BPA COM on connector J7.

High voltage output of the 5725A (B-OUT HI and B-SENSE HI) is connected to the 5700A Motherboard via cable 4406 where it can be switched to the 5700A binding posts by relays on the Motherboard.

Relays K8 and K9 connect the 5725A current function lines I-RET, and B-CUR on connector J8 to B-IRTN, and B-CURRENT, on connector J7 when the 5725A is outputting 5700A current (<=2.2A). Line B-RCL is used during 5725A calibration. Line B-RCL on J7 is connected to J8 through relay K6. Line B-RCL is routed via the motherboard to the Current assembly (A7) where it is switched to the calibrator RCL line by a relay.

2-215. PHASE LOCK IN/VARIABLE PHASE OUT

The Oscillator Output assembly (A13) can be phase locked to an external signal connected to the PHASE LOCK IN BNC connector J6. Relay K10B connects the shell of this BNC connecter to chassis ground through protection resistor R19 when the 5700A is on internal operation, or to P LOCK LO when the 5700A is phase locked to the external signal coming in on J6.

This incoming signal is called PHLK IN on the schematic. Relay K10A switches an external phase-lock signal from J6 to the input of Q1 and Q2. FETs Q1 and Q2 provide current limiting for PHLK IN. Signal P LOCK is routed to connector J8 where it is connected to the Oscillator Output assembly via the Motherboard.

Components CR1, CR2, VR1, VR2, R4, and R5 provide amplitude protection for the phase lock circuitry on the Oscillator Output assembly by limiting the amplitude of P LOCK.

The Variable Phase Out BNC connector (J5) is connected to P SHIFT and its shell is connected to PA COM by energizing relay K12. Signal P SHIFT is a fixed-amplitude variable phase signal generated by the Oscillator Output assembly (A13). Refer to the Oscillator Output assembly theory of operation for a detailed description on the generation of P SHIFT. Resistor R18 serves as overcurrent protection for the BNC shell connection on J5.

2-216. REAR PANEL RELAY CONTROL

The relays on the Rear Panel assembly are used as the interfaces for the 5205A, 5215A, 5220A, or 5725A amplifiers, or for switching the PHASE LOCK IN and VARIABLE PHASE OUT signals.

The relay switching circuitry is under control of the guarded digital bus via connector J8. This guarded digital bus is generated on the Regulator/Guard Crossing assembly (A17).

The relay control circuitry is located on page 5 of the Rear Panel schematic. This circuit uses an 82C55 programmable peripheral interface (U14) and two relay drivers (U16 and U17) to control the 12 relays on this assembly and one relay (K12) on the analog motherboard. The 82C55 (U14), which is under control of the guarded digital bus via connected J8, has three ports generating 24 outputs.

Port A (PA0-PA7) provides the input lines for relay driver U16.

Port B (PB0-PB7) provides the input lines for relay driver U17.

PC0-PC2 of port C provides the CLEAR, STROBE, and OUTPUTENABLE lines for these relay drivers.

Relay Driver U16 controls two latching relays (K2 and K3) and four non-latching relays (K1, K4, K5, and K7). Relay driver U17 controls one latching relay (K6) and five non latching relays (K8-K12). Relay driver U17 also creates control line RLY12* (pin 13) which controls relay K12 on the Analog Motherboard assembly (A3).

2-217. REAR PANEL CPU INTERFACE

The rear panel is interfaced to the CPU assembly (A20) via connector J8 on the rear panel. The CPU has:

- Five address lines (RPA1-RPA5) which comprise the ADDRESS BUS
- Seven control lines which comprise the CONTROL BUS
- A low-level 3.6864 MHz clock (CLOCK, CLOCK*)
- Eight data lines RPD0-RPD7

Interfacing between the Rear Panel data bus (D100-D107) and the CPU data bus (RPD0-RPD7) is done with a bus transceiver U1.

2-218. Wideband AC Module (Option -03)

The Option -03 Wideband AC Module consists of the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5).

The wideband module operates in conjunction with the Oscillator Output assembly (A13), and provides calibrated output voltages in the range of 300 uV to 3.5V rms at frequencies of 10 Hz to 30 MHz, into a 50 ohm load resistance.

The output impedance of the assembly is 50 ohms. It is designed to drive 50 ohm loads. The output of this option connects to the Type "N" wideband connector on the 5700A front panel.

The theory of operation covers the Wideband Oscillator assembly (A6) and the Wideband Output assembly (A5).

2-219. Wideband Oscillator (A6) (Option -03)

The Wideband Oscillator assembly generates sine wave outputs in the range of 1.1 MHz to 30 MHz, (with two-digit resolution) at a nominal full scale output of 700 mV rms.

The frequency source is a ECL-level square wave with a frequency range of 1.1 MHz to 30 MHz, created in the phase-locked loop and divider circuit. The amplitude of this square wave is controlled by the WB AMPLITUDE CONTROL line, which is a DC signal from the Wideband Output assembly, and the circuitry contained in the amplitude control amplifier.

The resulting variable frequency and amplitude square wave is converted to sine wave by one of the five-pole filters. This variable frequency and amplitude sine wave is routed to the Wideband Output assembly via connector J1 and a 75 ohm coaxial cable.

2-220. WIDEBAND OSCILLATOR POWER SUPPLIES

The +5LH, -5LH, +17S, and -17S supplies are generated on the Regulator assembly and routed to this assembly via the motherboard.

The -5LH supply is buffered by L12 and C49, creating the -5F supply.

The +5LH supply is divided by R66 and R67 to create the +2.5 supply which is the reference voltage for comparators in U7, U10, and U11.

Zener diode VR1 and resistor R39 create the +12 supply from the +17S supply. Zener diodes VR4 and VR5, resistors R40 and R41, and diodes CR8 and CR9 create the -12, -11, and -9.5 supplies from the -17S supply. These are used throughout the Wideband Oscillator assembly.

2-221. WIDEBAND OSCILLATOR DIGITAL CONTROL

The digital control circuit on the Wideband Output assembly creates control lines WB MUXA, WB MUXB, WB MUXC, WB FBS, and WB ON/OFF*. These lines are routed to the Wideband Oscillator via the Motherboard.

Control lines WB MUXA, WB MUXB, and WB MUXC are inverted and level-shifted by comparators in U7 to create the control lines for multiplexer U6. They are also used by the filter-select circuitry.

In this circuit, WB MUXA, WB MUXB, and WB MUXC are decoded by U8 to generate four control lines, These are inverted and level-shifted by comparators in U10 and U11. The output of these comparators create 16-32MHz FILTER, 8-16MHz FILTER, 4-8MHz FILTER, 2-4MHz FILTER, 1-2MHz FILTER, and Q8/Q9 SELECT, which are used in the filter switch drive circuitry.

Control line WB FBS is inverted and level-shifted by a comparator in U10. This creates FILTER BAND SWITCH, which is also used in the filter selection circuitry. Control line WB ON/OFF* shuts down the 8 MHz clock generator and vco when the wideband module is not in use.

2-222. PHASE-LOCKED LOOP AND DIVIDER CIRCUIT

The phase-locked loop and divider circuit uses 8 MHz clock generator U15, synthesizer IC U1, amplifier U2, vco U3, and dividers in U4 and U5 to generate an ECL-level square wave from 1.1 MHz to 30 MHz.

The 8 MHz clock generator creates the 8 MHz reference frequency from the 8 MHz system clock lines CLK and CLK*, which is a low level (~200 mV p-p) 8 MHz sine wave generated on the Regulator/Guard Crossing (A17) assembly. Comparator U15 converts this sine wave into a TTL-level 8 MHz square wave to provide the reference frequency for synthesizer IC U1.

Synthesizer IC U1 contains two programmable divide-by-N counters and a phase detector. The divide-by-N counters are controlled by inputs from the guarded digital bus, which are latched into internal latches on the IC. NOR gates in U14 are used to gate the chip select (CS14) and write (WR) lines from the digital bus. This forms the strobe pulse necessary to latch the frequency data into the synthesizer IC.

The first divide-by-N counter is programmed to divide the 8 MHz reference by 160 to give 50 kHz. This, in turn, is applied to one input of the internal phase detector. The other divide-by-N counter is used to divide the feedback frequency at pin 3 by 80 to 160 in 1 digit steps, and then apply it to the second input of the phase detector. The loop is locked when the two inputs to the phase detector are the same frequency and phase.

With a 50 kHz reference frequency and the feedback divider programmed between 80 and 160, the input frequency at pin 3 (feedback frequency) must be between 4 MHz and 8 MHz. (50 kHz X 80 = 4 MHz and 50 kHz X 160 = 8 MHz.)

The frequency into U1 pin 3 is generated by the vco (U3) and dividers in U4 and U5. A flip flop in U4 divides the vco frequency by 2 and the binary counter in U5 further divides by 4 to give a total division of 8.

If the input to U1 pin 3 is between 4 MHz and 8 MHz, then the vco frequency before the divide-by-8 must be 32 MHz to 64 MHz.

The phase detector outputs ("OV" on pin 14 and "OR" on pin 15) of the synthesizer U1 are used by the amplifier (U2) to control the vco (U3). If the divider feedback frequency is greater than the 50 kHz reference frequency, or if the phase of the divider feedback frequency leads the output, then OV pulses low while output OR remains high.

If the divider feedback frequency is less than the 50 kHz reference frequency, of if the phase of the divider feedback frequency lags the output, then OR pulses low and the output OV remains high.

When the feedback frequency and the 50 kHz reference frequency are the same and in phase, the output OV and OR both remain high except for a small period when both pulse low in phase. This condition occurs when the loop is locked.

The vco frequency is controlled by varactor diodes, CR1 + CR2, which get their bias voltage from amplifier U2. Amplifier U2, which gets its input from the phase detector outputs (OV and OR) of U1, changes the bias on varactor diodes CR1 and CR2 until the divided vco frequency has the same frequency and phase as the 50 kHz reference frequency at the input to the phase detector in U1.

Any phase difference is amplified by U2 and filtered by L6, C53, and C17 to bring the loop into lock.

The vco is shut off whenever the Wideband AC module is not in use. To shut off the vco control line WB ON/OFF* is set low and inverted by a comparator in U7 which then turns on Q3.

With transistor Q3 on, transistor Q2 is turned off which removes the -5V supply from the vco to stop the oscillation.

With the vco frequency between 32 and 64 MHz, U4 divides by 2 to give a symmetrical square wave of 16 to 32 MHz, which is the top octave range required for this assembly. Further division by two (pin 15), four (pin 13), eight (pin 4), and sixteen (pin 2) by binary counter U5 gives the other ranges required of 8 to 16 MHz, 4 to 8 MHz, 2 to 4 MHz, and 1 to 2 MHz.

Multiplexer U6, under software control via control lines WB MUXA, WB MUXB, WB MUXC, and comparators in U7, can be programmed to select which of the 5 ranges is needed to give the output frequencies of 1 to 32 MHz.

2-223. AMPLITUDE CONTROL AMPLIFIER AND X10 WIDEBAND AMPLIFIER

The square wave output generated by the phase-locked loop and divider circuit (1-32MHZ OUTPUT) is connected to the amplitude control amplifier circuit.

This circuit uses transistor array U9 to form a differential gain-control amplifier. Gain of the amplifier is controlled by the dc signal AMPLITUDE CONTROL, connected to U9 pin 10.

DC signal AMPLITUDE CONTROL is generated by the thermal rms sensor amplitude control circuitry on the Wideband Output assembly (A5) and is discussed in that section.

The gain controlled square wave output of U9 (pin 6) is further amplified by the x10 wideband amplifier circuit. Transistors Q4, Q5, and Q6 are configured as an amplifier with a gain of ten. This amplifier raises the gain-controlled square wave to the level needed to drive output filters. The output of this circuit is a square wave with an amplitude between 1.4V p-p to 6.0V p-p.

2-224. WIDEBAND OSCILLATOR FILTERS

Each of the five octave frequency ranges has a 5-pole filter to change the square wave input to a sine wave output with a nominal full scale output of 700 mV rms.

The filter switch drive circuit uses control lines from the filter select circuit (that contains transistor arrays U12 and U13) to provide the drive to properly turn on and off FETs and transistors in each of the filters.

The filter inputs and outputs are switched on by FETs and the filter output is applied to output driver Q7. The corresponding filter is selected automatically as each octave range is selected. The operation of the 16-32 MHz filter is described. The other four filters operate in a similar fashion.

The input FET Q101 is turned on via control line 16-32MHZ FILTER and a transistor in U13. This applies the signal FILTER INPUT from the X10 wideband amplifier to follower Q102. Transistor Q102 drives the filter that contains L102, L103, L104, C109 and C112. FET Q105 is turned on, in the same manner as FET Q101, to connect the sine wave output of this filter to FILTER OUTPUT. This is applied to output driver transistor Q7.

To obtain the required amount of filtering over the entire octave range, additional capacitors C110 and C111 are switched into the filter by PIN diodes CR102 and CR103 when operating below 70% of the full range (22 MHz in this case).

Diodes CR102 and CR103 are activated by turning on Q103 and Q104, respectively. Transistors Q103 and Q104 are turned on via control line Filter Band Switch and a transistor in U12.

Two additional FETs, Q8 and Q9, are used to isolate the 16-32 MHz filter and the 8-16 MHz filter, from the three other lower frequency filters, whenever the two high frequency filters are used. The isolation provided by FETs Q8 and Q9 eliminates both the input and output load capacity and circuit board capacity of the three lower frequency filters, so that follower Q6 can drive the high frequency filter input without distortion of the waveform. This also eliminates loading the filter outputs, which changes the filter frequency response.

2-225. Wideband Output Assembly (A5) (Wideband AC Module, Option -03)

The Wideband Output assembly (A5) takes the sine wave signal from either the Wideband Oscillator assembly (A6) or the Oscillator Output assembly (A13), and amplifies it to a power level that drives 3.5V into a 50 ohm load at the output.

The Oscillator Output assembly generates the sine wave signal from 10 Hz to 1.1 MHz, and the Wideband Oscillator assembly generates the sine wave signal from 1.2 MHz to 30 MHz. This provides a total frequency range of 10 Hz to 30 MHz.

The Wideband Output assembly contains a power amplifier circuit that increases the gain and/or power level of the input signal. Also contained on the assembly are a thermal rms sensor circuit necessary for amplitude control, the 50 ohm attenuators needed to reduce the output level through all of the amplitude ranges, an overload control circuit, and digital control circuitry.

Figure 2-35 is a simplified schematic for the Wideband Output assembly.

The Wideband Output assembly has three basic operating ranges:

1. The first range is for Wideband AC module operation at frequencies between 10 Hz and 11.9 kHz. In this frequency range, relay K1A is in the set position so the input signal is from the Oscillator Output assembly with its amplitude is controlled by the Oscillator Control assembly (A12).

   The amplitude control circuit on the Wideband Output assembly is only used for overload protection. This is done by control line PB0 which goes high and turns on FETs Q2 and Q3 via comparator U4B.

   These FETs shunt the rms sensor's input and output to ground through 200 ohm resistors (R2 and R18) to reduce the sensitivity of the sensor.

2. The second range is for operation at frequencies between 12 kHz and 1.1 MHz. In this mode the input signal is also from the Oscillator Output assembly, but the amplitude is controlled by the amplitude control circuit on the Wideband Output assembly.

   Relay K10 is in the set position to connect the output of the rms sensor and amplitude control circuit to the RCL line where it is measured by the adc circuit on the DAC assembly.

   The DAC assembly operates in conjunction with the Oscillator Control assembly to adjust the amplitude of the Oscillator Output signal.

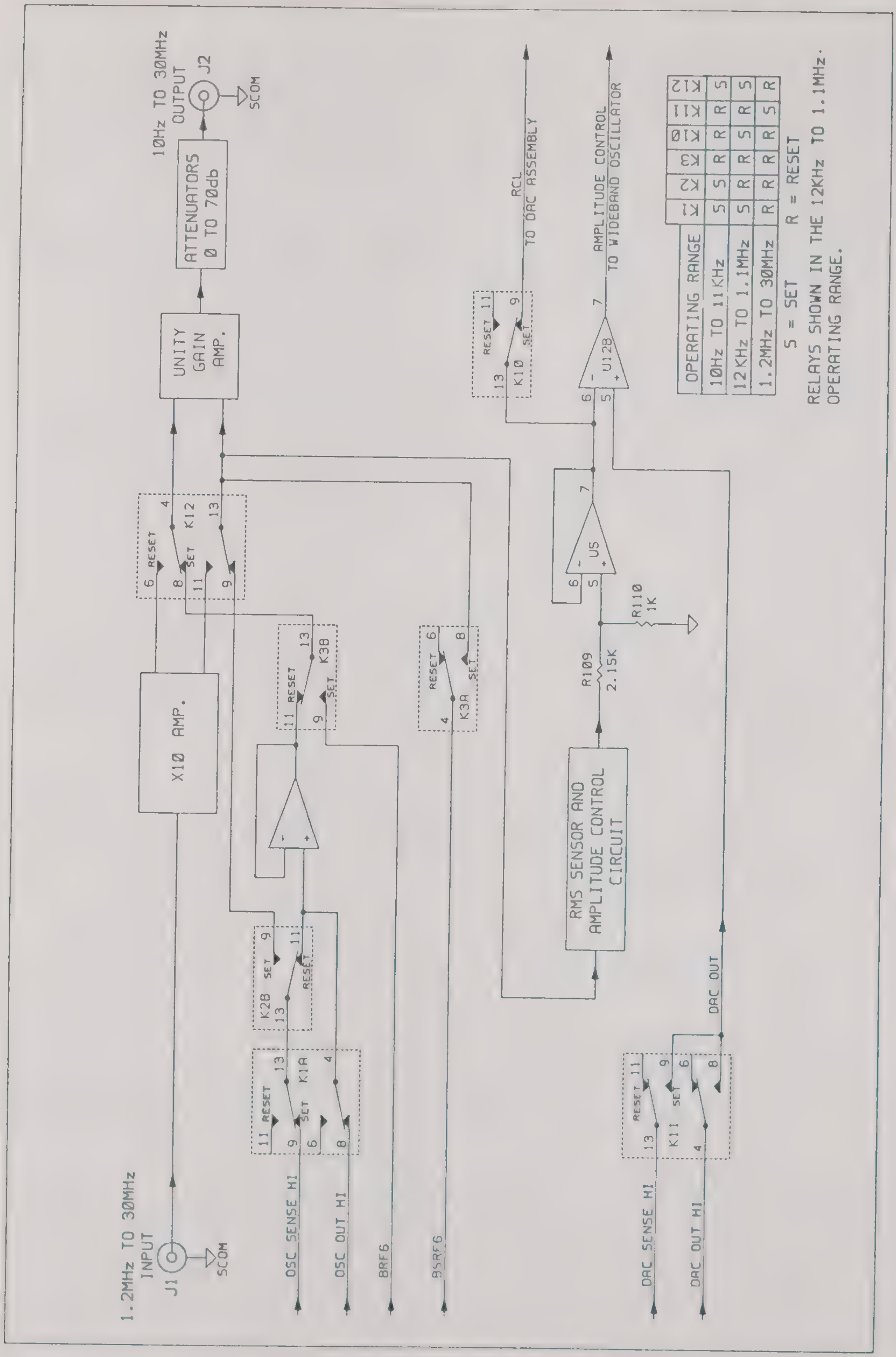

1.2MHz TO 30MHz INPUT
J1
SCOM
X10 AMP.
K12
RESET
SET
UNITY GAIN AMP.
ATTENUATORS 0 TO 70db
10Hz TO 30MHz OUTPUT
J2
SCOM
K3B
K3A
K2B
K1A
OSC SENSE HI
OSC OUT HI
BRF6
BSRF6
RMS SENSOR AND AMPLITUDE CONTROL CIRCUIT
R109 2.15K
R110 1K
U5
U12B
K10
RCL TO DAC ASSEMBLY
AMPLITUDE CONTROL TO WIDEBAND OSCILLATOR
K11
DAC OUT
DAC SENSE HI
DAC OUT HI
OPERATING RANGE | K1 | K2 | K3 | K10 | K11 | K12
10Hz TO 11KHz | S | S | R | R | R | S
12KHz TO 1.1MHz | S | R | R | S | R | S
1.2MHz TO 30MHz | R | R | R | R | S | R
S = SET R = RESET
RELAYS SHOWN IN THE 12KHz TO 1.1MHz OPERATING RANGE.

Figure 2-35. Wideband Output Assembly Simplified Schematic

3. The third range is for operation at frequencies between 1.2 MHz and 30 MHz. In this mode the input signal is from the Wideband Oscillator assembly via connector J1. Its amplitude is controlled by the amplitude control circuit on the Wideband Output assembly.

   In this mode the output of the DAC assembly, DAC OUT HI and DAC SENSE HI, are connected to DAC OUT by relay K11 in the set position. Op amp U12B compares DAC OUT to the output of the rms sensor and amplitude control circuit. Any difference between these two signals is amplified and routed to the Wideband Oscillator assembly via the AMPLITUDE CONTROL line.

   The Wideband Oscillator uses the Amplitude Control line to adjust its AC amplitude until the sensor output is equal to the DAC voltage.

2-226. WIDEBAND OUTPUT POWER AMPLIFIER CIRCUIT

The power amplifier circuit, as outlined on page 1 of the Wideband Output assembly schematic, contains all the circuitry shown on page 2 of the schematic. This circuitry consists of the x10 amplifier, the unity-gain amplifier, and the 10 Hz to 1.1 MHz buffer circuit as outlined on the schematic.

The x10 amplifier circuit is used only during operation in the 1.2 MHz to 30 MHz range. The 1.2 MHz to 30 MHz sine wave input comes from the Wideband Oscillator assembly via a coaxial cable and connector J1. This input signal has a nominal full-scale amplitude of 700 mV rms.

The x10 amplifier circuit uses transistors Q4, Q5, Q6, Q7, Q8, Q9, and Q10 to amplify this signal by a factor of 10. Amplifier U11A keeps the DC offset on the output to near zero. The output of the X10 amplifier is applied to the unity gain amplifier by relay K12 in the reset position. The output impedance of the unity gain amplifier is 50 ohms, therefore the x10 amplifier must produce 7.0V rms to give 3.5V rms into the 50 ohm load.

The 10 Hz to 1.1 MHz buffer circuit is used during operation in the 10 Hz to 12 kHz range or the 13 kHz to 1.1 MHz range. In this mode, the input signal comes from the Oscillator Output assembly. This input signal is buffered by Q17 and applied to relay K12. Amplifier U11B keeps the DC offset on the output near zero for the 10 Hz to 1.1 MHz range.

The unity-gain amplifier is connected to either the output of the x10 amplifier or the output of the 10 Hz to 1.1 MHz Buffer by relay K12. The unity gain amplifier uses transistors Q11-Q16 and associated components. This circuit increases the power to a level that drives 3.5V rms into a 50 ohm load. The four 1/2 watt resistors in parallel (R96, R97, R98, R99) along with the output resistance of the amplifier form the 50 ohm output resistance.

The output of this amplifier, called 10HZ TO 30MHZ OUTPUT, is a sine wave with an amplitude between 1.1V and 3.5V rms into 50 ohms. This output signal is used by the attenuators to provide the overall output range of the Wideband Output assembly. Resistors R41 and R42, and capacitor C23 divide this output signal to create OUTPUT OFFSET for diagnostics.

2-227. WIDEBAND OUTPUT ATTENUATORS

The 10 Hz to 30 MHz sine wave signal output of the power amplifier circuit connects to the 50 ohm output attenuator composed of attenuator networks Z1 and Z2 and relays K4, K5, K6, K7, and K8.

Relay K4 switches the 10 dB attenuator into the circuit when activated or bypasses it when not activated.

Relay K5 switches the 20 dB attenuator into the circuit when activated or bypasses it when not activated.

Relays K6 and K7 switch the 40 dB attenuator into the circuit when activated and bypasses it when not activated. The attenuator can therefore reduce the signal level in 10 dB steps from 0 to 70 dB.

The output amplitude of the power amplifier circuit can be continuously varied over a 10 dB range, which when combined with the 0 to 70 dB attenuator, gives the the continuous output range of 300 uV to 3.5V rms.

When energized, relay K8 enables the output signal to be connected to the output coaxial connector J2.

2-228. WIDEBAND OUTPUT RMS SENSOR AND AMPLITUDE CONTROL CIRCUIT

The rms sensor circuit is used for:

- Amplitude control
- Overload control over the frequency range of 12 kHz to 30 MHz
- Overload control only over the frequency range of 10 Hz to 12 kHz

The rms sensor and amplitude control circuit is composed of U1, U2A, U2B, U3, U5, U12A, U12B, and associated components. Thermal sensor U1 provides a dc voltage equal to the rms value of the input voltage (at pin 6).

Input voltage to the thermal sensor comes from the power amplifier circuit. DC voltage output from the thermal sensor is connected to U2A configured as an intergrator. The output of the intergrator is connected to a square-root amplifier configured by U2B U3, and U12A, which keeps the settling time of the sensor constant.

The dc output of this sensor circuit (available at TP1) is buffered by U5. In the 12 kHz to 1.1 MHz range, the output of U5 is connected to the RCL line by relay K10 in the set position. In the 1.2 MHz to 30 MHz range, the output of U5 is compared by U12B to DAC OUT.

The DAC assembly (A11) output, DAC OUT HI and DAC SENSE HI, are tied together by relay K11 to create DAC OUT.

Relay K2A connects capacitor C7 into the rms sensor circuit in the 10 Hz to 11 kHz range to add additional filtering for low frequency signals.

2-229. WIDEBAND OUTPUT OVERLOAD CONTROL CIRCUIT

The overload control circuit contains comparator U4 (A and B), FETs Q2 and Q3, transistor Q1, and associated circuitry. This circuit protects the rms sensor and attenuators during an overload condition. Comparator U4A detects an overload condition by comparing the dc output of the rms sensor against a reference voltage.

The reference voltage is determined by zener diode VR2 and resistor R21. If the dc output of the rms sensor reaches a voltage 10% greater than the normal full-scale voltage, the output of U4A goes negative. This negative voltage causes a positive voltage at the output of U4B which turns on FETs Q2 and Q3. These FETs protect the rms sensor from damage by shunting its input and output to ground through the 200 ohm resistors R2 and R18.

The negative voltage at the output of U4A also turns off transistor Q1 and causes control line U9 ENABLE to go high. This disables relay driver U9, which turns off all attenuator relays (K4-K7) and output relay K8.

2-230. WIDEBAND OUTPUT DIGITAL CONTROL

The heart of the Wideband Output assembly digital control circuitry is a 82C55 programmable peripheral interface IC (U7), which is under software control via the guarded digital bus.

This IC has three ports, generating 24 outputs. These outputs control three relay drivers (U6, U9, U10) and a 4051 analog multiplexer IC (U8) for self diagnostics.

Port A (PA0-PA7) is used as a common input bus for the relay drivers. Relay driver U6 controls latching relays K1, K2, K10, K11, and K12. Driver U6 is enabled by PC3 and strobed by PC2. Relay driver U9 controls non-latching relays K4-K8. Driver U6 is strobed by PC0 and enabled by control line U9 ENABLE, which is generated in the overload control circuit. Relay driver U10 controls latching relays K3 and K9. It is strobed by PC1 and enabled by PC3.

Relays K1 and K12 are controlled by the same drive lines and, when in the set position, select the input from the Oscillator Output (A13) assembly during operation between 10 Hz and 1 MHz.

Relay K9 connects a 50 ohm load (R43 and R44 in parallel) to the RCL line where the adc circuit on the DAC assembly can monitor the output voltage and thereby determine proper operation of the output attenuator resistors and relays.

The 4051 analog multiplexer IC (U8) is used by self-diagnostic routines for the Wideband AC module. This allows the 5700A to monitor three points on the Wideband Output assembly and one point on the Wideband Oscillator assembly. Points AMPLITUDE CONTROL, OUTPUT OFFSET, and SENSOR CAL are monitored on the Wideband Output assembly, and point PLL DIAGNOSTIC is monitored on the Wideband Oscillator assembly. PC4-PC6 of port C select which point the multiplexer monitors. PC7 enables the output of U8 to the SDL line where is is measured by the adc circuit on the DAC assembly (A11).

2-231. WIDEBAND OUTPUT CALIBRATION

Linearity of the rms sensor is determined by configuring the Wideband Output similarly to the second range of operation as described earlier. A difference is that the Oscillator Output assembly operates at 1 kHz instead of between 12 kHz and 1.1 MHz during operating in this range.

The Oscillator Output is set to 2.5V at 1 kHz. The resulting dc voltage from the rms sensor is connected to the RCL line by relay K10 in the set position. The RCL line is routed to the +input of the adc circuit on the DAC assembly, and the adc -input is connected to the DAC output. The difference between the two is measured and stored in memory. The Oscillator Output is increased to 7.0V and the difference between the two adc inputs is again measured. Software uses these values to determine the linearity of the rms sensor.

The previously calibrated 6.5V reference BRF6 and its sense line BSRF6, from the DAC assembly is used to calibrate the 10 dB, 20 dB, and 40 dB attenuators.

Relays K3 A and B and K12 are in the set position. This connects the 6.5V reference to the unity-gain amplifier and the attenuators. Output at the WIDEBAND type-N connector is connected back to the OUTPUT HI SENSE and OUTPUT LO SENSE binding posts.

Attenuation is calibrated starting with 70 dB and decreased in 10 dB steps to 0 dB. The Switch Matrix assembly connects the output of the Wideband AC module to its internal cal zero amplifier circuit during all attenuator calibrations except the 0 dB and 10 dB. The internal cal zero amplifier circuit provides a gain of 10 to Wideband output during 20 dB to 70 dB attenuation calibration. The output of this amplifier is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. Output from the DAC is connected to the -input of the adc circuit and adjusted until a null is achieved. The exact attenuator value is then determined.

Section 3
Calibration and Verification

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3-1. INTRODUCTION

This section gives procedures for 5700A calibration, verification, acceptance testing, and performance testing. Information here applies to testing the performance of and calibrating a normally operating 5700A. In case of malfunction, refer to Section 5, Troubleshooting, which explains how to use self diagnostic tests to identify a faulty module. Calibration and Performance Testing is presented in the following three parts:

- Calibration, which is to be done at the beginning of every calibration cycle. This is the same procedure as in Section 7 of the 5700A Operator Manual. It uses three external standards; 1 ohm, 10 kilohm, and 10V dc. The procedure is duplicated here for convenience. Also included in this part are procedures for doing Calibration Check and Range Calibration.

- Full Performance Verification, which is the full verification procedure, recommended every two years. Part of this procedure is Wideband AC Module (Option 5700A-03) flatness calibration, also recommended only every two years.

- Optional Tests, which are recommended following repair or for use in acceptance testing. These tests include such checks as load regulation, noise, and distortion. These tests are not required on a routine basis. They are not necessary after a 5700A passes Full Performance Verification.

3-2. CALIBRATION

The following paragraphs cover the procedures for calibrating the 5700A to external standards, performing calibration check, and adjusting a range constant.

When shipped, your 5700A is calibrated at the factory, traceable to the U.S. National Bureau of Standards. All that is required to maintain traceability is calibration to external standards at the beginning of the calibration cycle and performance verification every two years. Calibration check and range calibration are optional procedures that are available for special needs.

Additional information about 5700A calibration is contained elsewhere in the manuals:

- Section 1 of the Operator Manual describes the calibration process and the theory behind its use to establish traceability to national standards. Included in the same section is a description of the calibration check feature, and how you can use it to develop a performance history for your 5700A.
- Section 2 of the Service Manual contains detailed theory of operation.
- Section 4 of the Operator Manual explains how to do the very quick, automatic DC Zeros Calibration, which removes offsets on the 2.2V dc range.
- This section of the Service Manual contains a performance verification procedure that may be done every two years to maintain traceability. Part of this is Wideband AC Module (Option 5700A-03) flatness calibration.

3-3. Calibrating the 5700A to External Standards

Calibration to external standards is required at the beginning of the calibration cycle. The cycle is selected in a setup menu as described in Section 4 of the Operator Manual (24 hours, 90 days, 180 days, or 1 year). To calibrate the 5700A, you apply three portable standards to the OUTPUT binding posts: a 10V dc voltage standard, a 1 ohm resistance standard, and a 10 kilohm resistance standard. The following standards are recommended:

- Model 732A dV Reference Standard
- Model 742A-1 1 Ohm Standard Resistor
- Model 742A-10k 10 kilohm Standard Resistor

You do not need to calibrate the 5700A in a tightly-controlled temperature environment. The recommended external standards and the 5700A have the ability to control or compensate for ambient temperature variations internally. During the procedure, the 5700A prompts you to input the ambient temperature. The 5700A retains this information for inclusion in specification readout and output shift reports.

When you finish calibration, but before you save the new constants, the 5700A presents you with the new changes as ± ppm and change as a percentage of specification for each range and function. You can print a list of changes through the serial (RS-232-C) port, or send the changes to a computer through either the serial port or the instrument control (IEEE-488) port. The 5700A displays the largest proposed change on the front panel.

Table 3-1 lists the equipment required to calibrate the 5700A to external standards.

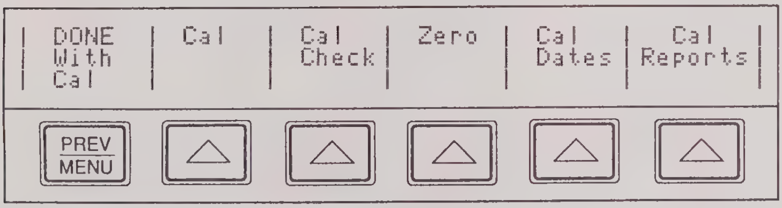
Table 3-1. Equipment Required to Calibrate the 5700A

MODEL	DESCRIPTION
Fluke 732A	DC Voltage Reference Standard
Fluke 742A-1	1 Ohm Resistance Transfer Standard
Fluke 742A-10K	10 kilohm Resistance Transfer Standard
Fluke 5440A-7002	Low Thermal EMF Test Leads, 2 ft (61 cm)

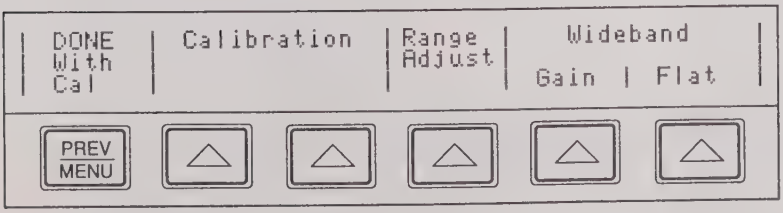
Proceed from the power-up state as follows to calibrate the main output functions:

1. Turn on the 5700A and allow it to warm up for at least 30 minutes.

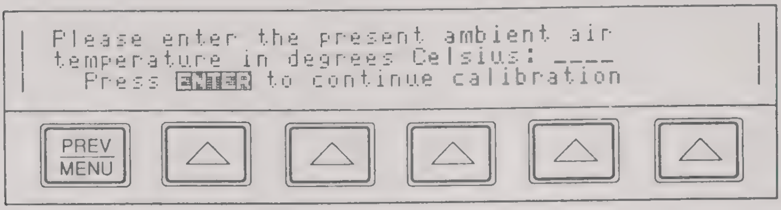
2. Press the "Setup Menus" softkey then the "Cal" softkey. The calibration menu appears:


DONE With Cal
Cal
Cal Check
Zero
Cal Dates
Cal Reports
PREV MENU

3. Press the "Cal" softkey. The display changes to:

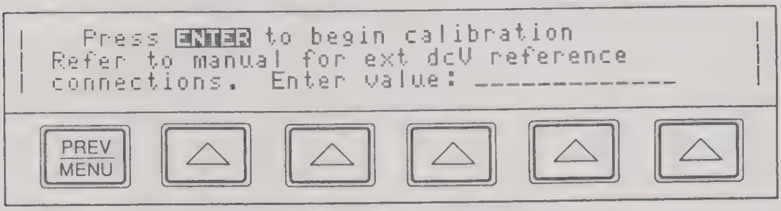

DONE With Cal
Calibration
Range Adjust
Wideband
Gain
Flat
PREV MENU

4. To calibrate the main output functions, press one of the softkeys under the "Calibration" label. The display changes to:



```
Please enter the present ambient air
temperature in degrees Celsius: ____
  Press ENTER to continue calibration
```

5. Enter the ambient temperature, and press the ENTER key. The display changes to:

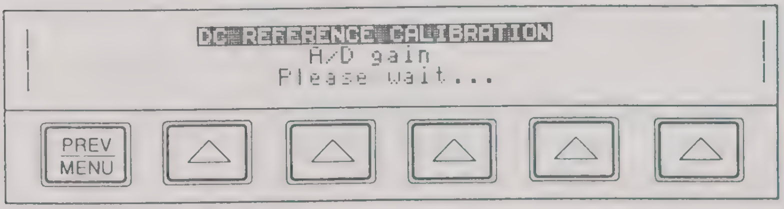


```
  Press ENTER to begin calibration
Refer to manual for ext dcV reference
connections.  Enter value: _____________
```

6. Connect the 732A to the 5700A as shown in Figure 3-1.

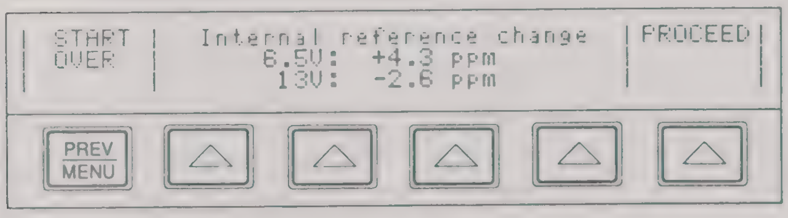
7. Enter the true value of the 732A 10V output. The true value is the value printed on the calibration sticker, plus or minus any drift since calibration. The 732A drifts in a very linear way, so you can interpolate the true value based on observed drift.

   If the entered value is not between 9 and 11V, an error message appears which allows you to start again from this point with a calibrated 732A. After you press the ENTER key, the display changes to:



```
            DC REFERENCE CALIBRATION
                    A/D gain
                 Please wait...
```

   When the 5700A 6.5V and 13V references have been characterized, the following message appears, allowing you to accept or reject the changes about to be made to the calibration constants:



```
| START |  Internal reference change  | PROCEED |
| OVER  |      6.5V:  +4.3 ppm        |         |
|       |       13V:  -2.6 ppm        |         |
```

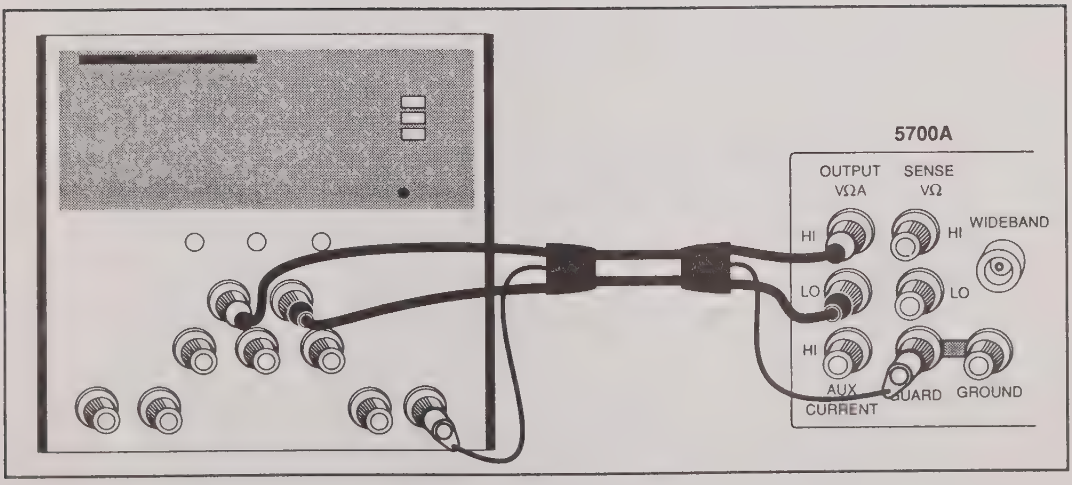
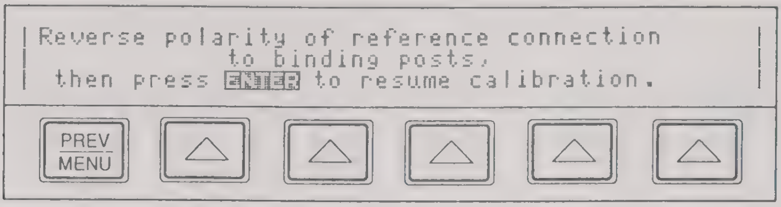

5700A
OUTPUT
VΩA
SENSE
VΩ
HI
HI
WIDEBAND
LO
LO
HI
AUX
CURRENT
GUARD
GROUND

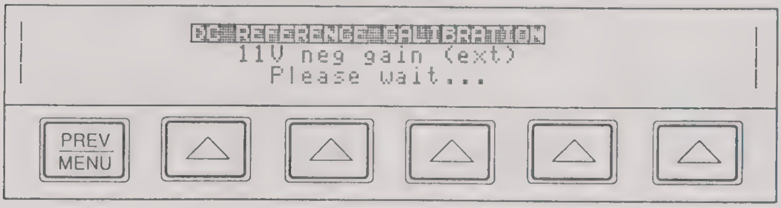
Figure 3-1. 732A External Calibration Connections

8. If you press PREV MENU, control reverts to the menu in step 3. If you press the "PROCEED" softkey, the 5700A saves the settings in temporary memory for future storage in nonvolatile memory. Calibration continues with the following message on the display:



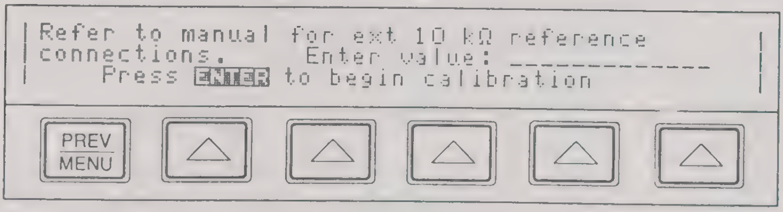
```
Reverse polarity of reference connection
          to binding posts,
 then press ENTER to resume calibration.
```

9. Reverse the HI and LO connections at the 732A terminals, and press ENTER. The display changes to:



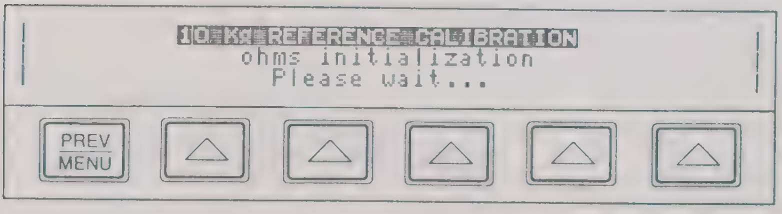
```
DC REFERENCE CALIBRATION
   11V neg gain (ext)
     Please wait...
```

10. When the display changes to:



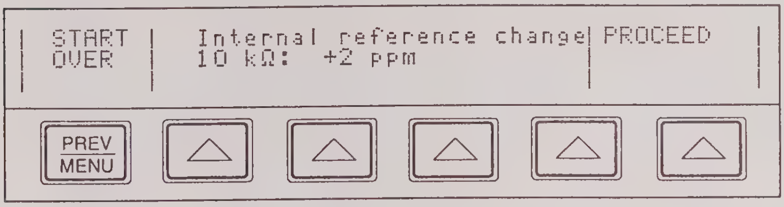
```
Refer to manual for ext 10 kΩ reference
connections.     Enter value: ______________
     Press ENTER to begin calibration
```

Connect the 5700A to the 10 kilohm standard as shown in Figure 3-2 and enter the true value of the standard. If the standard is not between 9 kilohm and 11 kilohm, an error message appears, which allows you to start again from this point with another standard. When you press the ENTER key, the display changes to:



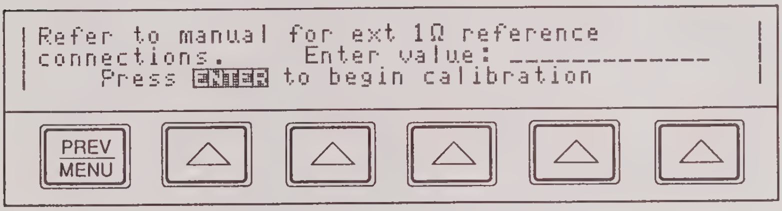
```
10 kΩ REFERENCE CALIBRATION
    ohms initialization
      Please wait...
```

When the internal 10 kilohm reference has been characterized, the following message appears, allowing you to accept or reject the changes about to be made to the calibration constant:



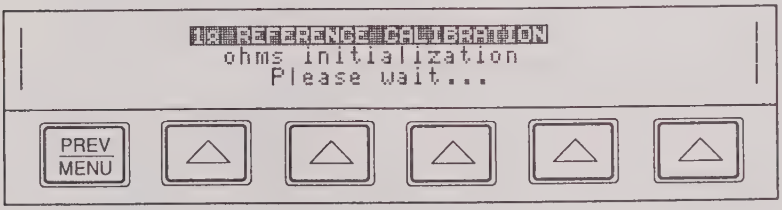
```
| START |   Internal reference change| PROCEED   |
| OVER  |   10 kΩ:   +2 ppm          |           |
|       |                            |           |
```

11. If you press PREV MENU, control reverts to the menu in step 3. If you press the "PROCEED" softkey, the 5700A saves the settings in temporary memory for future storage in nonvolatile memory. Calibration continues with the following message on the display:



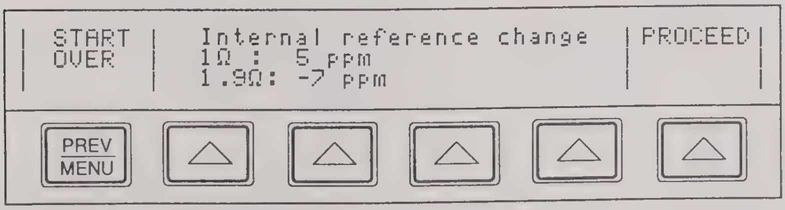
```
|Refer to manual for ext 1Ω reference             |
|connections.      Enter value: ______________     |
|     Press ENTER to begin calibration             |
```

12. Disconnect the 10 kilohm standard, and connect the 5700A to the 1 ohm standard the same way, then enter the true value of the 1 ohm standard. If the standard is not between 0.9 ohm and 1.1 ohm, an error message appears which allows you to start again from this point with another standard. When you press the ENTER key, the display changes to:



```
|              1Ω REFERENCE CALIBRATION              |
|                ohms initialization                 |
|                   Please wait...                   |
```

When the internal 1 ohm reference has been characterized, the following message appears allowing you to accept or reject the changes about to be made to the calibration constant:



```
| START |  Internal reference change  |PROCEED|
| OVER  |  1Ω  :   5 ppm              |       |
|       |  1.9Ω: -7 ppm               |       |
```

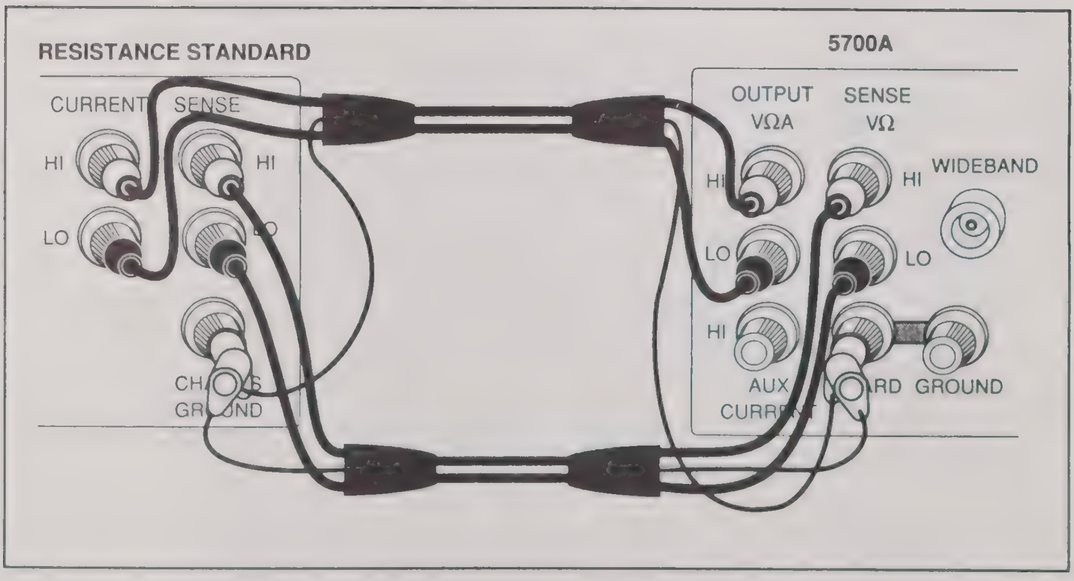

RESISTANCE STANDARD
CURRENT
SENSE
HI
LO
HI
LO
CHASSIS GROUND
5700A
OUTPUT VΩA
SENSE VΩ
HI
LO
HI
LO
WIDEBAND
HI
AUX CURRENT
GUARD
GROUND

Figure 3-2. 742A-1 and 742A-10K External Calibration Connections

13. If you press PREV MENU, control reverts to the menu in step 3. If you press the "PROCEED" softkey, the 5700A saves the settings in temporary memory for future storage in nonvolatile memory. Calibration continues with internal-only calibration steps.

14. Calibration is not effective until you store the newly-calculated constants in memory. To store the constants, set the rear panel CALIBRATION switch to ENABLE, then press the "Store Values" softkey.

NOTE

You can print a listing of the proposed output shifts to review them before storing the new constants. To print the listing, press the "Print Output Shifts" softkey.

15. After you store the constants, press the "DONE with cal" softkey to exit the calibration menu and resume normal operation. If you press this softkey before storing the constants, the process is aborted without updating existing calibration constants.

16. Set the rear panel CALIBRATION switch to NORMAL.

3-4. Wideband AC Module (Option 5700A-03) Calibration

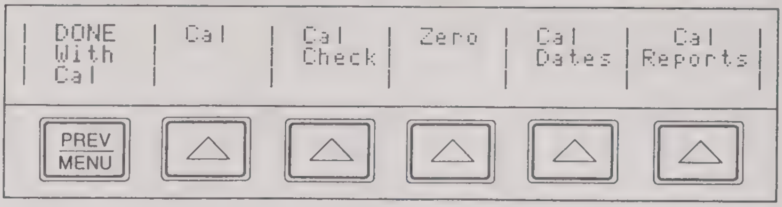
The Wideband AC Module (Option 5700A-03) requires two kinds of calibration: gain and flatness. Gain should be calibrated at the same time as routine calibration of the 5700A main output functions.

Because frequency flatness is determined by such stable parameters as circuit geometry and dielectric constants, flatness of the Wideband AC module has excellent long-term stability. This stability gives the Wideband AC Module a two-year calibration cycle for flatness calibration. Flatness calibration is required only infrequently, and can be done when the 5700A is returned to a standards laboratory for periodic verification. The wideband gain calibration procedure is presented here. The wideband flatness calibration procedure is presented later in this section under "Full Verification".

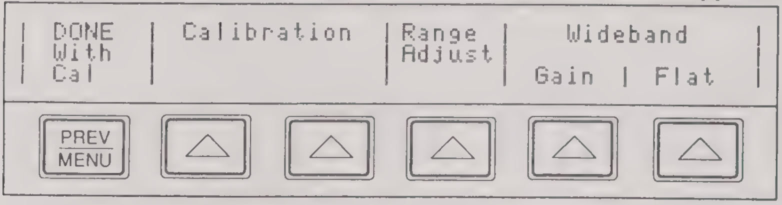
Proceed as follows to calibrate wideband gain:

1. Verify that the 5700A has warmed up for at least 30 minutes.

2. Press the "Setup Menus" softkey then the "Cal" softkey. The calibration menu appears:

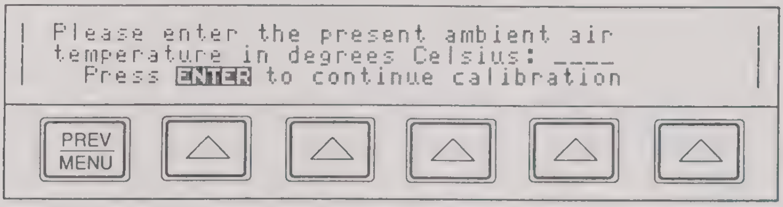

DONE With Cal
Cal
Cal Check
Zero
Cal Dates
Cal Reports
PREV MENU

3. Press the "Cal" softkey. The calibration menu appears:


DONE With Cal
Calibration
Range Adjust
Wideband
Gain
Flat
PREV MENU

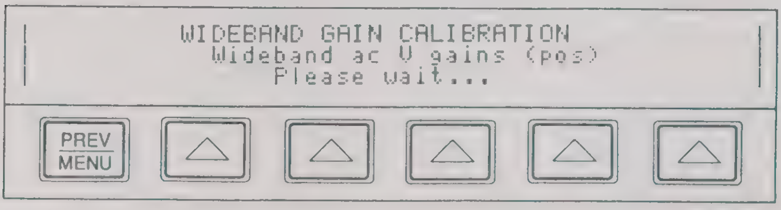
4. Connect the wideband output cable between the WIDEBAND connector and the SENSE binding posts with the center conductor of the 50 ohm feedthrough going to SENSE HI as Figure 3-3 shows. The GND tab on the adapter should be on the LO side.

5. Press the "Gain" softkey. The display changes to:



```
Please enter the present ambient air
temperature in degrees Celsius: ____
  Press ENTER to continue calibration
```

6. Enter the ambient temperature, and press ENTER. The display changes to:



```
WIDEBAND GAIN CALIBRATION
 Wideband ac V gains (pos)
     Please wait...
```

As wideband gain calibration proceeds, messages appear on the display identifying all processes as they are encountered. When positive gains calibration is complete, a message appears telling you to refer to the manual for negative gains connections.

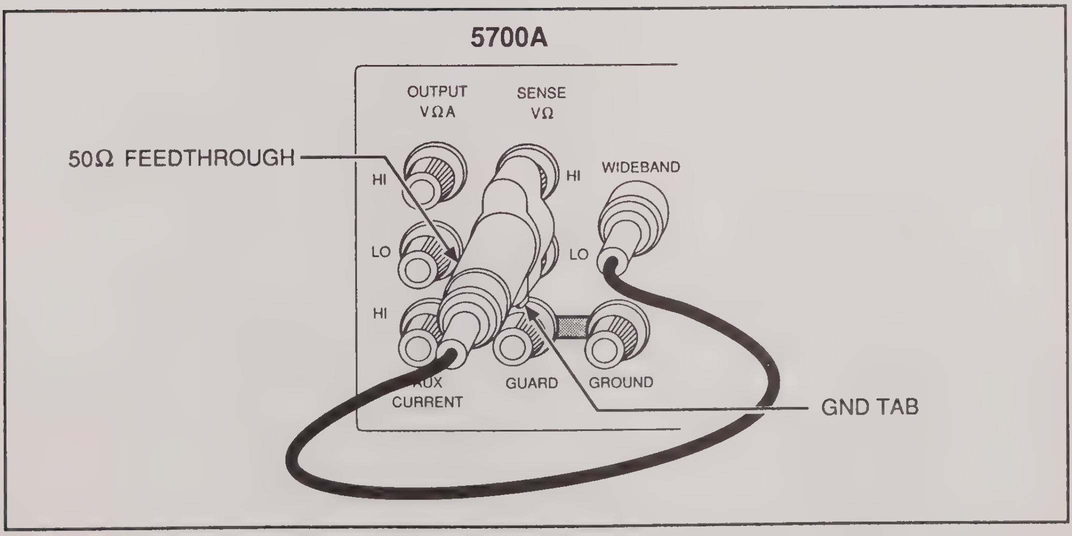
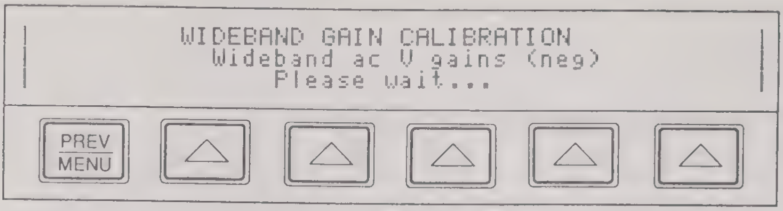

5700A
OUTPUT
VΩA
SENSE
VΩ
50Ω FEEDTHROUGH
HI
HI
WIDEBAND
LO
LO
HI
AUX
CURRENT
GUARD
GROUND
GND TAB

Figure 3-3. Wideband Module Calibration Connection

7. Reverse the dual-banana connector so that the center conductor is connected to LO and press ENTER. The display changes to:


WIDEBAND GAIN CALIBRATION
Wideband ac V gains (neg)
Please wait...

A message announces that wideband gains calibration is done.

8. To store the new constants, set the CALIBRATION switch to ENABLE and press "Store values". If you do not wish to make wideband gains calibration effective, press "DONE with cal" and answer "YES" to the next display that asks for verification.

9. Calibration is finished. Set the CALIBRATION switch to NORMAL, disconnect the wideband cable, and press RESET.

3-5. Doing a Calibration Check

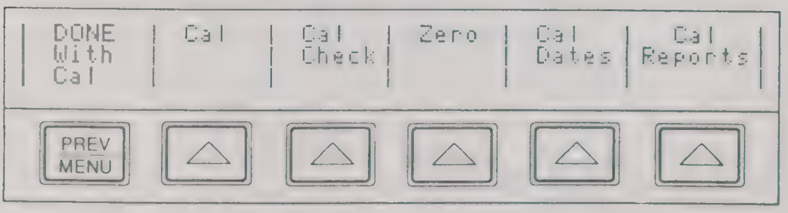
Calibration check is similar to calibration except that no changes are made to stored constants, and the internal check standards are used as the reference points. Calibration check produces a report similar to normal calibration, showing proposed changes. Because calibration check does not change stored calibration constants, there is no need to enable the rear panel CALIBRATION switch. The procedure can be done by an external computer, completely unattended by a person. (See Section 5 of the 5700A Operator Manual for a calibration check remote program example.)

You can use calibration check at any time to confirm the integrity of the 5700A's state of calibration without having to connect external standards. You can also use calibration check as a powerful performance history gathering tool.

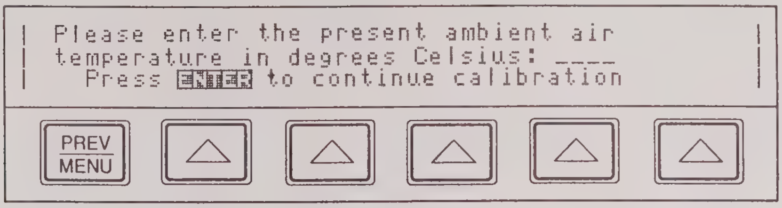
Proceed from the power-up state as follows to do a calibration check:

1. Turn on the 5700A, and allow it to warm up for at least 30 minutes.

2. Press the "Setup Menus" softkey, then press the "Cal" softkey. The calibration menu appears:

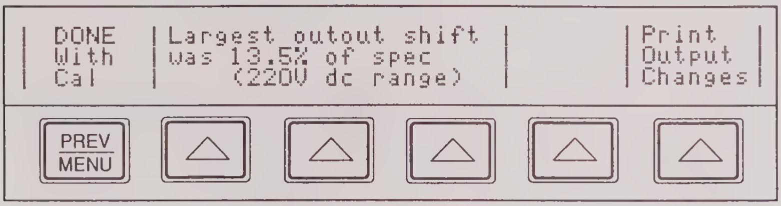


3. Press the "Cal Check" softkey. The display changes to:



```
| Please enter the present ambient air         |
| temperature in degrees Celsius: ____          |
|   Press ENTER to continue calibration         |
```

4. Enter the ambient temperature and press ENTER. As calibration check proceeds, messages appear on the display identifying all processes as they are encountered. When the whole process is complete, the display shows the largest shift detected:



```
| DONE  |Largest outout shift |          |Print  |
| With  |was 13.5% of spec    |          |Output |
| Cal   |     (220V dc range) |          |Changes|
```

5. At this point you can print a listing of the proposed shifts or you can quit. To return to normal operation, press the "DONE with check" softkey.

   To print a calibration check report, Press the "Print Output Changes" softkey.

6. Press PREV MENU to exit the calibration menu.

3-6. Range Calibration

After calibration, you can make further fine adjustments to each range if you wish by adjusting a range constant. This is called Range Calibration. A range constant is an additional gain multiplier for each range. Range adjustments are optional; they are not necessary to meet total uncertainty specifications. However, they do allow you to align the 5700A closer to your standards.

To adjust a range constant, you use your own laboratory standard. This procedure is designed to work for laboratory standard values that are greater than or equal to 45% of the range full-scale value and less than or equal to 95% of the range full-scale value. The new range constant is active until the next calibration event. Every time you calibrate the 5700A, all range constant multipliers are reset to 1.

The procedure to adjust a range constant is menu driven, similar to normal calibration. Many different types of standards in many different configurations can be used for the different functions and ranges. For example, you can adjust the 220V dc range using the following equipment:

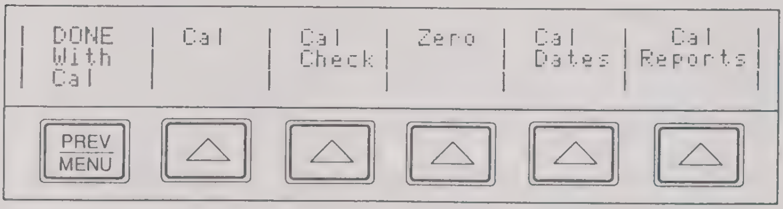
- o 732A DC Reference Standard
- o 752A Reference Divider
- o 845AB/845AR Null Detector
- o 5440B-7002 Low Thermal Test Leads (three sets)

A procedure to adjust the 220V dc range constant using the above equipment is described here. You can use your own laboratory standards to adjust other range constants similarly.

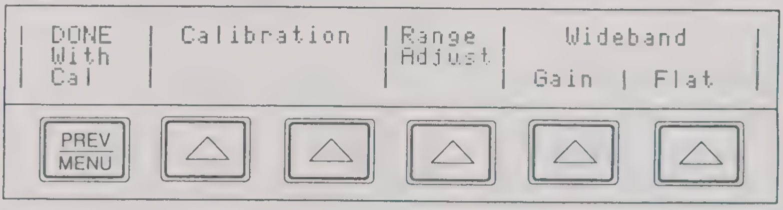
Proceed as follows to adjust the 220V dc range constant:

1. Perform calibration to external standards as described previously in this section.

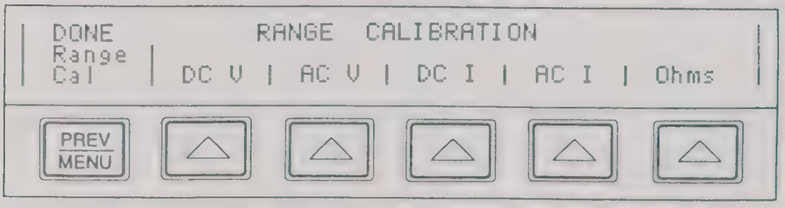
2. Press the "Setup Menus" softkey, then press the "Cal" softkey. The calibration menu appears:


DONE With Cal
Cal
Cal Check
Zero
Cal Dates
Cal Reports
PREV MENU

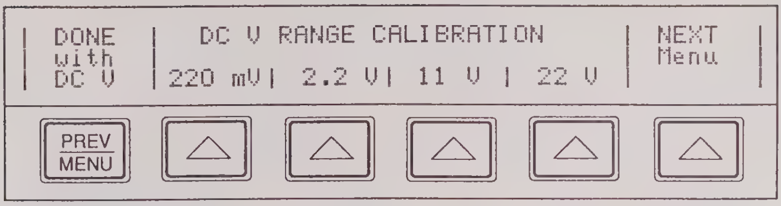
3. Press the "Cal" softkey. The display changes to:


DONE With Cal
Calibration
Range Adjust
Wideband
Gain
Flat
PREV MENU

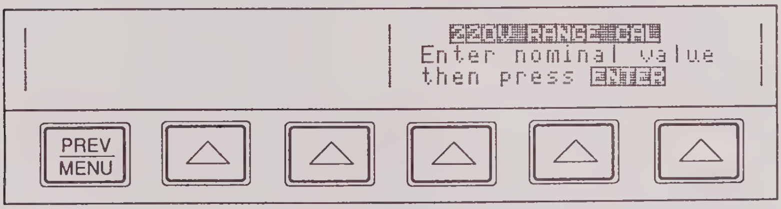
4. Press the "Range Adjust" softkey. The display changes to:


DONE Range Cal
RANGE CALIBRATION
DC V
AC V
DC I
AC I
Ohms
PREV MENU

5. Press the "DC V" softkey. The display changes to:

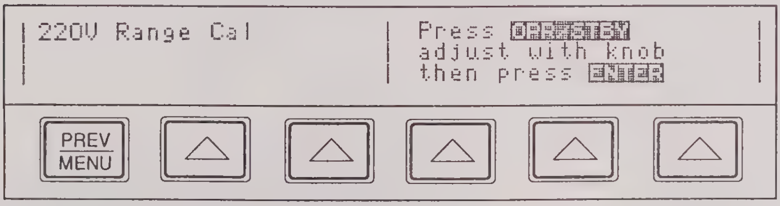


6. All the ranges for dc voltage are presented in a series of menus. Pressing the "NEXT Menu" softkey scrolls through the choices. Press "NEXT Menu" until "220 V" appears, then press its softkey.


220V RANGE CAL
Enter nominal value
then press ENTER

7. Connect the 732A, 845A, and 752A in a 10:1 configuration as Figure 3-4 shows.

8. Enter the value of the 732A multiplied by 10. (This is the output of the 752A to which you will null the output of the 5700A.) When you press ENTER, the display changes to:


220V Range Cal
Press OPR/STBY
adjust with knob
then press ENTER

9. Press OPR/STBY to activate the calibrator output.

10. Rotate the 5700A output adjustment knob to achieve a null on the 845A Null Detector.

11. Set the rear panel CALIBRATION switch to ENABLE.

12. Press ENTER. This causes the 5700A to calculate a new range constant multiplier for the 220V dc range and store it in nonvolatile memory.

13. Range calibration is complete. Set the rear panel CALIBRATION switch to NORMAL, disconnect the external standards, and press RESET.

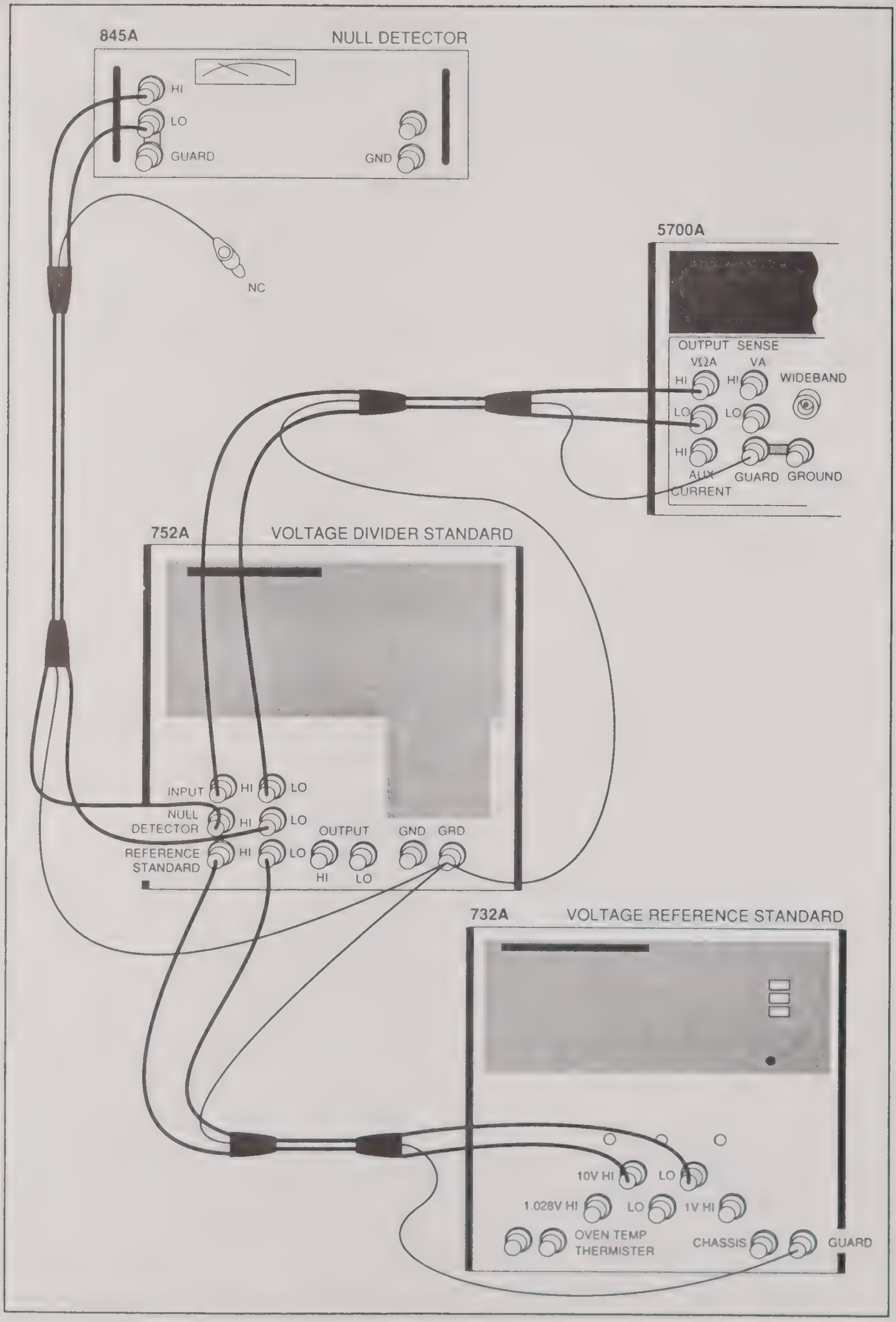

845A
NULL DETECTOR
HI
LO
GUARD
GND
NC
5700A
OUTPUT SENSE
VΩA
VA
HI
HI
WIDEBAND
LO
LO
HI
AUX
CURRENT
GUARD
GROUND
752A
VOLTAGE DIVIDER STANDARD
INPUT
HI
LO
NULL DETECTOR
HI
LO
REFERENCE STANDARD
HI
LO
OUTPUT
HI
LO
GND
GRD
732A
VOLTAGE REFERENCE STANDARD
10V HI
LO
1.028V HI
LO
1V HI
OVEN TEMP THERMISTER
CHASSIS
GUARD

Figure 3-4. 220V DC Range Calibration Connections

3-7. FULL VERIFICATION

An independent external verification is recommended every two years, following a normal periodic calibration. Verification establishes and maintains parallel external, traceability paths for the internal functions that are not adjusted or corrected during calibration. An example is the internal ac/dc transfer standard. Verification also serves as a check that internal calibration processes are in control.

NOTE

All performance limits specified in the test records apply to 90-day specifications for the 5700A. If limits to other specifications are desired, the test records must be modified.

Before beginning verification, make copies of the Test Record (Table 3-27) (Table 3-27) located at the end of this section. Due to the state of the art performance of the 5700A, it is necessary to record test data for many of the tests for use as characterized values in subsequent tests. Many of the performance limits are shown only on the test record rather than in the body of the text. This allows an experienced technician to use the test record as an abbreviated version of the test procedure.

3-8. Required Equipment for All Tests

An abbreviated summary of required equipment for all the verification and optional tests is given in Table 3-2. Individual lists of required equipment are included at the beginning of each test. For substitution information, refer to Table 3-26, Minimum Use Requirements, located near the end of this section.

Table 3-2. List of Required Equipment for Main Output Tests

MFR.	MODEL	DESCRIPTION	APPLICATION
Fluke	742A Series	Resistance Standards	Cal, ohms, DC
Fluke	752A	Reference Divider	DC V
Fluke	845A	Null Detector	DC V
Holt	11	Thermal Voltage Conv.	AC V
Fluke	540B	Thermal Transfer Std.	AC V, AC
Fluke	5100B	Calibrator	Ohms
ESI	DT72A	Ratio Transformer	mV AC
Philips	PM6669	Frequency Counter	Frequency
Fluke	A40 Series	Shunts	AC
Fluke	Y5020	High Current Shunt	DC
L&N	0.1 Ohm	Standard Resistor	DC
Fluke	931B	RMS Differential Vm.	mV AC
Fluke	8922A	RMS Wideband Voltmeter	mV AC
Fluke	8500 Series	DMM	Ohms, DC
GenRad	874		
or, Narda	777C-20	20 dB RF Atten. (Qty. 3)	mV AC
Fluke	P/N 853429	50 Ohm Termination	mV AC
Fluke	5440-7002	Low Thermal Cables	Various

EQUIPMENT REQUIRED FOR WIDEBAND AC MODULE (OPTION 5700-03) VERIFICATION

MFR.	MODEL	DESCRIPTION	APPLICATION
Fluke	A55-3V	High Freq. Thermal Converter	WB
Narda	777C-20	20 dB RF Attenuator (Qty. 3)	WB
Narda	777C-10	10 dB RF Attenuator (Qty. 1)	WB
Comlinear	CLC100	20 dB Amplifier (Qty. 2)	WB
Fluke	8920A	Wideband RMS Voltmeter	WB mV AC
(Any)		±12V Power Supply	WB

EQUIPMENT REQUIRED FOR OPTIONAL TESTS

MFR.	MODEL	DESCRIPTION	APPLICATION
Tektronix		Scope Mainframe	HF Noise
Tektronix	7A22	Differential Amplifier	HF Noise
HP	334A or 8903A	Distortion Analyzer	AC V, AC, Dist.
Tektronix	7L12	Spectrum Analyzer	AC V, WB, HF Dist.
Fluke	720A	Kelvin Varley	DC V Linearity

3-10. Warmup Procedure For All Verification Tests

Before performing verification, do the following things:

1. Verify that the 5700A has warmed up for at least thirty minutes.
2. If you are doing a regularly scheduled full verification as recommended by Fluke, calibrate the 5700A as previously described before continuing with verification.
3. Ensure that each piece of external test equipment has satisfied its specified warmup requirements.
4. Ensure that the 5700A is in standby (STANDBY annunciator lit).

3-11. Resistance Verification Test

The following test requires testing at the high, low and intermediate values only. This is because the 5700A creates the other values of resistance from these values. For the convenience of anyone wishing to test the intermediate values, the tolerance limits are included. Testing these values could be done using a Hammon-type ratio device and a very stable, high-resolution bridge or DMM, or a combination of the two. Table 3-3 lists equipment required for this test. See Table 3-26, Minimum Use Requirements, for substitution information.

Table 3-3. Equipment Required for Resistance Testing

EQUIPMENT	DESCRIPTION
Standard Resistors	Fluke 742A Series in the following values: 1 ohm, 10 ohm, 10 kilohm, 19 kilohm, 10 megohm, and 19 megohm
Current Source	Fluke 5100B, 5700A, or EDC CR103/J
DMM	Fluke 8500 Series

1. Connect the equipment as shown in Figure 3-5.
2. Set the 5700A output to 1 ohm with external sensing (EX SENS indicator lit) and set the dc DMM to read dc V. Record the 1 ohm standard resistor value on the test record as the "1 Ohm Standard Resistor Value."
3. Multiply the certified value of the 1 ohm standard resistor by 0.1 and record the result on the test record as the "1 Ohm Standard Voltage."
4. Connect the DMM across the sense terminals of the 1 ohm standard resistor.

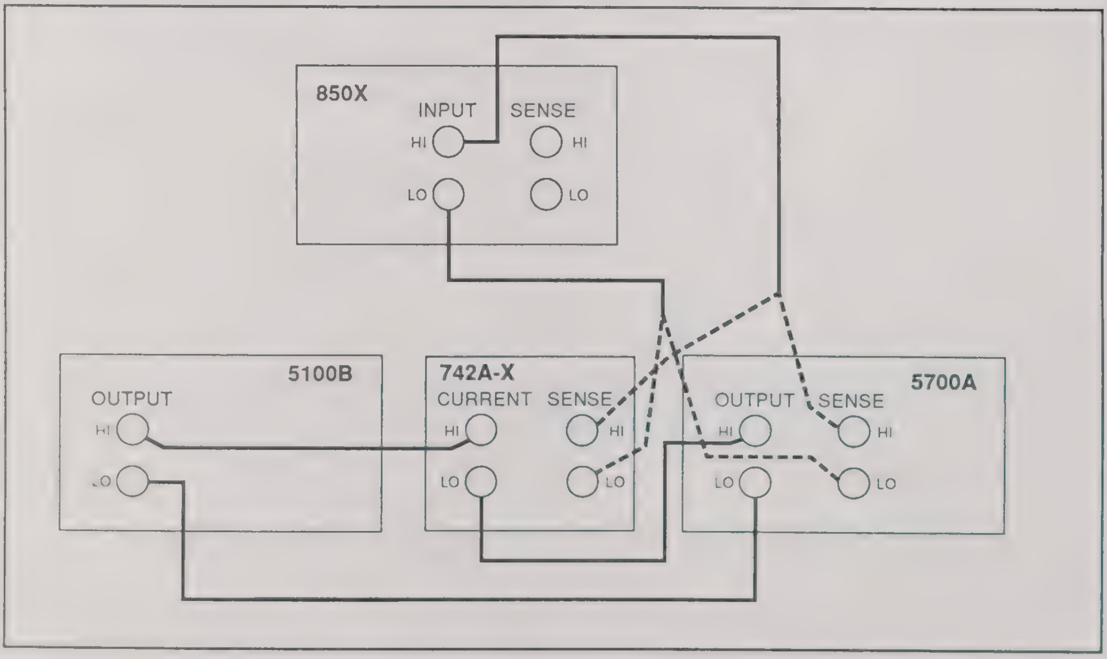

850X
INPUT
SENSE
HI
HI
LO
LO
5100B
OUTPUT
HI
LO
742A-X
CURRENT
SENSE
HI
HI
LO
LO
5700A
OUTPUT
SENSE
HI
HI
LO
LO

Figure 3-5. 1 Ohm and 10 Ohm Resistor Verification

5. Set the direct current source for a nominal 100 mA output. Vary the source until the DMM reading is as close as possible to the 1 ohm Standard Voltage recorded in the previous step. Record the DMM voltage reading on the test record as the "Measured 1 Ohm Standard Voltage."

6. Calculate the exact current by dividing the "Measured 1 Ohm Standard Resistance Value"; record the result on the test record as the "Calculated Current."

7. Enter the 5700A displayed 1 ohm value on the test record as the "UUT 1 ohm Displayed Value."

8. Transfer the dc DMM leads to the 5700A sense terminals.

9. Enter the DMM voltage reading on the test record as the "UUT 1 Ohm Voltage."

10. Calculate the UUT true 1 ohm resistance by dividing the "UUT 1 Ohm Voltage" by the "Cal Current."

11. Edit the 5700A "Reading = ###" on the Control Display to the true 1 ohm resistance value calculated in the previous step. The error from the displayed value is also shown on the Control Display. Enter the value of the error (with polarity reversed) on the test record as the "UUT Deviation from Displayed Value."

12. Repeat steps 3 through 11 for the 10 ohm resistance using the 10 ohm standard resistor 10 mA of current.

13. The low-value (1 ohm and 10 ohm) tests are summarized in Table 3-4.

Table 3-4. Low Value Resistance Calibration Using a Current Source

5700A RESISTANCE	APPLIED CURRENT	5700A DEVIATION FROM DISPLAYED VALUE	5700A DISPLAYED VALUE
1 ohm	100 mA	±95 ppm	0.9995 to 1.0005
10 ohm	10 mA	±28.0 ppm (90-day spec.)	9.997 to 10.003

14. For the remaining tests, no current source is required. Verify that each true 5700A value is within the limits shown in Table 3-5.

    - Connect the DMM, set for 4-wire resistance, first to the Standard Resistor equal to the 5700A nominal output and then to the 5700A. In each case, record the standard resistor DMM reading and the standard resistor certified value.

    - Calculate the DMM correction by subtracting the DMM reading from the certified value; enter this calculated value on the test record as "DMM Error."

    - Move the DMM to the 5700A (UUT) terminals; enter the DMM reading on the test record as "DMM UUT Resistance Reading."

    - Algebraically add the "DMM Error" and the "DMM UUT Resistance Reading"; enter the sum on the test record as "UUT True Resistance Value."

    - Edit the 5700A "READING - ###" on the Control Display to the true resistance value previously calculated. The error from the displayed value is also shown on the Control Display. Enter this error (with polarity reversed) on the test record as the "UUT Deviation from Displayed Value."

Table 3-5. Resistance Test Summary

1 OHM STD RES VALUE	1 OHM STD VOLTAGE	MEASURED 1 OHM STD VOLTAGE	CAL CURRENT	UUT 1 OHM DISPLAYED VALUE	UUT 1 OHM VOLTAGE	UUT TRUE RES.	UUT DEVIATION FROM DISPLAYED VALUE	LIMIT OF DEVIATION FROM DISPLAYED VALUE	MAXIMUM DIFFERENCE OF CHARACTERIZED TO NOMINAL VALUE
								+/-94 ppm	.9995 to 1.0005

10 OHM STD RES VALUE	10 OHM STD VOLTAGE	MEASURED 1 OHM STD VOLTAGE	CAL CURRENT	UUT 1 OHM DISPLAYED VALUE	UUT 1 OHM VOLTAGE	UUT TRUE RES.	UUT DEVIATION FROM DISPLAYED VALUE	LIMIT OF DEVIATION FROM DISPLAYED VALUE	MAXIMUM DIFFERENCE OF CHARACTERIZED TO NOMINAL VALUE
								+/-28.5 ppm	9.997 to 10.003

RESISTANCE ACCURACY VERIFICATION (19 OHM AND ABOVE)

	STD RES VALUE	DMM STD RES RDG	DMM ERROR	DMM UUT RES RDG	UUT TRUE RES VALUE	UUT DEVIATON FROM DISPLAYED VALUE		
19 ohm (1)							+/-26 ppm	18.9943 to 19.0057
100 ohm (1)							+/-17 ppm	99.985 to 100.015
190 ohm (1)							+/-17 ppm	189.9715 to 190.0285
1 kilohm (1)							+/-12 ppm	999.85 to 1000.15
1.9 kilohm (1)							+/-12 ppm	1.899715k to 1.900285k
10 kilohm							+/-11 ppm	9.9985k to 10.0015k
19 kilohm							+/-11 ppm	18.99715k to 19.00285k
100 kilohm (1)							+/-13 ppm	99.985k to 100.015k
190 kilohm (1)							+/-13 ppm	189.9715k to 190.0285k
1 megohm (1)							+/-18 ppm	0.9998M to 1.0002M
1.9 megohm (1)							+/-19 ppm	1.89962M to 1.90038M
10 megohm							+/-37 ppm	9.997M to 10.003M
19 megohm							+/-47 ppm	18.9943M to 19.0057M
100 megohm (2)							+/-120 ppm	99.95M to 100.05M

Note 1: Not necessary to test due to 5700A internal calibration process.

Note 2: Due to extremely slow settling time (approximately 5 minutes to 0.005% and sensitivity to any nearby movement, use of the DMM to test 100 megohms to the specified 0.01% uncertainty is not practical and therefore is not recommended. For those who wish to test it, a suitable way is to use an ESI SR 1050 10M/step Hammon-type Resistance Transfer Standard and use it in conjunction with an ESI 242-series bridge to effect the measurement to the required uncertainty.

3-12. Two-Wire Compensation Verification

Use the following steps to verify that two-wire compensation operates correctly:

1. Connect the 5700A (UUT) (output set to 100 ohm, with external sensing) to the DMM (set for 4-wire resistance measurement). Note the DMM reading.
2. Connect two shorts: DMM SOURCE HI to SENSE HI and DMM SOURCE LO to SENSE LO.
3. Activate 5700A (UUT) 2-wire compensation.
4. Check that the DMM reading returns to within 4 milliohm of the reading noted in step 1.

3-13. DC Voltage Verification Test

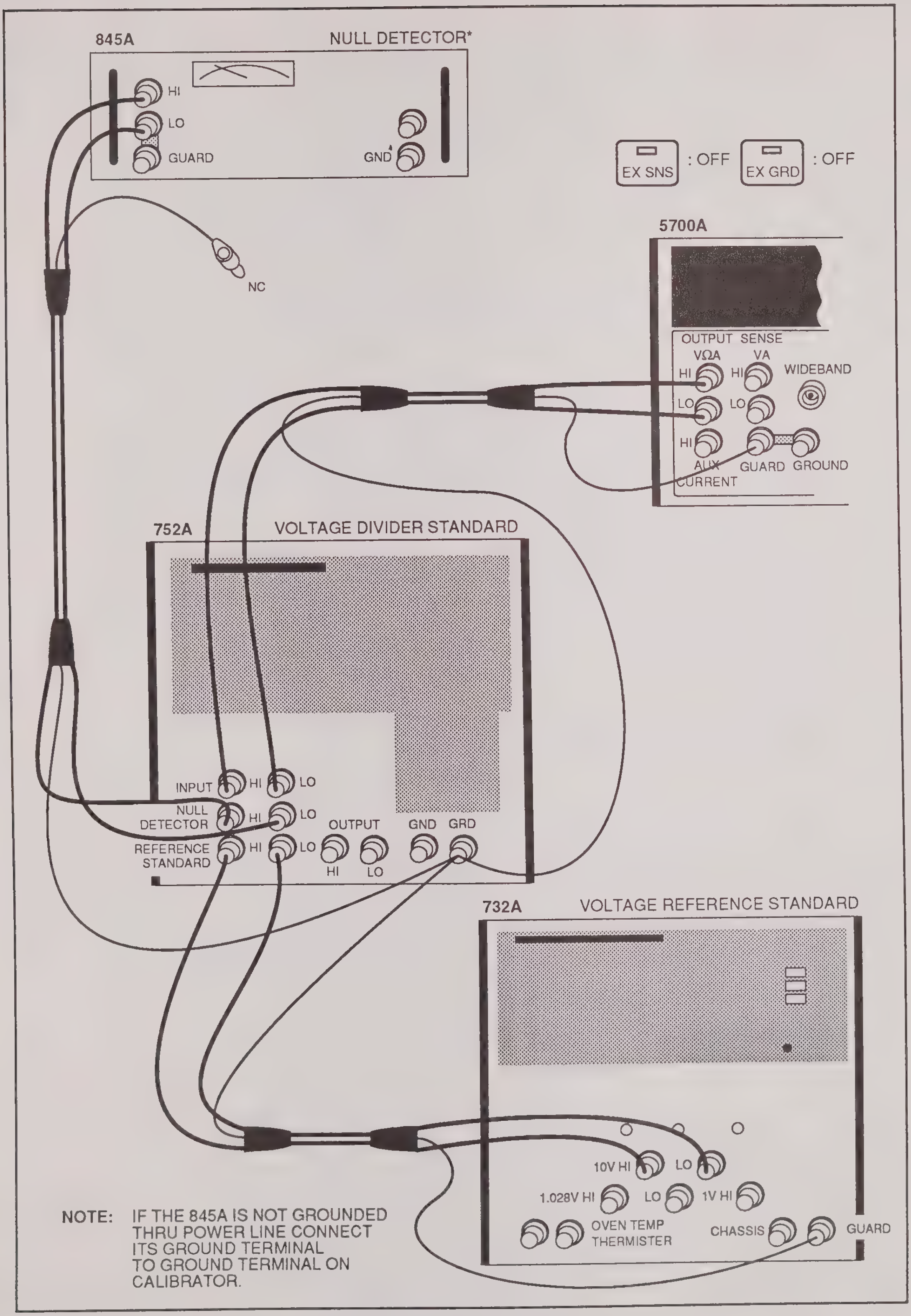
The following test checks every dc voltage range by testing the output accuracy at decade values of voltage from 100 mV to 1000V. Table 3-6 lists equipment required for this test as well as the Linearity Test that follows. See Table 3-26, Minimum Use Requirements, for equipment substitution information.

Table 3-6. Equipment Required for DC Voltage Testing

EQUIPMENT	MODELS
DC Reference Standard	Fluke 732A
Reference Divider	752A
Null Detector	845A(B or R)

Proceed as follows to perform the dc voltage verification test:

1. Connect the equipment as shown in Figure 3-6.
2. Set the reference divider to 0.1V. Set the 5700A to the certified value of the dc reference standard divided by 100. For example, if the the certified value of the dc reference standard is 10.000007V, set the 5700A to 100.00007 mV.
3. Press OPR/STBY. After the reading has settled, verify that the null detector reads 0V ±1.45 uV (the 90-day specification). Set the 5700A to standby.
4. Repeat the above process to test each 5700A dc voltage range output listed in Table 3-7. (0.1V is in the table for completeness; you do not need to repeat it.) After the null detector reading stabilizes, ensure that any observed meter rattle over a ten-second period does not exceed the amount shown in the last column. In each case, set the 5700A to standby before changing to the next voltage settings and go back to operate before reading the null detector.


845A
NULL DETECTOR*
HI
LO
GUARD
GND
NC
EX SNS
: OFF
EX GRD
: OFF
5700A
OUTPUT SENSE
VΩA
VA
HI
HI
WIDEBAND
LO
LO
HI
AUX CURRENT
GUARD
GROUND
752A
VOLTAGE DIVIDER STANDARD
INPUT
HI
LO
NULL DETECTOR
HI
LO
OUTPUT
GND
GRD
REFERENCE STANDARD
HI
LO
HI
LO
732A
VOLTAGE REFERENCE STANDARD
10V HI
LO
1.028V HI
LO
1V HI
OVEN TEMP THERMISTER
CHASSIS
GUARD

NOTE: IF THE 845A IS NOT GROUNDED THRU POWER LINE CONNECT ITS GROUND TERMINAL TO GROUND TERMINAL ON CALIBRATOR.

Figure 3-6. DC Voltage Verification Test

Table 3-7. Output Voltage Test Summary

DIVIDER SETTING	5700A RANGE	5700A OUTPUT (NOTE # 1)	NULL DETECTOR READING (uV)	NULL DET LIMIT (uV p-p)	METER LIMIT (uV) RATTLE
0.1V	0.22V	0.1V		±1.45 uV (# 2)	NA
1V	2.2V	1V		±7.2 uV (# 2)	0.55 uV
1V	11V	1V (# 3)		±9 uV (# 2)	2.2 uV
10V	11V	10V (# 4)		±54 uV	3.5 uV
10V	22V	10V (# 3)		±58 uV	5.5 uV
100V	220V	100V		±70 uV	7.5 uV
1000V	1100V	1000V		±86 uV	4.5 uV

TABLE NOTES

Note 1: On the 752A 0.1 and 1V ranges, the null detector polarity is reversed. A low input (5700A output) causes a positive null detector reading.

Note 2: Mathematically, the true 5700A output programmed is the certified value of the reference standard divided by the reference standard nominal value, multiplied by the required 5700A nominal output. In other words, the 5700A output is always programmed for the nominal output adjusted up or down by the same percentage as the certified value of the reference standard.

Note 3: Use Range Lock to obtain 1V on 11V and 10V on 22V range. Deactivate Range Lock before setting the next voltage output.

Note 4: Line regulation can be verified at this time by adjusting the autotransformer for a ±10% change in line voltage. The null detector reading must remain constant within ±1 uV.

5. Reverse the connections of the dc reference standard at the reference divider and repeat the previous measurement process for the -0.1V and -10V 5700A outputs only.

3-14. DC Voltage One-Tenth Scale Linearity Test

NOTE

If the result of the previous test at 1V on the 11V range was less than 2.5 uV it is not necessary to perform this test.

This test uses the same equipment as the previous test. Proceed as follows to perform the DC Voltage One-Tenth Scale Linearity Test:

1. Set the reference divider range to 10V. On the voltage reference standard, remove the lead from the 10V high terminal and connect it under the binding post of the low terminal along with the low lead to provide a 0V reference input to the reference divider. Set the 5700A output for 10V, then activate range lock for the 11V range. Now set the 5700A to 0V OPERATE.
2. Note the reading on the null detector. Press OFFSET on the 5700A. Return the lead on the voltage reference to the high output terminal.
3. Set the 5700A to 10V. Use the knob to adjust the 5700A output for the reading previously noted on the null detector. Press SCALE on the 5700A.
4. Set the reference divider to the 1V range. Set the 5700A to 1V dc and verify that the null detector indicates less than 2.5 uV from the noted reading.
5. Press RESET on the 5700A. This completes the DC Voltage Calibration Verification testing.

3-15. AC Voltage Frequency Accuracy Test

This test requires the use of a frequency counter. Philips model PM6669 is recommended. Refer to Table 3-26, Minimum Use Requirements, for substitution information.

To check the 5700A frequency accuracy, proceed as follows:

1. Connect the frequency counter to the output terminals of the 5700A.
2. Set the 5700A to 1V at the output frequencies listed in Table 3-8. Verify that the counter reads within the limits shown on the test record.

Table 3-8. AC Voltage Frequency Accuracy

FREQUENCY	TOLERANCE	ACTUAL
10 Hz	99.99 ms - 100.01 ms	
15 Hz	66.673 ms - 66.66 ms	
100 Hz	9.999 ms - 10.001 ms	
200 Hz	199.98 Hz - 200.02 Hz	
500 Hz	499.95 Hz - 500.05 Hz	
1 kHz	999.9 Hz - 1000.1 Hz	
5 kHz	4999.5 Hz - 5000.5 Hz	
10 kHz	9.999 kHz - 10.001 kHz	
140 kHz	139.986 kHz - 140.014 kHz	
200 kHz	199.98 kHz - 200.02 kHz	
500 kHz	499.95 kHz - 500.05 kHz	
1 MHz	0.9999 MHz - 1.0001 MHz	

3. Disconnect the counter from the 5700A.

3-16. Output Level Tests for AC V Ranges 2V and Above

This test requires the use of equipment listed in Table 3-9.

Table 3-9. Equipment Required for AC V Output Level Tests

Holt 11 Thermal Voltage Converter
Fluke 540B Thermal Transfer Standard
GR874 to male banana adapter
Coaxial cable from TVC output to High Freq Converter input of 540B

NOTE

Before beginning this test, refer to the Certified Report of Calibration for the transfer standard for corrections. If its corrections are 10 ppm or greater, enter them on the test record and use them to correct the results of this test to obtain a reference transfer standard indication. Enter any required corrections at this time in + or - ppm in the space provided for on the test record for each level and frequency.

1. Select a transfer standard 2V input range.

2. Connect the equipment as shown in Figure 3-7. To protect the Holt 11 from over voltage, set the limits on the 5700A to +2.002V and -2.002V.

   NOTE

   If a GR 874 to male banana adapter is not available, you can use a GR 874 to banana female adapter and wires of 12 gauge or heavier no more than 2 inches in length tightened securely under the terminals to attach the 5700A to the Holt 11. Support the Holt as necessary.

3. Set the 5700A for 2V dc. Press OPR/STBY.

4. Allow sufficient time (usually around 10 minutes for the first reading) for the transfer standard null meter reading to stabilize. Adjust the transfer standard null controls for a precise null indication.

5. Proceed as follows to obtain an average of the reversed dc to obtain a reference for the ac:

   a. Adjust the transfer standard null controls for a null with positive polarity voltage from the 5700A.

   b. Reverse the 5700A output voltage by pressing the 5700A ± key.

   c. Record the final deflection on the transfer standard null meter in + or - small divisions.

   d. Reverse the 5700A output voltage to obtain a positive output. Verify that the null meter returns to a precise null.

   e. Adjust the transfer standard controls to obtain one-half the deflection recorded in step c, but in the opposite direction. For example, if you recorded +4.7 divisions for step c, the correct offset for step e would be -2.4 divisions (rounded to the nearest tenth).

6. Set the 5700A output to 2V at 1 kHz.

7. Without touching the transfer standard null controls, use the knob to adjust the 5700A output as necessary to obtain a null on the Transfer Standard null meter. Record the 5700A error display reading and verify that it is within the limit shown on the test record.

8. Set the 5700A output to +2V dc.

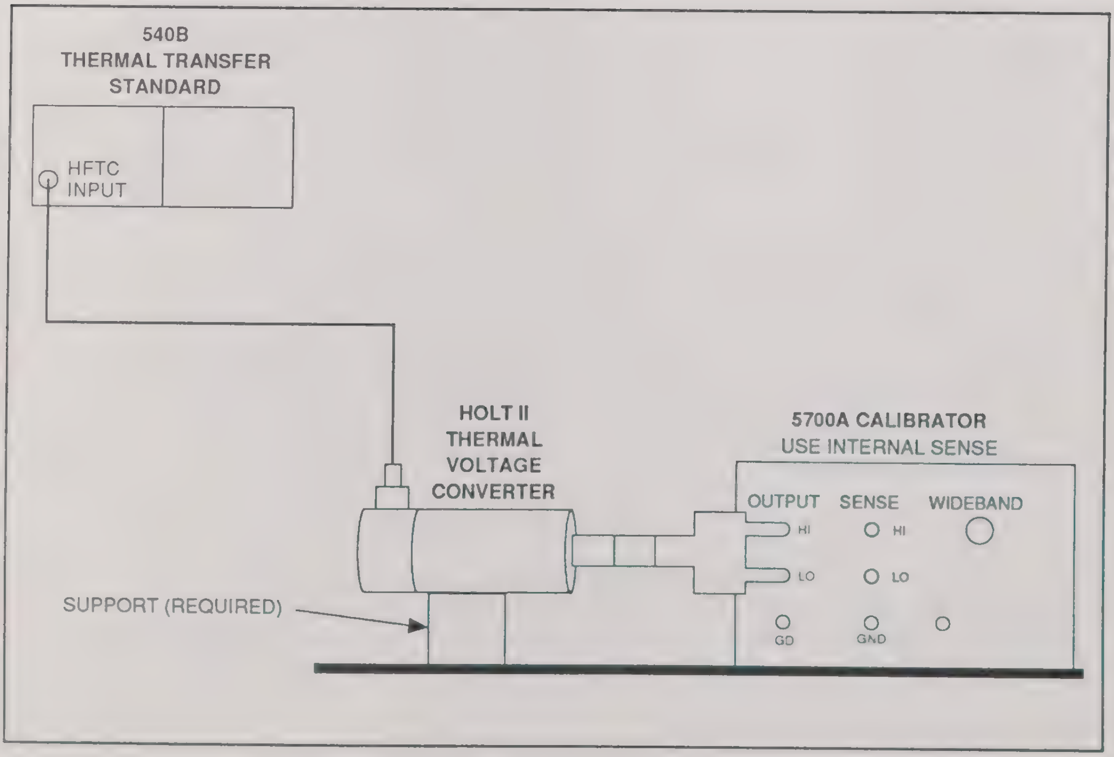

540B
THERMAL TRANSFER
STANDARD
HFTC
INPUT
HOLT II
THERMAL
VOLTAGE
CONVERTER
5700A CALIBRATOR
USE INTERNAL SENSE
OUTPUT
SENSE
WIDEBAND
HI
HI
LO
LO
GD
GND
SUPPORT (REQUIRED)

Figure 3-7. AC Voltage Verification

9. Verify that the null meter offset is within ± 1/2 small division (5 ppm) of that recorded in step 5e. Otherwise, repeat steps 5 through 10 until the required result is achieved.

NOTE

> From this point on, for this range, the test uses an ac/ac transfer technique rather than ac/dc. The test references every frequency back to 1 kHz using the recorded error display reading from step 8 as the reference.

10. With the 5700A set to 2V at 1 kHz, adjust the transfer standard null controls for a null.

NOTE

> Do not adjust the transfer standard controls again until instructed to do so.

11. Set the 5700A to the next frequency listed in Table 3-10 and on the test record. Adjust the 5700A using the knob for a null on the Transfer Standard null meter. Record the 5700A error display reading. Algebraically add the readings to any transfer standard corrections previously entered for 1 kHz and verify that the result is within the limits shown.

12. Repeat steps 10 and 11 for each remaining frequency for this range in Table 3-10 and on the test record.

13. Repeat the preceding process for each remaining range and frequency shown in Table 3-10 and on the test record. Select the required range of transfer standard and program the nominal dc voltage for each range to obtain the reversed dc reference as was done for the 2V range.

    For the 1000V range, remove the Holt TVC and use the 540B directly. The 50 ppm uncertainty at 1000V for the 540B is sufficient to check the 5700A/5725A 1000V range. Alternately, a more accurate check of this range can be made at 600V with the Holt 5 mA thermoelement and the 600V converter.

NOTE

> At 1000V output, the transfer standard used to test the 5700A must draw less than 6 mA. Some single-range transfer standards draw 10 mA (10W dissipation) at this level. Do not use these. Table 3-21, Minimum Use Requirements, recommends alternatives.

Table 3-10. AC Voltage Output Test

FREQUENCY	OUTPUT LEVEL	TRANSFER STANDARD CORRECTION	ERROR DISPLAY READING	CAL ERROR ADDING ERROR 1 kHz	90-DAY SPEC
1 kHz	2V				78.5 ppm
40 Hz	2V				78.5 ppm
20 kHz	2V				78.5 ppm
50 kHz	2V				140 ppm
100 kHz	2V				290 ppm
300 kHz	2V				515 ppm
500 kHz	2V				0.13%
1 MHz	2V				0.27%
20 Hz	2V				185 ppm
10 Hz	2V				600 ppm
1 kHz	2.3V (Note 1)				78.5 ppm
1 kHz	20V				78.5 ppm
40 Hz	20V (Note 2)				78.5 ppm
20 kHz	20V				78.5 ppm
50 kHz	20V				140 ppm
100 kHz	20V				270 ppm
300 kHz	20V				635 ppm
500 kHz	20V				0.155%
1 MHz	20V				0.325%
20 Hz	20V				185 ppm
10 Hz	20V				600 ppm
40 Hz	200V	Stability for 10 minutes: <± 7.5 ppm			
1 kHz	200V				85 ppm
40 Hz	200V				85 ppm
20 kHz	200V				85 ppm
50 kHz	200V				240 ppm
100 kHz	200V				600 ppm
20 Hz	200V				130 ppm
10 Hz	200V				600 ppm
20 kHz	300V (Note 3)				155 ppm
50 kHz	600V (Note 3)				378 ppm
100 kHz	600V (Note 3)				0.1375%
50 Hz	1000V (Note 4)				84 ppm
200 Hz	1000V (Note 4)				84 ppm
500 Hz	1000V (Note 4)				84 ppm
1 kHz	1000V (Note 4)				84 ppm
40 Hz	1000V (Note 3)				84 ppm
20 kHz	1000V (Note 3)				131 ppm

Table 3-10. AC Voltage Output Test (cont)

TABLE NOTES

Note 1: This is a test of the bottom of the 20V range and will require re-referencing at 2.3 V dc.

Note 2: Observe the 5700A output at 20V, 40 Hz for 10 minutes and verify it remains stable within ± 7.5 ppm. Return to 1 kHz and algebraically subtract from the reading any drift caused by the element.

Note 3: Perform only for units with 5725A Amplifier attached. At 600V, use the 500V range on the 540B.

Note 4: Maximum load current is 6 mA for 1 kV range without a 5725A attached.

3-17. AC Voltage mV Ranges Output Level Test

The following test uses the just-measured 5700A 2V range and a ratio transformer to establish absolute millivoltage levels at 1 kHz on an rms differential voltmeter (200 mV and 20 mV) and an rms wideband voltmeter dc DMM combination (2 mV). These meters are used as transfer devices. The rms meters measure the absolute voltage on each 5700A millivolt range. Then 20 dB rf attenuators are connected between the 5700A output and an rms meter input. Using the corrections for the 5700A 2V range, if necessary, the 5700A output is maintained constant into the 20 dB rf attenuators. In this way, the rms meters are characterized for frequency response. Once characterized, the rms meters measure the 5700A millivolt ranges directly for frequency response from the characterized absolute 1 kHz reference. Use Table 3-11 or the test record for these tests.

3-18. ABSOLUTE LEVEL VERIFICATION AT 1 kHz (200 mV, 20 mV, AND 2 mV)

1. Connect the equipment as shown in Figure 3-8.
2. Set the 5700A for a 2V, 1 kHz output and adjust the error display for the reading recorded in step 7 of the Output Level Tests for AC Voltage Ranges 2V and Above.
3. Set the ratio transformer to 0.1, and adjust the rms differential voltmeter dials for a null. Record the dial setting as the "200 mV" reading on the test record.
4. Set the ratio transformer to 0.01 and adjust the rms differential voltmeter dials for null. Record the dial setting as the "20 mV" reading on the test record.
5. Substitute the rms wideband voltmeter (with the dc DMM connected to its output) for the rms differential voltmeter in the test setup. Switch in the 8922 filter.

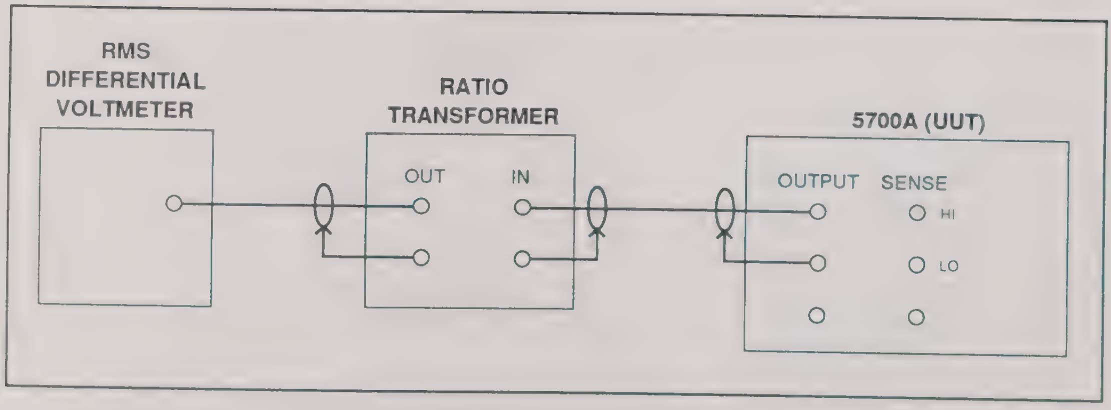

RMS
DIFFERENTIAL
VOLTMETER
RATIO
TRANSFORMER
OUT
IN
5700A (UUT)
OUTPUT
SENSE
HI
LO

Figure 3-8. Absolute Level Verification at 1 kHz (200 mV and 20 mV)

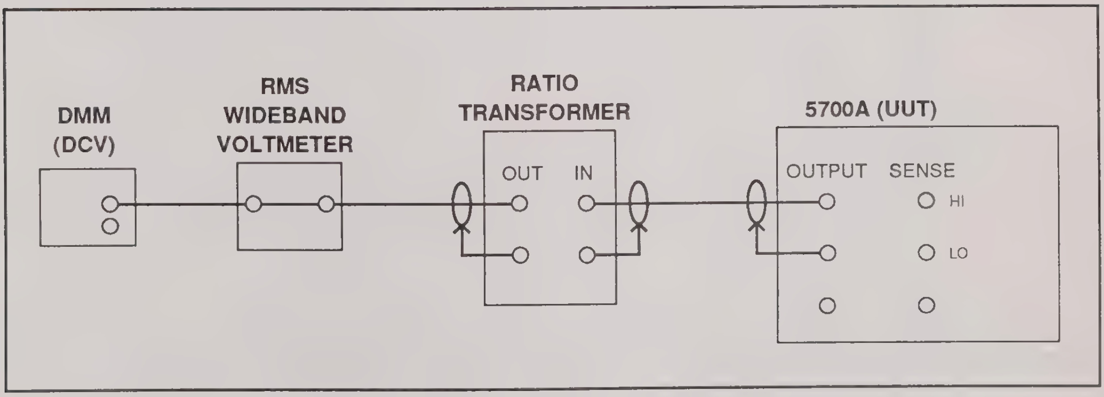

DMM
(DCV)
RMS
WIDEBAND
VOLTMETER
RATIO
TRANSFORMER
OUT
IN
5700A (UUT)
OUTPUT
SENSE
HI
LO

Figure 3-9. Absolute Level Verification at 1 kHz (2 mV)

6. Set the ratio transformer to 0.001 and record the dc DMM "2 mV" reading on the test record.

7. Disconnect the ratio transformer from the setup. Use the characterized rms meters to measure and record the 5700A 1 kHz outputs at each characterized 1 kHz voltage level of 2 mV, 20 mV, and 200 mV. That is, adjust the 5700A using the knob to obtain the characterized reading on the rms meter (or dc DMM). Record the 5700A error display in each case and verify it is within the limits shown.

3-18. FREQUENCY RESPONSE TESTS (200, 20, AND 2 mV RANGES)

1. Connect the equipment as shown in Figure 3-10.

2. Set the 5700A for a 2V, 1 kHz output. Set the rms differential voltmeter dials to the previously characterized 200 mV, 1 kHz setting. Adjust the 5700A using the knob until the rms differential voltmeter reads precisely null. By using the NEW REF key, simultaneously obtain a 5700A error display reading equal to that recorded for 2V, 1 kHz of the Output Level Tests for AC Voltage Ranges 2V and Above.

3. Program frequencies of 40 Hz, 20 kHz, 50 kHz, 100 kHz, 300 kHz, and 1 MHz. At each frequency, use the knob to obtain in the 5700A ppm error display the reading previously recorded for the 2V range in the Output Level Tests for AC Voltage Ranges 2V and Above.

4. Record the rms differential voltmeter percentage error as shown on its null meter at each frequency up to 100 kHz. At the higher frequencies, set the differential dials for a null and record the dial settings. Return the 5700A to 1 kHz and the dials to the original 1 kHz setting to verify the rms differential voltmeter still indicates the original null within ± 0.003% (30 ppm). If not, redo the entire process until it does repeat adequately.

5. Set the 5700A for a 200 mV, 40 Hz output.

6. Remove the 20 dB rf attenuator and 50 ohm terminator from the test setup, and connect the rms differential voltmeter directly to the 5700A output.

7. Set the rms differential voltmeter dials for the characterized 200 mV, 1 kHz setting. Adjust the 5700A using the knob for the characterized rms differential voltmeter null meter reading recorded for 40 Hz. Record the 5700A error display reading and verify that it is within the limits shown on the test record.

8. Repeat step 7 at 20 kHz, 50 kHz, 100 kHz, 300 kHz, and 1 MHz and adjust the 5700A using the knob to obtain the characterized rms differential voltmeter null meter readings recorded in step 4 for each frequency. Record the 5700A error display and verify that it is within the limits shown on the test record.

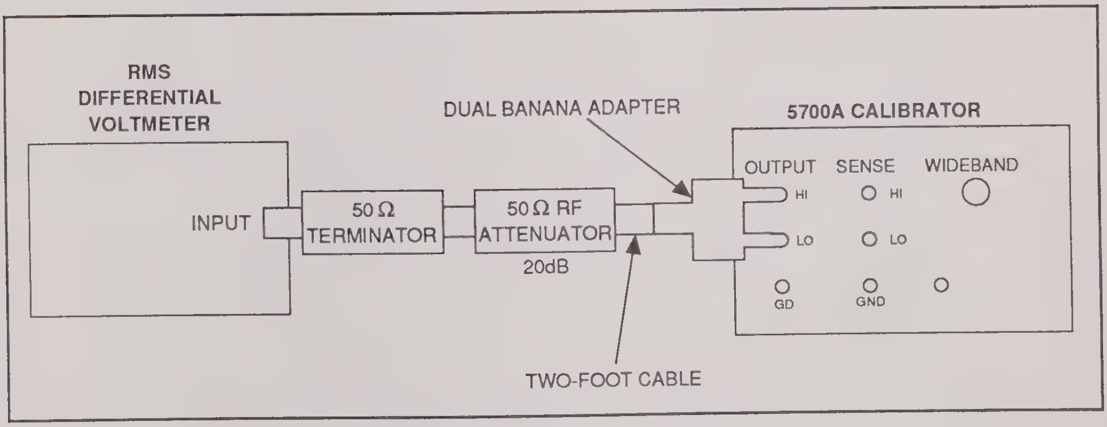

RMS
DIFFERENTIAL
VOLTMETER
INPUT
50 Ω
TERMINATOR
50 Ω RF
ATTENUATOR
20dB
DUAL BANANA ADAPTER
TWO-FOOT CABLE
5700A CALIBRATOR
OUTPUT
SENSE
WIDEBAND
HI
HI
LO
LO
GD
GND

Figure 3-10. Frequency Response Characterization

9. Reconnect the equipment of Figure 3-10 except use two 20 dB RF Attenuators in series to output approximately 20 mV. Repeat the process in steps 2 through 8 for 20 mV testing, substituting 20 mV wherever 200 mV appears in the text. However, the requirement for repeatability for this level is ±0.01% whenever returning to the 1 kHz reference.

3-19. 2 mV RANGE TEST

1. Set up the equipment connections shown in Figure 3-10. Use three 20 dB rf attenuators in series.
2. Set the 5700A for a 2.0V, 1 kHz output.
3. Adjust the 5700A using the knob to obtain the characterized 2 mV reading on the dc DMM attached to the rms wideband voltmeter output.
4. Press the 5700A NEW REF key to reference the output level.
5. As was done previously for the 200 mV and 20 mV levels, set the 5700A to the following frequencies: 40 Hz, 20 kHz, 50 kHz, 100 kHz, 300 kHz, and 1 MHz. At each frequency, record the dc DMM reading. (Due to the lower accuracy, it will not be necessary to edit in any 5700A 2V range corrections for this test). Then, as before, return to the 1 kHz reference to check for repeatability within ±0.03%. The 8922 filter must be switched in at all frequencies below 100 kHz.
6. Remove the rf attenuators from the setup and connect the characterized rms wideband voltmeter/dc DMM combination directly to the 5700A output.
7. Set the 5700A for a 2.0 mV, 40 Hz output. Adjust the 5700A using the knob to obtain a dc DMM reading equal to the previously characterized reading at 40 Hz recorded in step 5. Record the 5700A error display reading and verify that it is within the limits shown on the test record.
8. Repeat step 7 at 20 kHz, 50 kHz, 100 kHz, 300 kHz, 1 MHz. At each frequency adjust the 5700A error controls to obtain the characterized reading from step 5 on the dc DMM. Record the 5700A error display and verify that it is within the limits shown on the test record.
9. This completes the AC Voltage Calibration Verification Tests.

Table 3-11. AC Voltage Millivolt Ranges Test Summary

1 KHZ LEVEL VERIFICATION (200 MV, 20 MV, AND 2 MV RANGES)

UUT OUTPUT	RATIO TRANS. SETTING	931 200 mV READING	931 20 mV READING	8922/DMM 2 mV READING
2V @ 1 kHz	0.1		N/A	N/A
2V @ 1 kHz	0.01	N/A		N/A
2V @ 1 kHz	0.001	N/A	N/A	

UUT OUTPUT	UUT ERROR DISPLAY	LIMITS
200 mV @ 1 kHz		±150 ppm
20 mV @ 1 kHz		±410 ppm
2 mV @ 1 kHz		±0.261 ppm

FREQUENCY RESPONSE TESTING (200 MV, 20 MV, AND 2 MV RANGES)

CHARACTERIZING 200 mV LEVEL OF RMS DIFF. VOLTMETER:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Null
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to Null ±0.003%

200 mV OUTPUT ACCURACY:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±150 ppm
20 kHz		±150 ppm
50 kHz		±380 ppm
100 kHz		±0.115%
300 kHz		±0.19%
1 MHz		±0.38%

Table 3-11. AC Voltage Millivolt Ranges Test Summary (cont)

CHARACTERIZING 20 mV LEVEL OF RMS DIFF. VOLTMETER:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Null
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to Null ±0.01%

20 mV OUTPUT ACCURACY:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±410 ppm
20 kHz		±410 ppm
50 kHz		±670 ppm
100 kHz		±0.13%
300 kHz		±0.195%
1 MHz		±0.48%

CHARACTERIZING 2 mV LEVEL OF RMS DIFF. VOLTMETER:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Same as reading in 1 kHz Level Verification, ratio trans: 0.001
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to first entry reading ±0.03%

2 mV OUTPUT ACCURACY:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±0.261%
20 kHz		±0.261%
50 kHz		±0.287%
100 kHz		±0.49%
300 kHz		±0.87%
1 MHz		±1.83%

3-20. Direct Current Accuracy Verification Test

Equipment required for the Direct Current Accuracy Verification Test is listed in Table 3-12.

Table 3-12. Equipment Required for Direct Current Test

EQUIPMENT	MODEL OR DESCRIPTION	
DC DMM, 6-1/2 digit	Fluke 8500 Series	
High-Current Shunt	Fluke Y5020	(for 5725A)
Standard Resistor Shunts:	L&H 0.1 ohm at 2A 10 ohm at 200 mA 100 ohm at 20 mA 1 kilohm at 2 mA Fluke 742A-10k 10 kilohm at 200 uA	

1. Connect the dc DMM to the 5700A output and program the 5700A for outputs of 200 mV, 2V, and -2V, and record the dc DMM reading at each voltage.
2. Refer to the standard resistor test report and enter the corrections for all the certified values in ppm in column A on the test record.
3. Connect the equipment as shown in Figure 3-11 using the L&H 0.1 ohm resistor.

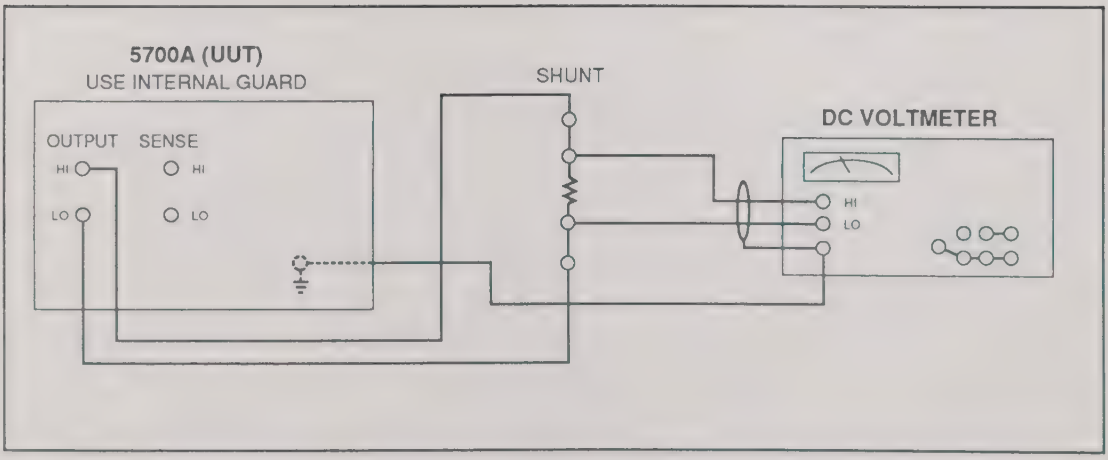

5700A (UUT)
USE INTERNAL GUARD
OUTPUT
SENSE
HI
LO
HI
LO
SHUNT
DC VOLTMETER
HI
LO

Figure 3-11. Direct Current Tests

4. Set the 5700A for a 2A dc output, and adjust the 5700A using the knob to obtain the characterized voltage reading on the dc DMM. Wait 3 seconds, and record the 5700A error display reading (Column B).

5. Subtract column B from column A. Enter the result (with polarity reversed) on the test record. Verify that it is within the limits shown on the test record.

6. Repeat steps 2 through 5 using the Fluke 742A Resistance Standards and 5700A output currents shown in Table 3-13.

Table 3-13. Direct Current Accuracy Verification

CHARACTERIZING DC DMM @ ±200 MV AND ± 2.0V

+200 mV RDG	-200 mV RDG	+2.0V RDG	-2.0V RDG

OUTPUT CURRENT	STD RES VALUE	STD RES CORRECTION	UUT ERROR READING	UUT ACTUAL ERROR (A-B) REVERSE POL	LIMIT OF ERROR
+2A	0.1 ohm				±100 ppm
-2A	0.1 ohm				±100 ppm
+200 mA	10 ohm				±65 ppm
-200 mA	10 ohm				±65 ppm
+20 mA	10 ohm				±55 ppm
+2 mA	1 kilohm				±55 ppm
-2 mA	1 kilohm				±55 ppm
+200 uA	10 kilohm				±100 ppm

5725A AMPLIFIER DC CURRENT TEST

OUTPUT CURRENT	DC DMM RDG	SHUNT CERT VALUE	CAL ACTUAL CURRENT	LIMITS
-10A				±428 ppm
5A				±428 ppm
2A				±428 ppm
-2A				±428 ppm

7. If the 5700A is attached to a 5725A Amplifier, connect the Y5020 shunt to the 5700A output terminals. Connect the dc DMM to the Y5020 sense connector.

8. Set the 5700A to 10A, 5A, 2A and -2A and record the dc DMM readings on the Test Record. Divide these readings by the certified value of the Y5020, record the resultant current and verify that it is within the tolerances shown.

9. This completes the direct current accuracy verification.

3-21. Alternating Current Tests

Equipment required for the Alternating Current Accuracy Verification Test is listed in Table 3-14.

Table 3-14. Equipment Required for Alternating Current Test

EQUIPMENT	MODEL OR DESCRIPTION
Thermal Transfer Standard	Fluke 540B
Current Shunts	Fluke A40 Series
DMM	Fluke 850X
T9 Metal Film resistors	1k ohm, 10k ohm, and 1M ohm value

1. Connect the equipment as shown in Figure 3-12. Use the 2A Current shunt.

2. Set the 5700A for a +2A dc output. Adjust the output so that the error display is equal to the UUT actual error for a +2A output, as shown on the dc current test record.

3. Allow sufficient time (usually around 10 minutes for the first reading) for the transfer standard null meter reading to stabilize. Adjust the transfer standard null controls for a precise null indication.

4. Proceed as follows to obtain an average of the reversed dc to obtain a reference for the ac:

    a. Adjust the transfer standard null controls for a null with a positive polarity current from the 5700A.

    b. Reverse the current polarity into the transfer standard by pushing the POLARITY (push to reverse) button on the transfer standard.

    c. Record the final deflection on the transfer standard null meter in + or - small divisions.

    d. Push the POLARITY button on the transfer standard again for positive polarity. Verify that the null meter returns to a precise null.

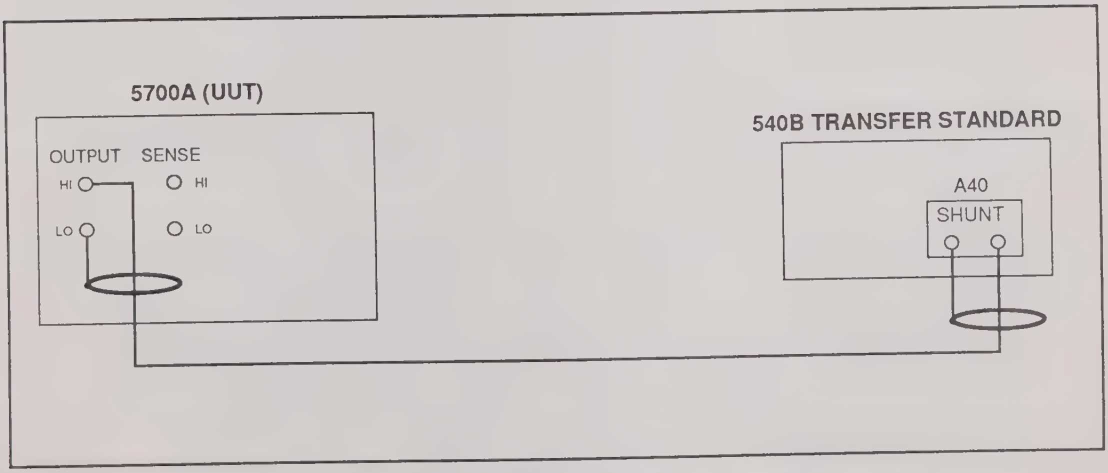

5700A (UUT)
OUTPUT
SENSE
HI
HI
LO
LO
540B TRANSFER STANDARD
A40
SHUNT

Figure 3-12. Alternating Current Accuracy Verification Test

   e. Adjust the transfer standard controls to obtain one-half the deflection recorded in step c, but in the opposite direction. For example, if you recorded +4.7 divisions for step c, the correct offset for step e would be -2.4 divisions (rounded to the nearest tenth).

5. Set the 5700A to 2A at 40 Hz OPERATE.

6. Without touching the transfer standard null controls, use the 5700A edit knob to adjust the 5700A output as necessary to obtain a null on the Transfer Standard null meter. Reverse the polarity of the error display reading, and enter the result on the test record. Verify that it is within the limits shown on the test record.

7. Set the 5700A to 2A dc. Verify that the Transfer Standard null meter returns to the setting in step 4e. If necessary, repeat steps 2 through 6 until the required result is obtained.

8. Change the 5700A frequency to 1 kHz, 5 kHz, and 10 kHz. At each frequency, edit the 5700A for a null on the Transfer Standard null meter. Reverse the polarity of the error display reading, enter and verify the results as done in step 6 above.

9. Repeat steps 2 through 8 at currents of 200 mA and 20 mA using the appropriate A40 current shunt at the frequencies shown on the test record (Table 3-15).

10. For units with a 5725A Amplifier attached, repeat steps 2 through 8 at 11A using the 10A current shunt at the frequencies listed on the test record.

11. Now disconnect the 540B, and set the 5700A to 2V dc, operate. Connect the DMM to the output and record the DMM 2V dc reading on the test record.

12. Set the 5700A to 2V at frequencies of 10 Hz, 20 Hz, 40 Hz, 1 kHz, 5 kHz, and 10 kHz. At each frequency, record the DMM reading on the test record in the "DMM 2V ac READING" column.

13. Calculate the DMM ac-dc error by subtracting the 2V dc reading from each DMM 2V ac reading. Record the result on the test record in the "DMM AC-DC ERROR" column.

14. Connect the 1k ohm metal film shunt resistor across the 5700A output, and set the 5700A for a 2 mA dc operate. Adjust the output so the error display shows the same error as previously recorded at 2 mA dc. Since the DMM exhibits input impedance differences for ac and dc operation, you must connect a 1M ohm metal film resistor across the DMM input at this time to match the input impedance during an ac voltage measurement. Record the DMM reading as the "DMM 2 mA dc Reading" on the test record.

15. Algebraically add the "DMM 2 mA dc READING" to each previously calculated "DMM AC-DC ERROR", and record the results on the test record in the "EXPECTED DMM 2 mA ac READING" column.

16. Remove the 1M ohm resistor from the DMM input. Set the DMM for ac voltage operation. Set the 5700A to 2 mA ac at each frequency. Adjust the 5700A output at each frequency so that the DMM reading matches the the value in the "EXPECTED DMM 2 mA READING" column. Reverse the polarity of the error display and record this reading on the test record as the "ACTUAL 2mA ERROR". Verify that each reading is within tolerance.

17. Repeat steps 14 through 16, substituting 200 uA for 2 mA and using the 10k ohm metal film shunt resistor instead of the 1k ohm. Calculate the "EXPECTED DMM 200 uA READING" by algebraically adding the "DMM 200 uA dc READING" to each previously calculated "DMM AC-DC ERROR".

Table 3-15. Alternating Current Accuracy Verification

OUTPUT CURRENT	FREQ	ACTUAL UUT ERROR	ERROR LIMITS
2A	40 Hz		±675 ppm
2A	1 kHz		±675 ppm
2A	5 kHz		±800 ppm
2A	10 kHz		±0.91%
200 mA	10 Hz		±725 ppm
200 mA	20 Hz		±400 ppm
200 mA	40 Hz		±350 ppm
200 mA	1 kHz		±350 ppm
200 mA	5 kHz		±0.1%
200 mA	10 kHz		±0.49%
20 mA	10 Hz		±725 ppm
20 mA	20 Hz		±400 ppm
20 mA	40 Hz		±160 ppm
20 mA	1 kHz		±160 ppm
20 mA	5 kHz		±0.125%
20 mA	10 kHz		±0.54%

Table 3-15. Alternating Current Accuracy Verification (cont)

5725A AMPLIFIER TESTS

11A	40 Hz	±415 ppm
11A	1 kHz	±415 ppm
11A	5 kHz	±535 ppm
11A	10 kHz	±0.3368%

DMM 2V dc READING =

	DMM 2V ac READING	DMM AC-DC ERROR
10 Hz =		
20 Hz =		
40 Hz =		
1 kHz =		
5 kHz =		
10 kHz =		

DMM 2 mA dc READING = * Add 1 megohm to DMM Input

	EXPECTED 2 mA ac READING	ACTUAL 2 mA ERROR	ERROR LIMITS
10 Hz =			±725 ppm
20 Hz =			±400 ppm
40 Hz =			±160 ppm
1 kHz =			±160 ppm
5 kHz =			±0.175%
10 kHz =			±0.64%

DMM 200 uA dc READING = * Add 1 megohm to DMM Input

	EXPECTED 200 uA ac READING	ACTUAL 200 uA ERROR	ERROR LIMITS
10 Hz =			±850 ppm
20 Hz =			±505 ppm
40 Hz =			±240 ppm
1 kHz =			±240 ppm
5 kHz =			±0.575%
10 kHz =			±2.44%

3-22. Wideband AC Voltage Module Output Verification

The verification test for the Wideband module works as follows:

- Accuracy at 1 kHz: Output at 1 kHz is tested using a characterized rf voltmeter reading the output across a precision dc 50 ohm termination.
- Flatness relative to 1 kHz: First the 3V range is tested using the following process:
    1. Characterizing a 50 ohm detector using a 3V Thermal Voltage Converter (TVC).
    2. Using the characterized 50 ohm detector to read the 5700A 3V output flatness and recording the 5700A error display to get corrections for the next test. The absolute accuracy at frequencies between 30 Hz and 500 kHz will also be verified by inspection of the data.
- Attenuator Flatness: The attenuator flatness is tested using the following process:
    1. The 3V range corrections are used via 5700A error display to serve as a reference for characterizing the Attenuator Test Setup at a reduced number of frequencies.
    2. Each attenuator section is tested using a "put and take" method involving removal of 10 dB of external standard attenuation to correspond to each added 10 dB section of the 5700A.

3-23. WIDEBAND FLATNESS CALIBRATION PROCEDURE

Table 3-16. Test Equipment Required for the Wideband Option

MFG. AND MODEL	EQUIPMENT
Fluke A55-3V	High Freq. Thermal Converter
Narda 777C-20	20 dB RF Attenuator (Qty. 3)
Narda 777C-10	10 dB RF Attenuator (Qty. 1)
Comlinear CLC100	20 dB Amplifier (Qty. 2)
Fluke 8920A	Wideband RMS Voltmeter
(Any)	±12V Power Supply

1. Connect the equipment as shown in Figure 3-13.

2. Set the 5700A for 3V, 1 kHz operate. Select WIDEBAND Type "N" connector output by pressing the W BND key.

3. Adjust the 5700A output so the DMM connected to the RMS Wideband Voltmeter dc voltage output read exactly 1V. Press "NEW REF".

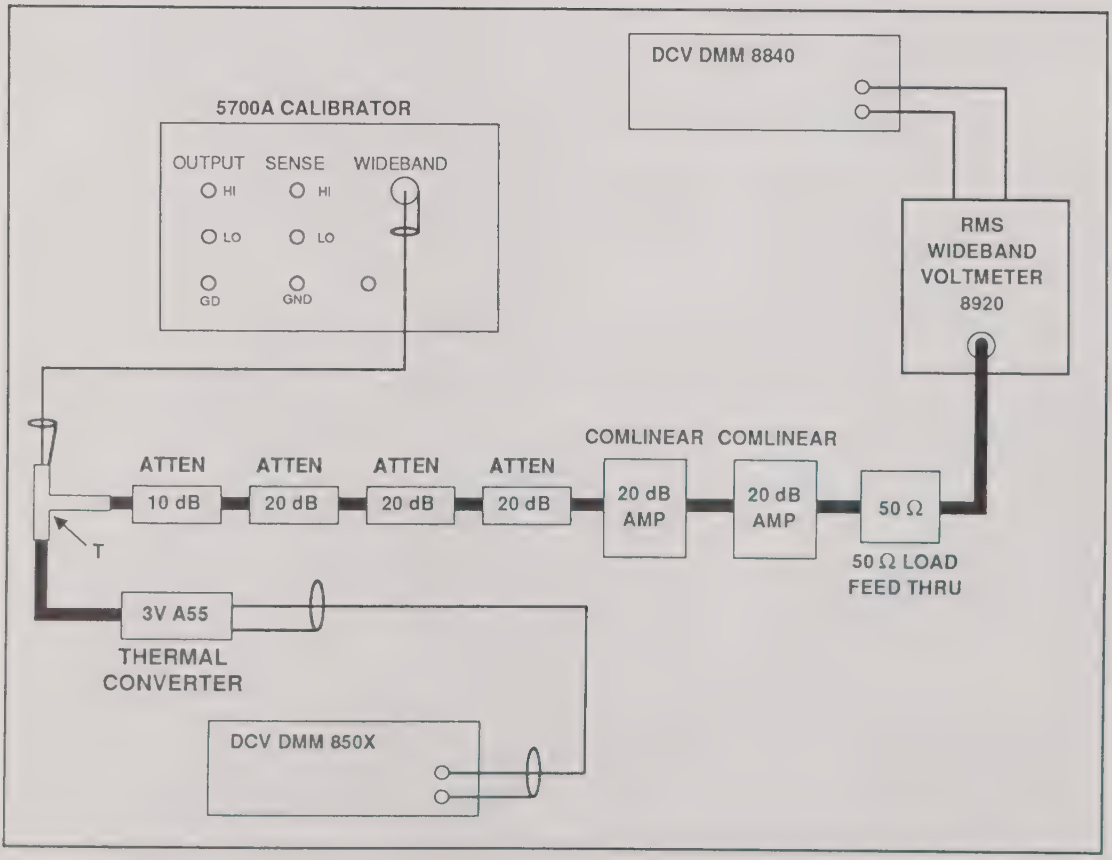

DCV DMM 8840
5700A CALIBRATOR
OUTPUT
SENSE
WIDEBAND
HI
HI
LO
LO
GD
GND
RMS
WIDEBAND
VOLTMETER
8920
COMLINEAR
COMLINEAR
ATTEN
ATTEN
ATTEN
ATTEN
10 dB
20 dB
20 dB
20 dB
20 dB
AMP
20 dB
AMP
50 Ω
50 Ω LOAD
FEED THRU
T
3V A55
THERMAL
CONVERTER
DCV DMM 850X

Figure 3-13. Wideband Flatness Calibration

4. Zero the 850X DMM that is connected to the A55 Thermal Sensor output.

5. At each frequency mentioned below, first adjust the 5700A output until the 850X DMM connected to the A55 Thermal Sensor reads 0 volts, then record the reading of the DMM connected to the RMS Wideband Voltmeter.

   Frequency: 12 kHz, 100 kHz, 500 kHz, 1.1999 MHz, 1.2 MHz,
   DMM Reading: _______/_______/_________/_________/_________

   Frequency: 2 MHz, 10 MHz, 20 MHz, 30 MHz.
   DMM Reading: _______/______/_______/_______

6. Remove the A55 Thermal Sensor and the 850X DMM from the setup.

7. Call up the 5700A Wideband Flatness Calibration routine on the 5700A front panel by pressing the softkey sequence "Setup Menus", "Cal", "Calibration", "Wideband Flat".

8. Enter the present ambient air temperature as prompted, and press ENTER.

9. Wideband Flatness Calibration starts with a 3V output at 1 kHz. Using the 5700A edit knob, adjust the output until the DMM connected to the RMS Wideband Voltmeter output reads exactly 1V; then press ENTER.

10. The Wideband output frequency changes to 12 kHz. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 12 kHz in step 5. Press ENTER.

    Repeat this step for each frequency through 30 MHz, adjusting the output each time to match the value recorded in step 5.

11. The 5700A Wideband output changes to 1V at 1 kHz. Remove the 10 dB attenuator from the test setup, leaving a total attenuation of 60 dB. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 1 kHz in step 5. Press ENTER.

    Repeat this step for each frequency through 30 MHz, adjusting the output each time to match the value recorded in step 5.

12. The 5700A Wideband output changes to 300 mV at 1 kHz. Remove a 20 dB attenuator, and replace the 10 dB attenuator on the test set up for a total attenuation of 50 dB. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 1 kHz in step 5. Press ENTER.

    Repeat this step for each frequency through 30 MHz, adjusting the output each time to match the value recorded in step 5.

13. The 5700A Wideband output changes to 100 mV at 1 kHz. Remove the 10 dB attenuator on the test setup for a total attenuation of 40 dB. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 1 kHz in step 5. Press ENTER.

    Repeat this step for each frequency, adjusting the output each time to match the value recorded in step 5. This time, only 1 kHz, 10 MHz, 20 MHz, and 30 MHz points are adjusted.

14. The 5700A Wideband output changes to 30 mV at 1 kHz. Remove another 20 dB attenuator from the test setup for a total attenuation of 30 dB. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 1 kHz in step 5.

    Repeat this step for each frequency through 30 MHz, adjusting the output each time to match the value recorded in step 5.

15. The 5700A Wideband output changes to 10 mV at 1 kHz. Remove the 10 dB attenuator from the test setup for a total attenuation of 20 dB. Use the 5700A output adjust knob to adjust the output until the DMM reads the voltage that was recorded for 1 kHz in step 5.

    Repeat this step for each frequency, adjusting the output each time to match the value recorded in step 5. This time, only 1 kHz, 10 MHz, 20 MHz, and 30 MHz points are adjusted.

16. Make sure the CALIBRATION switch is in the ENABLE position, and store the values by pressing a softkey to conclude the Wideband Flatness Calibration procedure.

3-24. WIDEBAND FREQUENCY ACCURACY TEST

Proceed as follows to test the Wideband module frequency accuracy:

1. Connect the frequency counter to the 5700A wideband output and measure the 5700A output frequency at the frequencies listed in Table 3-18. Verify that the frequency counter indicates within the 0.01% limits shown.

Table 3-18. Frequency Testing Points

FREQUENCY (HZ)	TOLERANCE LIMITS
10 Hz	99.99 ms to 100.01 ms
100 Hz	9.999 ms to 10.001 ms
300 Hz	299.97 Hz to 300.03 Hz
500 Hz	499.95 Hz to 500.05 Hz
800 Hz	799.92 Hz to 800.08 Hz
900 Hz	899.91 Hz to 900.09 Hz
1 kHz	999.0 Hz to 1.0001 kHz
1.19 kHz	1.189881 kHz to 1.190119 kHz
2.2 MHz	2.19978 MHz to 2.20022 MHz
3.5 MHz	3.49965 MHz to 3.50035 MHz
3.8 MHz	3.79962 MHz to 3.80038 MHz
10 MHz	9.990 MHz to 10.001 MHz
20 MHz	19.998 MHz to 20.002 MHz
30 MHz	29.997 MHz to 30.003 MHz

3-25. WIDEBAND OUTPUT ACCURACY AT 1 kHz TEST

Proceed as follows to perform rms wideband voltmeter characterization at 1 kHz:

1. Connect the equipment as shown in Figure 3-14. Use the wideband output cable provided for the connection from the main 5700A output to the 8920A.

NOTE

> At output levels below 200 mV, the capacitor works against the 5700A main output 50 ohm divider to form a 200 kHz low-pass filter, which eliminates noise-induced floor errors.

2. Set the 5700A main output to the voltage levels at 1 kHz listed on the test record. At each level record the rms wideband voltmeter reading.

3-26. WIDEBAND ACCURACY AT 1 kHz

3. Connect the equipment as shown in Figure 3-15. Use the same 50 ohm terminator as used during the wideband gain calibration.

4. Set the 5700A to the voltages shown on the test record and adjust the 5700A using the knob to obtain the characterized reading on the rms differential voltmeter from the previous test. Using Table 3-18, record and verify that the error reading is within limits.

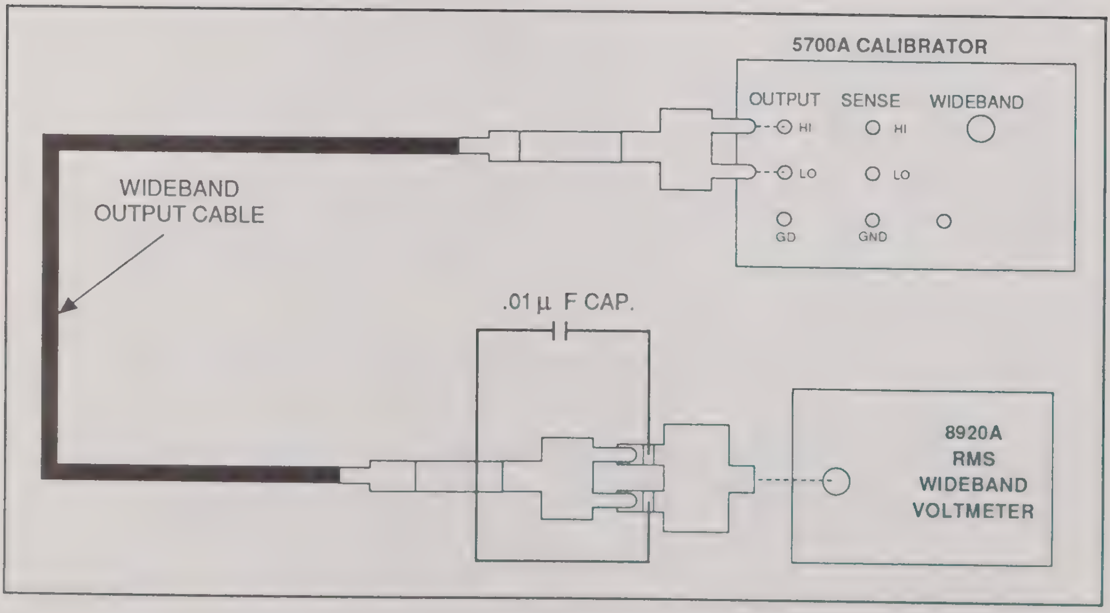

5700A CALIBRATOR
OUTPUT
SENSE
WIDEBAND
HI
HI
LO
LO
GD
GND
WIDEBAND OUTPUT CABLE
.01 µ F CAP.
8920A RMS WIDEBAND VOLTMETER

Figure 3-14. RF Voltmeter Characterization at 1 kHz

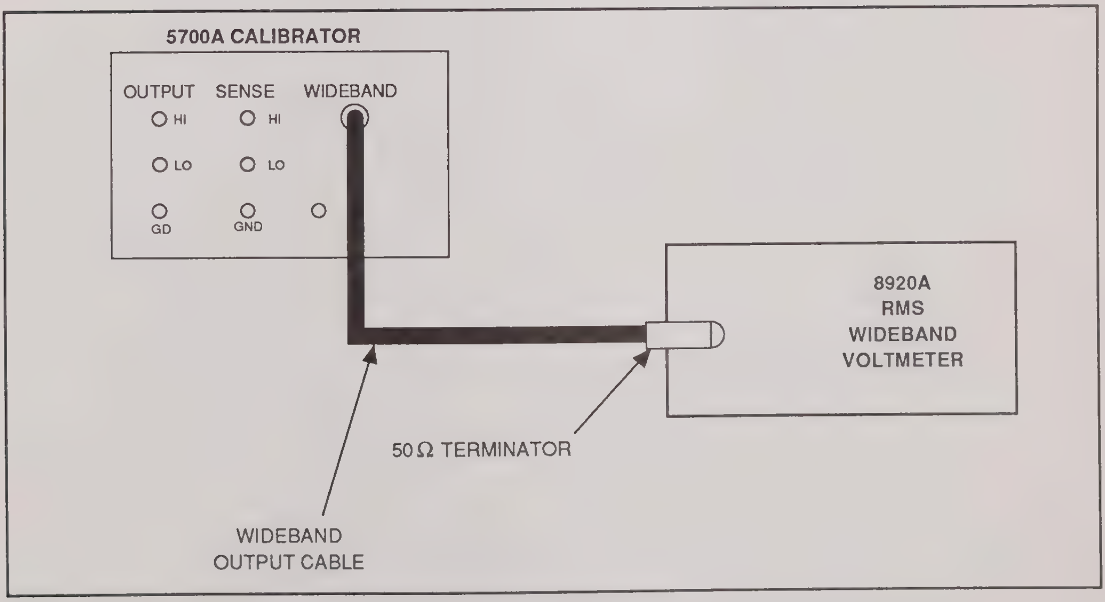

5700A CALIBRATOR
OUTPUT
SENSE
WIDEBAND
HI
HI
LO
LO
GD
GND
8920A
RMS
WIDEBAND
VOLTMETER
50 Ω TERMINATOR
WIDEBAND
OUTPUT CABLE

Figure 3-15. Wideband Accuracy Tests

Table 3-18. Wideband Accuracy at 1 kHz

OUTPUT LEVEL	8920A READING OF 5700A MAIN OUTPUT	WIDEBAND OUTPUT ERROR DISPLAY READING	LIMITS
3.0V			±.2167%
1.0V			±.2900%
0.3V			±.2833%
0.1V			±.3400%
30 mV			±.3333%
10 mV			±.3900%
3 mV			±.3833%
1 mV			±.4400%

3-27. WIDEBAND OUTPUT FLATNESS TEST

NOTE

The following test uses a non-50 ohm thermal voltage converter (TVC) to characterize a 50 ohm detector. For the 5700A output flatness test to be valid, the 5700A must be connected to a good rf 50 ohm device. It is not satisfactory to just parallel the input of the TVC with a good rf 50 ohm (especially at frequencies above 10 MHz). However, the TVC will indicate the actual voltage at the midpoint of a GR TEE connector when paralleled with 50 ohms. Therefore, it is valid to calibrate the 50 ohm detector with the TVC on the other end of the GR TEE.

3-28. 50 Ohm Detector Characterization

First you must perform 50 Ohm Detector Characterization. To do so, proceed as follows:

NOTE

Before beginning this test, obtain a copy of your 3V TVC test report. Apply any corrections that exceed the following:

- 0.01% to 20 MHz
- 0.02% to 10 MHz
- 0.04% to 20 MHz
- 0.1% to 30 MHz

At this time, note any corrections that exceed these levels for future reference.

1. Connect the equipment as shown in Figure 3-16.

2. Set the 5700A for a wideband output of 2.7V at 1 kHz.

3. Adjust the 5700A using the knob to obtain a convenient reference reading (such as 0.90000V) on the dc DMM connected to the RMS Wideband Voltmeter analog output. (Note: do not use log output if the meter is so equipped).

4. Allow sufficient time for the TVC to stabilize. Five to ten minutes is sufficient unless the TVC body has not reached ambient temperature before voltage is applied. Zero the 850X DMM connected to the A55 Thermal Sensor output.

5. Readjust the 5700A knob to obtain the 0.90000V reference reading of the rms wideband voltmeter dc DMM. Zero the 850X DMM again. Press the 5700A NEW REF button.

NOTE

Do not touch the 850X DMM connected to the A55 output until you are told to do so or you begin the test process at 1 kHz again.

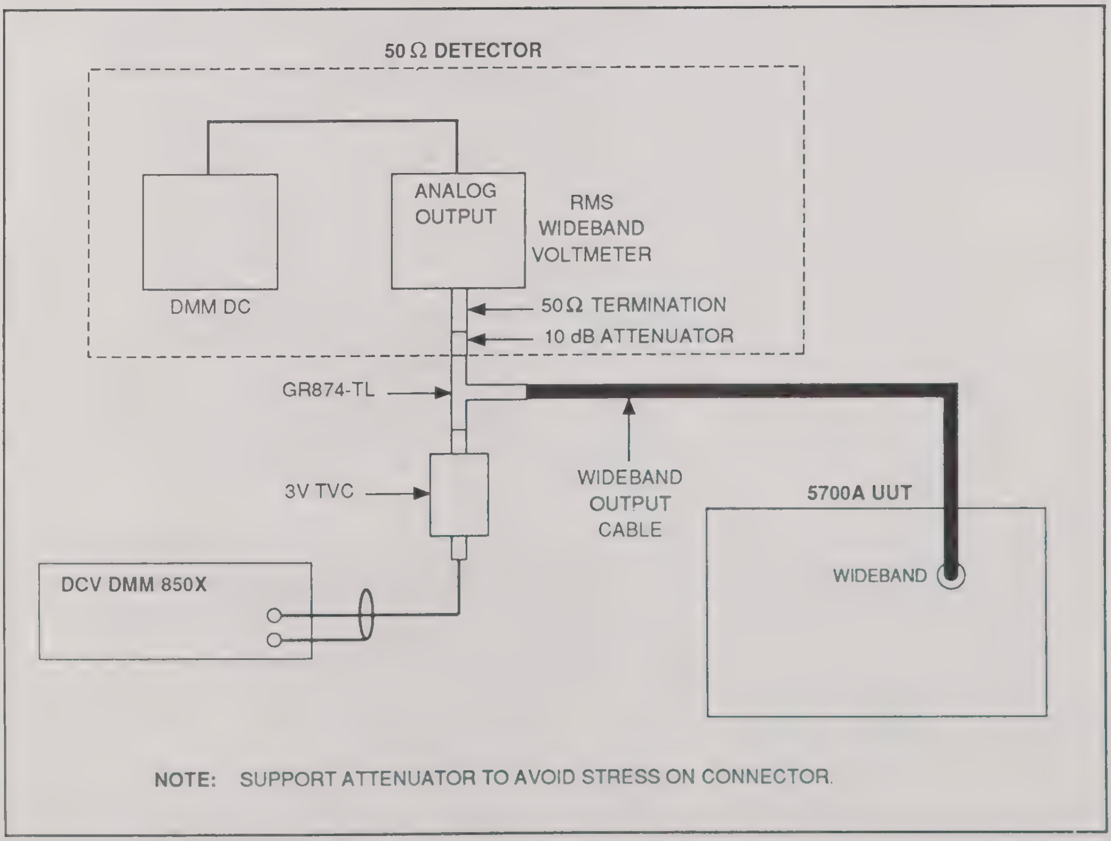
6. Program the frequencies shown on the test record (Table 3-19). For each frequency, adjust the 5700A using the knob to obtain a zero on the 850X DMM that is connected to the A55 output. Then record the rms wideband voltmeter dc DMM reading on the test record (Table 3-19) in the "50 Ohm Detector Characterization RMS Wideband DC DMM RDG" column.

NOTE

If any TVC corrections exceed the criteria stated in the step 1 note, use them by offsetting the 850X DMM by the opposite sign of the reported value. For example, if the reported rf/dc difference is +.05%, the UUT output (the one that has been nulled on the 850X DMM connected to the A55) must be edited down 0.05% before the rms wideband dc DMM reading can be recorded.

7. The last frequency point is to return to 1 kHz. Adjust the 5700A using the knob for a rms wideband voltmeter dc DMM reading of 0.90000V and verify that the transfer standard reading returns to null within ±0.02%. If it does not, repeat the process beginning at step 2 until this tolerance is met.

8. Set the 5700A to standby.


50 Ω DETECTOR
ANALOG OUTPUT
RMS WIDEBAND VOLTMETER
DMM DC
50 Ω TERMINATION
10 dB ATTENUATOR
GR874-TL
3V TVC
WIDEBAND OUTPUT CABLE
5700A UUT
WIDEBAND
DCV DMM 850X

NOTE: SUPPORT ATTENUATOR TO AVOID STRESS ON CONNECTOR.

Figure 3-16. 50 Ohm Detector Characterization

3-29. 3V Range Wideband Flatness Test

1. Connect the equipment as shown in Figure 3-17.
2. Program the 5700A for a wideband output of 2.7V at 1 kHz. Adjust the 5700A using the knob until the rms wideband voltmeter dc DMM reads the same reference reading (previous example was 0.90000V) used in the characterization test. Press NEW REF to reference the 5700A error display to zero.
3. Set the 5700A to the frequencies listed on the test record. At each frequency, adjust the 5700A output level using the knob to obtain the characterized rms wideband voltmeter dc DMM reading. Record the 5700A error display for that frequency in the "3V Range Wideband Flatness Test Error Display Rdg" column. Verify that the error readings are within the limits shown on the test record. The last frequency is the 1 kHz reference. If the readings do not repeat within 0.02% it will be necessary to repeat the test process until acceptability is attained.
4. Set the 5700A to standby and disconnect the equipment from the 5700A.

3-30. Setup for Attenuator Flatness Test

1. Connect the equipment as shown in Figure 3-18.
2. Program the 5700A for a 3V wideband output at 1 kHz.
3. The rms wideband voltmeter should be reading around 100 mV if the amplifier gains are nominal. Adjust the 5700A using the knob to obtain a 0.90000V indication on the rms wideband voltmeter dc DMM and then press NEW REF to reference the output.
4. Program each output frequency shown on the test record. Record the wideband voltmeter dc DMM reading for each frequency. As before, the return reading at 1 kHz must repeat within ±0.02%.

3-40. Attenuator Flatness Test

1. In the next column enter the 3V range error display readings from the "Output Flatness Test" record (for the appropriate frequency) on the test record.
2. With the equipment still connected as in Figure 3-18, remove the 10 dB attenuator and program the 5700A for a wideband output of 1V, 1 kHz.
3. Adjust the 5700A using the knob to obtain the rms wideband voltmeter dc DMM reference level of 0.90000V. Press NEW REF to re-reference the error display to zero.

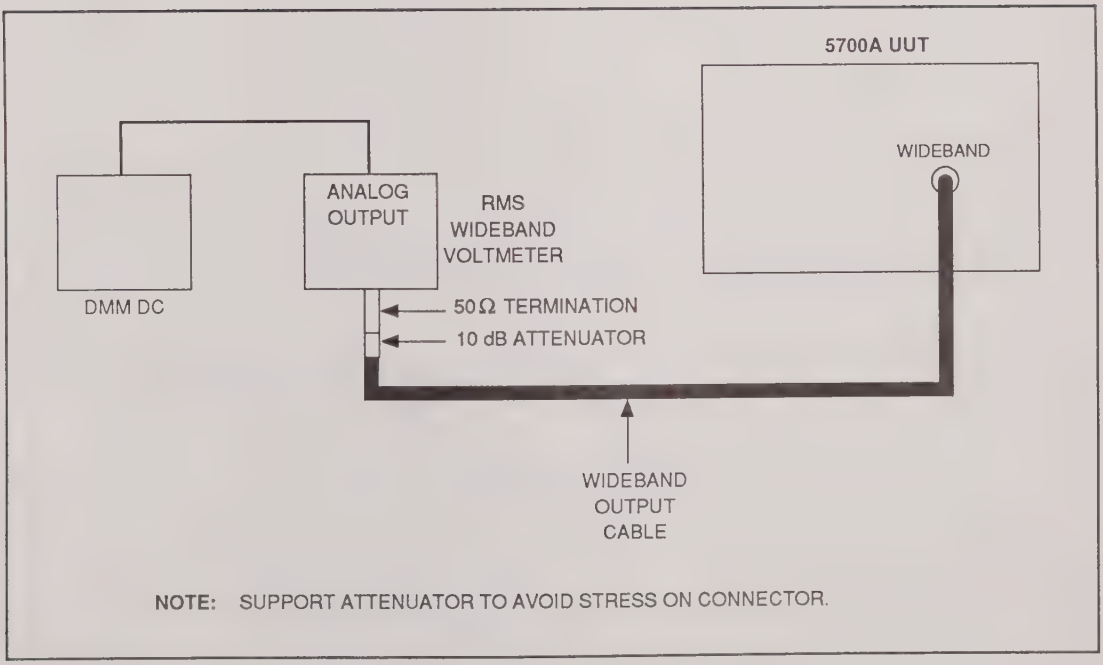
Table 3-19. Output Flatness Test and Attenuator Flatness Tests

Table 3-19. Output Flatness and Attenuator Flatness Tests

FREQUENCY	50 OHM DETECTOR CHARACTERIZATION RMS WIDEBAND DC DMM READING	3V RANGE WIDEBAND FLATNESS TEST ERROR DISPLAY READING	LIMITS
1 kHz	.90000V	---	---
10 Hz			0.3%
30 Hz			0.1%
120 kHz			0.1%
500 kHz			0.1%
2 MHz			0.1%
5 MHz			0.2%
10 MHz			0.4%
20 MHz			0.4%
30 MHz			1.0%

ATTENUATOR FLATNESS TEST RECORD

FREQ	WIDEBAND DC DMM CHAR DATA	3V RANGE WIDEBAND FLAT TEST ERR DISPL	(60 dB) 1.0V OUTPUT	(50 dB) 300 mV OUTPUT	(40 dB) 100 mV OUTPUT	(30 dB) 30 mV OUTPUT	(20 dB) 10 mV OUTPUT	>3 mV LIMIT	(10 dB) 3 mV OUTPUT	3 mV LIMIT	(0 dB) 1 mV OUTPUT	1 mV LIMIT
1 kHz	.90000V	- 0 -	.90000V	.90000V	.90000V	.90000V	.90000V		.90000V		.90000V	
2 MHz								.1%		.1%		.5%
10 MHz								.4%		.5%		.5%
20 MHz								.4%		.5%		.5%
30 MHz								1%		1.5%		3.0%
1 kHz	<.02%		<.02%	<.02%	<.02%	<.02%	<.02%		<.02%		<.02%	


5700A UUT
WIDEBAND
ANALOG OUTPUT
RMS WIDEBAND VOLTMETER
DMM DC
50 Ω TERMINATION
10 dB ATTENUATOR
WIDEBAND OUTPUT CABLE

NOTE: SUPPORT ATTENUATOR TO AVOID STRESS ON CONNECTOR.

Figure 3-17. 3V Output Flatness Test

4. Set the 5700A to the frequencies listed on the test record. For each frequency, turn the 5700A knob to obtain the rms wideband voltmeter dc DMM reference reading entered on the test record. Record the error display readings and verify that, after being algebraically added to the 3V range error readings in the second column, they are within the limits shown on the test record.

5. Repeat the preceding process for the remaining ranges by decreasing the range by 10 dB and the total external attenuation by 10 dB for each range. Note that for the next range (0.3V) you will have to remove a 20 dB section and replace the 10 dB section to achieve a 10 dB shift. The total external attenuation is shown in parentheses near each range value.

6. Set the 5700A to standby and disconnect the equipment. This completes wideband verification.

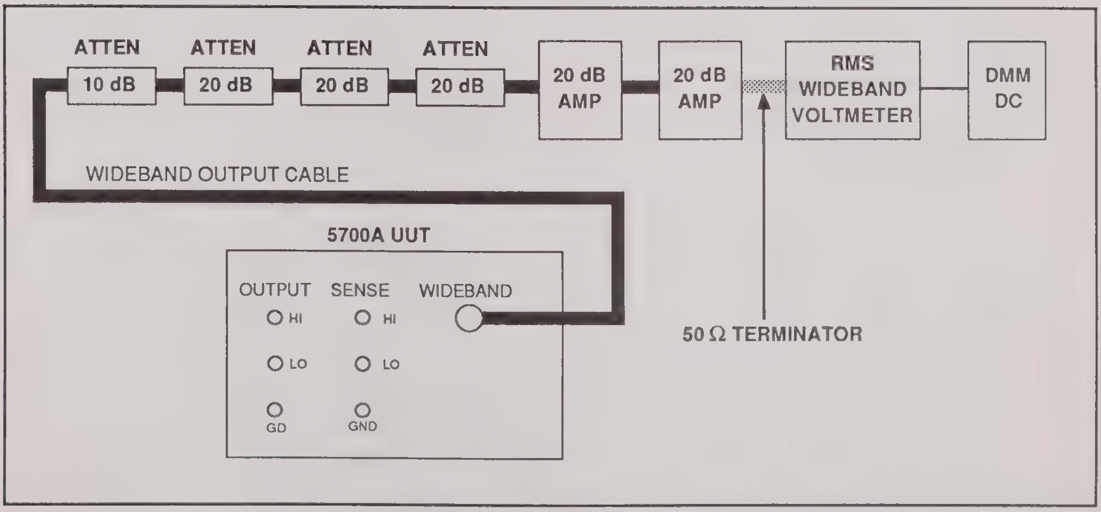

ATTEN
10 dB
ATTEN
20 dB
ATTEN
20 dB
ATTEN
20 dB
20 dB AMP
20 dB AMP
RMS WIDEBAND VOLTMETER
DMM DC
WIDEBAND OUTPUT CABLE
5700A UUT
OUTPUT
HI
LO
GD
SENSE
HI
LO
GND
WIDEBAND
50 Ω TERMINATOR

Figure 3-18. Attenuator Flatness Test Setup

3-41. OPTIONAL TESTS

These tests are recommended for use in acceptance testing or following repair likely to affect their characteristics. They are not recommended to be done routinely. If the 5700A passes Calibration Performance Verification, you do not need to perform these tests; verification either exercises these functions or is subject to their effects. The Optional Tests include such checks as load regulation, noise, and distortion.

Required equipment is listed in Table 3-20.

Table 3-20. Equipment Required For DC V Optional Tests

RMS Differential Voltmeter	Fluke 931B
Power Decade Resistor	Clarostat 240C
Differential Amplifier Plug-In	Tektronix 7A22
Oscilloscope Mainframe	Tektronix 7000-series
DC Voltage Reference Standard	Fluke 732A
Reference Divider	752A
Null Detector	845A(B or R)
Kelvin-Varley Divider	720A

3-42. DC Voltage Load Regulation Test

1. Ensure the 5700A is in standby. With the test setup of Figure 3-6, connect the power decade resistor across the 5700A OUTPUT terminals. Connect two shorting links between the 5700A SENSE and OUTPUT terminals and select external sense (EX SNS indicator lit).

2. Set the reference divider to 10V. Set the 5700A output to 10V dc. Set the power decade resistor to 199 ohms. Set the 5700A to operate. Adjust the 5700A as necessary to obtain a null on the null detector. Rotate the most significant dial on the power decade resistor to 9. Verify that the null detector indication changes less than ± 2 uV. Set 5700A to standby.

3. Repeat load regulation testing at the remaining 5700A outputs shown in Table 3-21.

Table 3-21. Load Regulation Test Summary

DIV. SETTING	5700A RANGE	5700A OUT/FULL LOAD	CHANGE IN NULL
10V	11V	10V/199 ohms	±2 uV
100V	220V	100V/1999 ohms	±2 uV
1000V	1100V	1000V/39.99 kilohms	±2 uV

4. Set the 5700A to RESET and disconnect all equipment from the 5700A.

3-43. DC Voltage Linearity Test

1. Self calibrate the Kelvin-Varley (KV) divider as called for in its service manual.
2. Connect the equipment as shown in Figure 3-19.
3. Set the KV dials to zero by using the RANGE LOCK. Set the 5700A to 0V on the 11V range operate. Note the Null Detector reading. Press OFFSET on the 5700A.
4. Set KV dials to 0.999999X and 5700A for a 10V output.
5. Adjust the 5700A output using the knob for a Null Detector reading equal to the reading noted in step 3. Press SCALE on the 5700A.
6. For each of the KV settings tabulated in Table 3-22, make the required Kelvin Varley setting, and verify that the null detector reads within the limits shown.

Table 3-22. Linearity Test Summary

KELVIN-VARLEY SETTING	5700A OUTPUT	NULL DETECTOR READING
0.1	1V	±2.3 uV
0.2	2V	±2.6 uV
0.3	3V	±2.9 uV
0.4	4V	±3.2 uV
0.5	5V	±3.5 uV
0.6	6V	±3.8 uV
0.7	7V	±4.1 uV
0.8	8V	±4.4 uV
0.9	9V	±4.7 uV

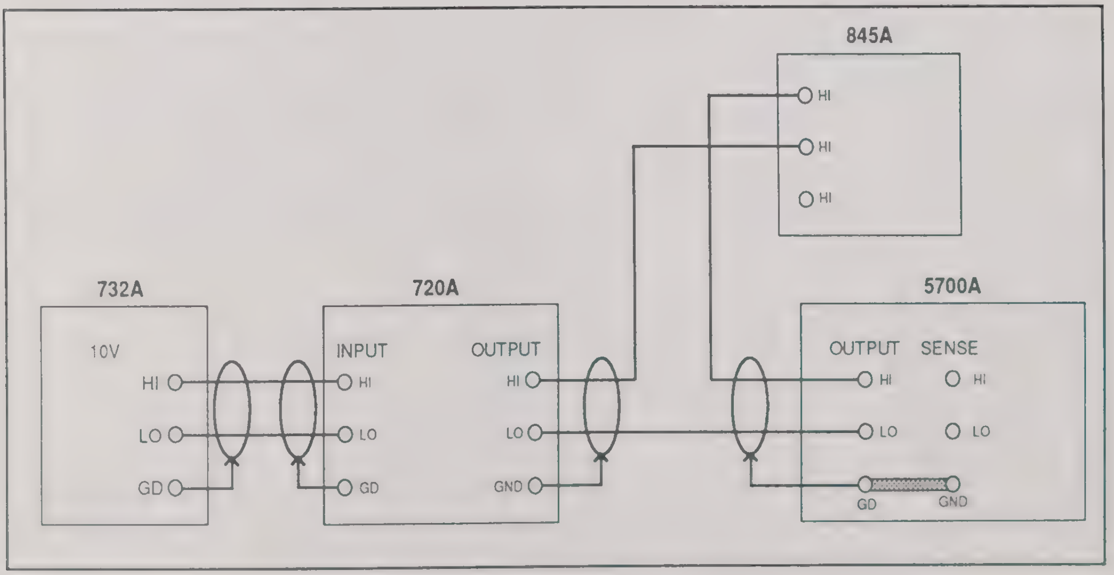

845A
HI
HI
HI
732A
10V
HI
LO
GD
720A
INPUT
HI
LO
GD
OUTPUT
HI
LO
GND
5700A
OUTPUT
SENSE
HI
LO
HI
LO
GD
GND

Figure 3-19. DC Voltage Linearity Test

3-44. DC Voltage Output Noise Test (10 Hz to 10 kHz)

1. Connect the equipment as shown in Figure 3-20.

2. Set the Oscilloscope Differential Amplifier controls as shown below.

Low Frequency -3 dB	10 Hz
High Frequency -3 dB	10 kHz
Input Coupling	AC (both inputs)
Volts/Div	50 uV (Var. to Cal.)

3. Set the Oscilloscope Time/Div for 2 ms.

4. Set the rms voltmeter range to 1V.

5. Set the 5700A to 2.2V dc and press OPR/STBY. Verify that the reading on the rms voltmeter is less than 150 mV.

NOTE

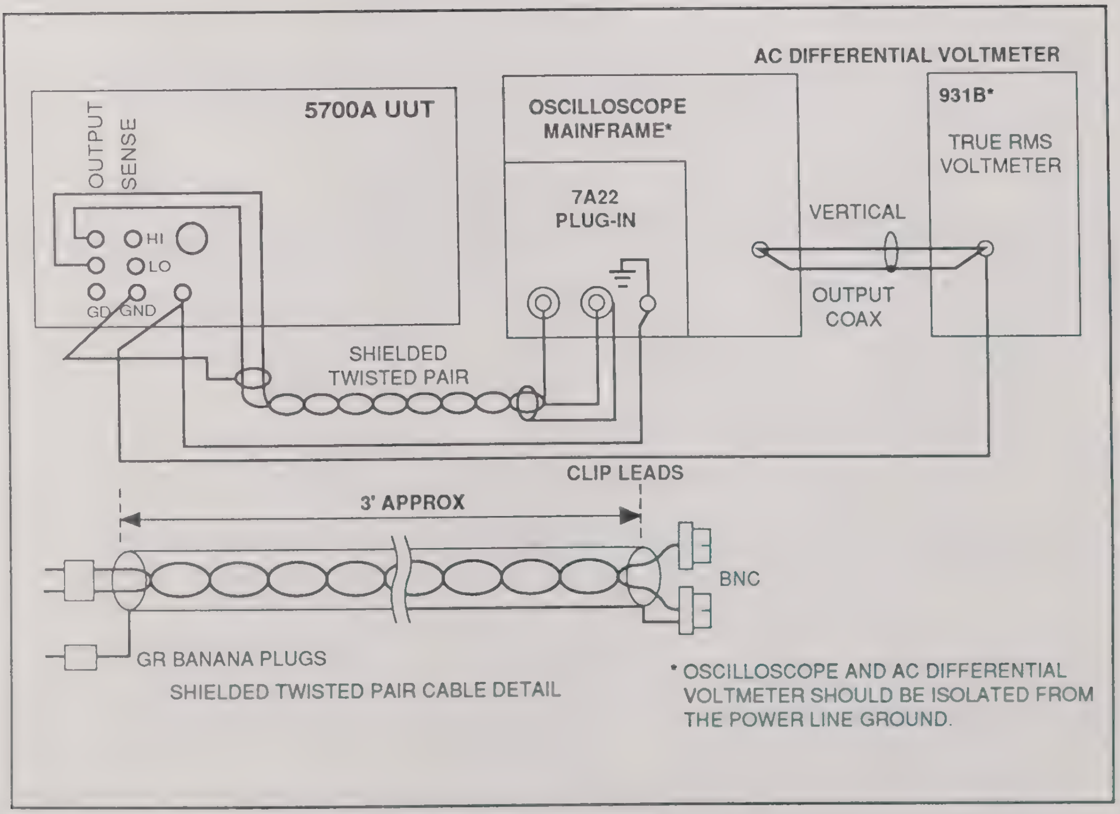
This test assumes that the amplifier plug-in and scope have a gain equal to 0.5V divided by the input/div. setting, which in the above case is 1 x 10^4.

6. Repeat the above process for the remaining tabulated settings shown in Table 3-23; verify that the rms meter indicates less than the amount shown for each required output level.

Table 3-23. DC Voltage Output Noise Test

DIFFERENTIAL AMPLIFIER SENSITIVITY	5700A OUTPUT	MAXIMUM RMS METER READING
50 uV/division	2.2V	150 mV
50 uV/division	10V	500 mV
50 uV/division	20V	500 mV
100 uV/division	200V	750 mV
500 uV/division	1000V	500 mV

7. Press RESET on the the 5700A and disconnect the test configuration. This completes the DC Voltage Optional tests.


AC DIFFERENTIAL VOLTMETER
5700A UUT
OUTPUT
SENSE
HI
LO
GD
GND
OSCILLOSCOPE MAINFRAME*
7A22 PLUG-IN
931B*
TRUE RMS VOLTMETER
VERTICAL
OUTPUT COAX
SHIELDED TWISTED PAIR
CLIP LEADS
3' APPROX
BNC
GR BANANA PLUGS
SHIELDED TWISTED PAIR CABLE DETAIL

* OSCILLOSCOPE AND AC DIFFERENTIAL VOLTMETER SHOULD BE ISOLATED FROM THE POWER LINE GROUND.

Figure 3-20. DC Voltage Output Noise Test

3-45. AC Voltage Distortion Test

Equipment required for these tests is listed in Table 3-24.

Table 3-24. Equipment Required for AC V Optional Tests

Distortion Analyzer	HP 334A or 8903A
Spectrum Analyzer	Tektronix 7L5
Non-wirewound load resistors	Stock Items (see Table 3-25 for values)

1. Connect the 5700A output terminals to the Distortion Analyzer.

2. Measure the 5700A distortion at the output voltages and frequencies tabulated in Table 3-25. Verify that the distortion measured is within the limits shown.

Table 3-25. AC Distortion Test

5700A OUTPUT	LOAD RESISTORS	FREQUENCY	MAX. DISTORTION
2V	100 ohm, 1/8W	10 Hz, 20 Hz	0.054%
		1 kHz, 20 kHz, 50 kHz,	0.044%
		100 kHz, 200 kHz, 500 kHz	0.355%
20V	1 kilohm, 1/2W	10 Hz, 20 Hz	0.0535%
		20 kHz, 100 kHz	0.0385%
		200 kHz, 500 kHz	0.304%
200V	10 kilohm, 5W	10 Hz, 20 Hz	0.055%
		50 kHz, 100 kHz	0.1065
300V	15 kilohm, 5W	10 Hz, 50 kHz, 70 kHz	0.07%

NOTE: The 5700A maximum volt-Hertz product is (2.2 x 10^7).

3-46. Wideband Distortion Testing

1. Connect the wideband output terminated in 50 ohms. If the spectrum analyzer input impedance is 50 ohms, do not use a separate termination.

2. With 0 dBm output programmed from the 5700A wideband output, select frequencies over the band of 1 MHz to 30 MHz and verify that use the spectrum analyzer to verify that any harmonics are below -40 dBm for fundamentals up to 10 MHz and below -34 dBm for fundamentals of 10 MHz and above.

3. Disconnect the equipment from the 5700A.

3-47. AC Voltage Overshoot Test

1. Connect the 5700A output to a properly compensated 10:1 probe.
2. AC couple the oscilloscope and set the sweeptime to a fairly low sweeptime (approximately 1 sec/div).
3. Set the 5700A to 7.07V at 1 kHz, and press OPR/STBY.
4. Set the scope vertical sensitivity for 0.05V/div. Offset the trace vertically until you can see the top of the waveform at the approximately center of the display (must be at least 2-3 divisions down from the top of the scope graticule).
5. Set the 5700A to standby and then back to operate. Verify that any overshoot visible on the oscilloscope display is less than 1.5 divisions (approximately 10% of the peak value).
6. Repeat the test at 100 Hz and 100 kHz. This completes the Optional Tests.

3-48. MINIMUM USE REQUIREMENTS

Table 3-26 defines specifications for test equipment needed for tests in this section of the manual. If the specific test equipment called for in these tests is not available, substitute equipment meeting these specifications can be used.

Table 3-26. Minimum Use Requirements

ITEM NO.	DESCRIPTION	MINIMUM USE SPECIFICATIONS	RECOMMENDED EQUIPMENT
		CALIBRATION EQUIPMENT	
1.	Voltage Reference	10V nominal, true value certified to within ±1.5 ppm	Fluke 732A
2.	Standard Resistors	1 ohm nominal, true value certified to within 10 ppm 10 kilohm nominal, true value certified to within 4 ppm	Fluke 742A Series, 1 ohm and 10 kilohm
		CALIBRATION VERIFICATION EQUIPMENT	
3.	Reference Voltage Divider	Range uncertainty: 100:1, 1 kV input, ±0.5 ppm 10:1, 100V input, ±0.2 ppm	Fluke 752A
4.	Null Detector	Leakage resistance to case: 10^12 ohms min. Resolution: 3 uV full scale	Fluke 854A
5.	Low Thermal EMF Cables	Plug-in or spade lug. Copper or gold-flashed copper (two cables per set, two sets required).	Fluke 5440-7002
6.	Digital Multimeter	DC Voltage Range: 0.1 to 10V Resolution and short-term stability: ±2 ppm Resistance range: 1 ohm to 10 megohms Resolution and short-term stability: ±20 microohms at 1 ohm, 1.9 ohms ±5 ppm at 10 ohms, 19 ohms ±2 ppm at 100 ohms to 1.9 megohms ±4 ppm at 10 megohms, 19 megohms	Fluke 850x
7.	Current Source	Range: 100 mA Typical short-term stability: ±15 ppm for 5 minutes	Fluke 5100B, 5700A, or EDC CR103/J

Table 3-26. Minimum Use Requirements (cont)

8.	AC/DC Transfer Standard (Thermocouple Type)	Ranges: 1 kV, 200V, 20V, and 2V Uncertainty: 1 kV; 50 Hz to 1 kHz: ±20 ppm 200V, 20V, 2V; 40 Hz to 20 kHz: ±20 ppm 200V, 20V, 2V; 10 to 20 Hz: ±125 ppm 200V, 20V, 2V; 20 to 40 Hz: ±40 ppm 200V, 20V, 2V; 20 to 50 kHz: ±40 ppm 200V, 20V, 2V; 50 to 100 kHz: ±60 ppm 200V, 20V, 2V; 100 to 300 kHz: ±125 ppm 200V, 20V, 2V; 300 to 500 kHz: ±250 ppm 200V, 20V, 2V; 500 kHz to 1 MHz: ±500 ppm	Holt 11 (Note 2)
9.	Transfer Standard	HFTC input; used as 7 mV dc output detector for item 8, and possibly as mentioned in Note 2.	Fluke 540B
10.	RMS Diff. Voltmeter	Range: 20 mV to 200mV; 10 Hz to 1 MHz Resolution: ±0.001%	Fluke 931B
11.	RMS Wideband Voltmeter	Range: 2 mV, analog dc output	Fluke 8922A
12.	Ratio Transformer	Range: 2V input at 1 kHz Uncertainty at ratio settings: 0.1 ±10 ppm; 0.01 ±15 ppm; 0.001 ±250 ppm	ESI DT72A
13.	RF Attenuators	50 ohms impedance +/1% at dc RF attenuation rated to 1 GHz minimum Flatness to 1 MHz: negligible error 20 dB (3 ea.), 10 dB (1 ea.) (Note 3)	Tektronix 017-0078-00 (20 dB)
14.	Frequency Counter	10 Hz to 30 MHz ±0.002%	Philips PM 6669
15.	Standard Resistors	0.1 ohm nominal, true value certified to within 20 ppm 1 ohm nominal, true value certified to within 20 ppm 1.9 ohms nominal, true value certified to within 20 ppm 10 ohms nominal, true value certified to within 7 ppm 100 ohms nominal, true value certified to within 4 ppm 1 kilohm nominal, true value certified to within 3 ppm 10 kilohms nominal (same as item 2) 19 kilohms nominal, true value certified to within 3 ppm 19 megohms nominal, true value certified to within 12 ppm	L&H 0.1 Fluke 742A Series or equiv.

Table 3-26. Minimum Use Requirements (cont)

16. DC Shunt (Note 4)	Range: 10A Uncertainty: ±0.008%	Fluke Y5020
17. AC/DC Shunt	Ranges: 10A and 2A, 40 Hz to 10 kHz ±100 ppm, 40 Hz to 5 kHz ±800 ppm, 5 kHz to 10 kHz	Fluke A40
18. Differential Amplifier	Sensitivity: 5 uV rms Bandwidth selectable to 10 kHz	Tektronix 7A22 w/7000-Series Mainframe
19. Distortion Analyzer	Range: 2V to to 300V Frequency: 10 Hz to 600 kHz	HP 334A or HP 8903A
20. Thermal Voltage Converter (TVC)	Range: 3V, 10 Hz to 30 MHz AC/DC difference: to 2 MHz: ±0.05% to 10 MHz: ±0.1%, to 20 MHz: ±0.15% to 30 MHz: ±0.25%	Fluke A55
21. Kelvin-Varley Voltage Divider	Ratio uncertainty: ±0.1 ppm of input	Fluke 720A
22. HV Decoupling Network	Used to decouple voltage above 2V to measure dc V output noise to 15 kHz bandwidth.	See Figure 3-21

Note 1: A Fluke 8500 Series DMM may be used for all but the 1 ohm and 1.9 ohm values. For those values using the 8500 Series, a test method using an external current source is used for low-value resistance.

Note 2: The Holt 11 draws 10 mA at 1 kV. The 5700A supplies 6 mA at voltages above 220V without a 5725A Amplifier attached. Therefore, another transfer device must be used at 1 kV unless a 5725A is attached. Substitute a Fluke 540B.

Note 3: The 10 dB attenuator is needed only for testing the Wideband AC Voltage Module (Option 5700A-03).

Note 4: Needed only for 5725A Amplifier testing.

Table 3-27. Test Record for Full Verification (cont)

Resistance Test Summary

1 OHM STD RES VALUE	1 OHM STD VOLTAGE	MEASURED 1 OHM STD VOLTAGE	CAL CURRENT	UUT 1 OHM DISPLAYED VALUE	UUT 1 OHM VOLTAGE	UUT TRUE RES.	UUT DEVIATION FROM DISPLAYED VALUE	LIMIT OF DEVIATION FROM DISPLAYED VALUE	MAXIMUM DIFFERENCE OF CHARACTERIZED TO NOMINAL VALUE
								+/-94 ppm	.9995 to 1.0005

10 OHM STD RES VALUE	10 OHM STD VOLTAGE	MEASURED 1 OHM STD VOLTAGE	CAL CURRENT	UUT 1 OHM DISPLAYED VALUE	UUT 1 OHM VOLTAGE	UUT TRUE RES.	UUT DEVIATION FROM DISPLAYED VALUE	LIMIT OF DEVIATION FROM DISPLAYED VALUE	MAXIMUM DIFFERENCE OF CHARACTERIZED TO NOMINAL VALUE
								+/-28.5 ppm	9.997 to 10.003

RESISTANCE ACCURACY VERIFICATION (19 OHM AND ABOVE)

	STD RES VALUE	DMM STD RES RDG	DMM ERROR	DMM UUT RES RDG	UUT TRUE RES VALUE	UUT DEVIATON FROM DISPLAYED VALUE		
19 ohm (1)							+/-26 ppm	18.9943 to 19.0057
100 ohm (1)							+/-17 ppm	99.985 to 100.015
190 ohm (1)							+/-17 ppm	189.9715 to 190.0285
1 kilohm (1)							+/-12 ppm	999.85 to 1000.15
1.9 kilohm (1)							+/-12 ppm	1.899715k to 1.900285k
10 kilohm							+/-11 ppm	9.9985k to 10.0015k
19 kilohm							+/-11 ppm	18.99715k to 19.00285k
100 kilohm (1)							+/-13 ppm	99.985k to 100.015k
190 kilohm (1)							+/-13 ppm	189.9715k to 190.0285k
1 megohm (1)							+/-18 ppm	0.9998M to 1.0002M
1.9 megohm (1)							+/-19 ppm	1.89962M to 1.90038M
10 megohm							+/-37 ppm	9.997M to 10.003M
19 megohm							+/-47 ppm	18.9943M to 19.0057M
100 megohm (2)							+/-120 ppm	99.95M to 100.05M

Note 1: Not necessary to test due to 5700A internal calibration process.

Note 2: Due to extremely slow settling time (approximately 5 minutes to 0.005% and sensitivity to any nearby movement, use of the DMM to test 100 megohms to the specified 0.01% uncertainty is not practical and therefore is not recommended. For those who wish to test it, a suitable way is to use an ESI SR 1050 10M/step Hammon-type Resistance Transfer Standard and use it in conjunction with an ESI 242-series bridge to effect the measurement to the required uncertainty.

Table 3-27. Test Record for Full Verification (cont)

OUTPUT VOLTAGE TEST SUMMARY

DIVIDER SETTING	5700A RANGE	5700A OUTPUT (NOTE 1)	NULL DETECTOR READING (uV)	NULL DET LIMIT (uV p-p)	METER LIMIT (uV) RATTLE
0.1V	0.22V	0.1V		±1.45 uV (Note 2)	N/A
1V	2.2V	1V		±7.2 uV (Note 2)	0.55 uV
1V	11V	1V (Note 3)		±9 uV (Note 2)	2.2 uV
10V	11V	10V (Note 4)		±54 uV	3.5 uV
10V	22V	10V (Note 3)		±58 uV	5.5 uV
100V	220V	100V		±70 uV	7.5 uV
1000V	1100V	1000V		±86 uV	4.5 uV

TABLE NOTES

Note 1: On the 752A 0.1 and 1V ranges, the null detector polarity is reversed. A low input (5700A output) causes a positive null detector reading.

Note 2: Mathematically, the true 5700A output programmed is the certified value of the reference standard divided by the reference standard nominal value, multiplied by the required 5700A nominal output. In other words, the 5700A output is always programmed for the nominal output adjusted up or down by the same percentage as the certified value of the reference standard.

Note 3: Use Range Lock to obtain 1V on 11V and 10V on 22V range. Deactivate Range Lock before setting the next voltage output.

Note 4: Line regulation can be verified at this time by adjusting the autotransformer for a ±10% change in line voltage. The null detector reading must remain constant within ±1 uV.

Table 3-27. Test Record for Full Verification (cont)

AC VOLTAGE FREQUENCY ACCURACY		
FREQUENCY	TOLERANCE	ACTUAL
10 Hz	99.99 ms - 100.01 ms	
15 Hz	66.673 ms - 66.66 ms	
100 Hz	9.999 ms - 10.001 ms	
200 Hz	199.98 Hz - 200.02 Hz	
500 Hz	499.95 Hz - 500.05 Hz	
1 kHz	999.9 Hz - 1000.1 Hz	
5 kHz	4999.5 Hz - 5000.5 Hz	
10 kHz	9.999 kHz - 10.001 kHz	
140 kHz	139.986 kHz - 140.014 kHz	
200 kHz	199.98 kHz - 200.02 kHz	
500 kHz	499.95 kHz - 500.05 kHz	
1 MHz	0.9999 MHz - 1.0001 MHz	

Table 3-27. Test Record for Full Verification (cont)

AC VOLTAGE OUTPUT TEST

FREQUENCY	OUTPUT LEVEL	TRANSFER STANDARD CORRECTION	ERROR DISPLAY READING	CAL ERROR ADDING ERROR 1 kHz	90-DAY SPEC
1 kHz	2V				78.5 ppm
40 Hz	2V				78.5 ppm
20 kHz	2V				78.5 ppm
50 kHz	2V				140 ppm
100 kHz	2V				290 ppm
300 kHz	2V				515 ppm
500 kHz	2V				0.13%
1 MHz	2V				0.27%
20 Hz	2V				185 ppm
10 Hz	2V				600 ppm
1 kHz	2.3V (Note 1)				78.5 ppm
1 kHz	20V				78.5 ppm
40 Hz	20V (Note 2)				78.5 ppm
20 kHz	20V				78.5 ppm
50 kHz	20V				140 ppm
100 kHz	20V				270 ppm
300 kHz	20V				635 ppm
500 kHz	20V				0.155%
1 MHz	20V				0.325%
20 Hz	20V				185 ppm
10 Hz	20V				600 ppm
40 Hz	200V	Stability for 10 minutes: <± 7.5 ppm			
1 kHz	200V				85 ppm
40 Hz	200V				85 ppm
20 kHz	200V				85 ppm
50 kHz	200V				240 ppm
100 kHz	200V				600 ppm
20 Hz	200V				130 ppm
10 Hz	200V				600 ppm
20 kHz	300V (Note 3)				155 ppm
50 kHz	600V (Note 3)				378 ppm
100 kHz	600V (Note 3)				0.1375%
50 Hz	1000V (Note 4)				84 ppm
200 Hz	1000V (Note 4)				84 ppm
500 Hz	1000V (Note 4)				84 ppm
1 kHz	1000V (Note 4)				84 ppm
40 Hz	1000V (Note 3)				84 ppm
20 kHz	1000V (Note 3)				131 ppm

Table 3-27. Test Record for Full Verification (cont)

AC VOLTAGE OUTPUT TEST (CONT)

TABLE NOTES

Note 1:	This is a test of the bottom of the 20V range and will require re-referencing at 2.3 V dc.
Note 2:	Observe the 5700A output at 20V, 40 Hz for 10 minutes and verify it remains stable within ± 7.5 ppm. Return to 1 kHz and algebraically subtract from the reading any drift caused by the element.
Note 3:	Perform only for units with 5725A Amplifier attached. At 600V, use the 500V range on the 540B.
Note 4:	Maximum load current is 6 mA for 1 kV range without a 5725A attached.

Table 3-27. Test Record for Full Verification (cont)

AC VOLTAGE MILLIVOLT RANGES TEST SUMMARY

1 KHZ LEVEL VERIFICATION (200 MV, 20 MV, AND 2 MV RANGES)

UUT OUTPUT	RATIO TRANS. SETTING	931 200 mV READING	931 20 mV READING	8922/DMM 2 mV READING
2V @ 1 kHz	0.1		N/A	N/A
2V @ 1 kHz	0.01	N/A		N/A
2V @ 1 kHz	0.001	N/A	N/A	

UUT OUTPUT	UUT ERROR DISPLAY	LIMITS
200 mV @ 1 kHz		±150 ppm
20 mV @ 1 kHz		±410 ppm
2 mV @ 1 kHz		±0.261 ppm

FREQUENCY RESPONSE TESTING (200 MV, 20 MV, AND 2 MV RANGES)

Characterizing 200 mV Level of RMS Diff. Voltmeter:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Null
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to Null ±0.003%

200 mV Output Accuracy:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±150 ppm
20 kHz		±150 ppm
50 kHz		±380 ppm
100 kHz		±0.115%
300 kHz		±0.19%
1 MHz		±0.38%

Table 3-27. Test Record for Full Verification (cont)

AC VOLTAGE MILLIVOLT RANGES TEST SUMMARY (CONT)

FREQUENCY RESPONSE TESTING (200 MV, 20 MV, AND 2 MV RANGES) (CONT)

Characterizing 20 mV Level of RMS Diff. Voltmeter:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Null
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to Null ±0.01%

20 mV Output Accuracy:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±410 ppm 20 kHz
		±410 ppm 50 kHz
		±670 ppm 100 kHz
		±0.13% 300 kHz
		±0.195% 1 MHz
		±0.48%

Characterizing 2 mV Level of RMS Diff. Voltmeter:

FREQ.	RMS DIFF. VOLTMETER READING
1 kHz	Same as reading in 1 kHz Level Verification, ratio trans: 0.001
40 Hz	
20 kHz	
50 kHz	
100 kHz	
300 kHz	
1 MHz	
1 kHz	Return to first entry reading ±0.03%

2 mV Output Accuracy:

FREQ.	UUT ERROR DISPLAY	LIMITS
40 Hz		±0.261% 20 kHz
		±0.261% 50 kHz
		±0.287% 100 kHz
		±0.49% 300 kHz
		±0.87% 1 MHz
		±1.83%

Table 3-27. Test Record for Full Verification (cont)

DIRECT CURRENT ACCURACY VERIFICATION

CHARACTERIZING DC DMM @ ±200 MV AND ± 2.0V

+200 mV RDG	-200 mV RDG	+2.0V RDG	-2.0V RDG

OUTPUT CURRENT	STD RES VALUE	STD RES CORRECTION	UUT ERROR READING	UUT ACTUAL ERROR (A-B) REVERSE POL	LIMIT OF ERROR
+2A	0.1 ohm				±100 ppm
-2A	0.1 ohm				±100 ppm
+200 mA	10 ohm				±65 ppm
-200 mA	10 ohm				±65 ppm
+20 mA	10 ohm				±55 ppm
+2 mA	1 kilohm				±55 ppm
-2 mA	1 kilohm				±55 ppm
+200 uA	10 kilohm				±100 ppm

5725A AMPLIFIER DC CURRENT TEST

OUTPUT CURRENT	DC DMM RDG	SHUNT CERT VALUE	CAL ACTUAL CURRENT	LIMITS
-10A				±428 ppm
5A				±428 ppm
2A				±428 ppm
-2A				±428 ppm

ALTERNATING CURRENT ACCURACY VERIFICATION

OUTPUT CURRENT	FREQ	ACTUAL UUT ERROR	ERROR LIMITS
2A	40 Hz		±675 ppm
2A	1 kHz		±675 ppm
2A	5 kHz		±800 ppm
2A	10 kHz		±0.91%
200 mA	10 Hz		±725 ppm
200 mA	20 Hz		±400 ppm
200 mA	40 Hz		±350 ppm
200 mA	1 kHz		±350 ppm
200 mA	5 kHz		±0.1%
200 mA	10 kHz		±0.49%
20 mA	10 Hz		±725 ppm
20 mA	20 Hz		±400 ppm
20 mA	40 Hz		±160 ppm
20 mA	1 kHz		±160 ppm
20 mA	5 kHz		±0.125%
20 mA	10 kHz		±0.54%

Table 3-27. Test Record for Full Verification (cont)

ALTERNATING CURRENT ACCURACY VERIFICATION (CONT)

5725A AMPLIFIER TESTS

11A	40 Hz	±415 ppm
11A	1 kHz	±415 ppm
11A	5 kHz	±535 ppm
11A	10 kHz	±0.3368%

DMM 2V dc READING =

	DMM 2V ac READING	DMM AC-DC ERROR
10 Hz =		
20 Hz =		
40 Hz =		
1 kHz =		
5 kHz =		
10 kHz =		

DMM 2 mA dc READING = * Add 1 megohm to DMM Input

	EXPECTED 2 mA ac READING	ACTUAL 2 mA ERROR	ERROR LIMITS
10 Hz =			±725 ppm
20 Hz =			±400 ppm
40 Hz =			±160 ppm
1 kHz =			±160 ppm
5 kHz =			±0.175%
10 kHz =			±0.64%

DMM 200 uA dc READING = * Add 1 megohm to DMM Input

	EXPECTED 200 uA ac READING	ACTUAL 200 uA ERROR	ERROR LIMITS
10 Hz =			±850 ppm
20 Hz =			±505 ppm
40 Hz =			±240 ppm
1 kHz =			±240 ppm
5 kHz =			±0.575%
10 kHz =			±2.44%

Table 3-27. Test Record for Full Verification (cont)

FREQUENCY TESTING POINTS	
FREQUENCY (HZ)	TOLERANCE LIMITS
10 Hz	99.99 ms to 100.01 ms
100 Hz	9.999 ms to 10.001 ms
300 Hz	299.97 Hz to 300.03 Hz
500 Hz	499.95 Hz to 500.05 Hz
800 Hz	799.92 Hz to 800.08 Hz
900 Hz	899.91 Hz to 900.09 Hz
1 kHz	999.0 Hz to 1.0001 kHz
1.19 kHz	1.189881 kHz to 1.190119 kHz
2.2 MHz	2.19978 MHz to 2.20022 MHz
3.5 MHz	3.49965 MHz to 3.50035 MHz
3.8 MHz	3.79962 MHz to 3.80038 MHz
10 MHz	9.990 MHz to 10.001 MHz
20 MHz	19.998 MHz to 20.002 MHz
30 MHz	29.997 MHz to 30.003 MHz

WIDEBAND ACCURACY AT 1 KHZ			
OUTPUT LEVEL	8920A READING OF 5700A MAIN OUTPUT	WIDEBAND OUTPUT ERROR DISPLAY READING	LIMITS
3.0V			±.2167%
1.0V			±.2900%
0.3V			±.2833%
0.1V			±.3400%
30 mV			±.3333%
10 mV			±.3900%
3 mV			±.3833%
1 mV			±.4400%

Table 3-27. Test Record for Full Verification (cont)

Output Flatness and Attenuator Flatness Tests

FREQUENCY	50 OHM DETECTOR CHARACTERIZATION RMS WIDEBAND DC DMM READING	3V RANGE WIDEBAND FLATNESS TEST ERROR DISPLAY READING	LIMITS
1 kHz	.90000V	---	---
10 Hz			0.3%
30 Hz			0.1%
120 kHz			0.1%
500 kHz			0.1%
2 MHz			0.1%
5 MHz			0.2%
10 MHz			0.4%
20 MHz			0.4%
30 MHz			1.0%

ATTENUATOR FLATNESS TEST RECORD

FREQ	WIDEBAND DC DMM CHAR DATA	3V RANGE WIDEBAND FLAT TEST ERR DISPL	(60 dB) 1.0V OUTPUT	(50 dB) 300 mV OUTPUT	(40 dB) 100 mV OUTPUT	(30 dB) 30 mV OUTPUT	(20 dB) 10 mV OUTPUT	>3 mV LIMIT	(10 dB) 3 mV OUTPUT	3 mV LIMIT	(0 dB) 1 mV OUTPUT	1 mV LIMIT
1 kHz	.90000V	- 0 -	.90000V	.90000V	.90000V	.90000V	.90000V		.90000V		.90000V	
2 MHz								.1%		.1%		.5%
10 MHz								.4%		.5%		.5%
20 MHz								.4%		.5%		.5%
30 MHz								1%		1.5%		3.0%
1 kHz	<.02%		<.02%	<.02%	<.02%	<.02%	<.02%		<.02%		<.02%	

Section 4
Maintenance

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4-1. INTRODUCTION

This section covers the routines that form the middle ground between performance verification and troubleshooting and repair. These routines relate to periodic cleaning of the 5700A, as well as to the access procedures that would be necessary during troubleshooting and repair.

4-2. CLEANING THE AIR FILTER

CAUTION

Damage caused by overheating may occur if the area around the fan is restricted, the intake air is too warm, or the air filter becomes clogged.

The air filter must be removed and cleaned every 30 days or more frequently if the calibrator is operated in a dusty environment. The air filter is accessible from the rear panel of the calibrator.

To clean the air filter, refer to Figure 4-1 and proceed as follows:

1. Remove the filter element.
    - a. Unscrew the knurled screw at the top of the air filter (counterclockwise).
    - b. Pull the air filter retainer downward; it hinges at the bottom.
    - c. Remove the filter element.
2. Clean the filter element.
    - a. Wash the filter element in soapy water.
    - b. Rinse the filter element in fresh running water.
    - c. Shake out the excess water, then allow the filter element to dry thoroughly before reinstalling it.
3. Reinstall the filter element, its retainer, and the knurled screw.

4-3. GENERAL CLEANING

To keep the 5700A looking like new, clean the case, front panel keys, and lens using a soft cloth slightly dampened with water or a non-abrasive mild cleaning solution that does not harm plastics.

CAUTION

Do not use aromatic hydrocarbons or chlorinated solvents for cleaning. They can damage the plastic materials used in the calibrator.

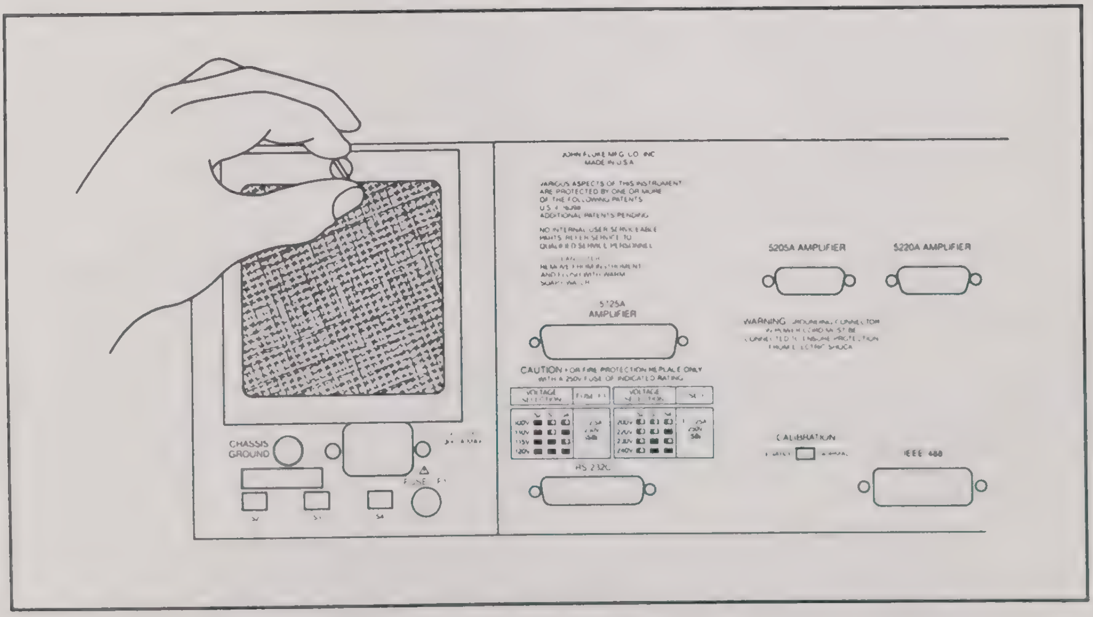

JOHN FLUKE MFG CO INC
MADE IN USA
5205A AMPLIFIER
5220A AMPLIFIER
5725A
AMPLIFIER
WARNING
CAUTION
VOLTAGE SELECTION
VOLTAGE SELECTION
100V
110V
115V
120V
200V
220V
230V
240V
CALIBRATION
IEEE 488
RS 232C
CHASSIS
GROUND

Figure 4-1. Air Filter

4-4. ACCESS PROCEDURES

WARNING

SERVICING DESCRIBED IN THIS SECTION IS TO BE PERFORMED BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING UNLESS QUALIFIED TO DO SO.

4-5. Top and Bottom Covers

Check that power is not connected to the 5700A; the power control must be off, and the line power cord must be disconnected. Top and bottom covers are each secured with eight Phillips head screws (four front, four rear).

4-6. Digital Section Cover

The Digital Section is accessed through one top cover that is secured by six Phillips head screws.

4-7. Analog Section Covers

The Analog Section is enclosed with separate covers on top and bottom. The top cover is secured with seven Phillips head screws. The bottom Analog Section cover is secured with eight Phillips head screws (three short, five longer).

4-8. Rear Panel Removal and Installation

Detach the Rear Panel by removing the six hex head screws (three on each rear handle side) and the two Phillips head screws found along the side of the Fan Assembly. Refer to Figure 4-2 for screw locations.

4-9. Rear Panel Assembly Access

Refer to Figure 4-3 during the following procedure:

1. Remove the six securing screws for the Rear Panel assembly housing.

2. Gently pull the rear panel housing from the Rear Panel.

3. Allow the rear panel housing to lay flat on the work surface by removing the two ribbon cables from the Rear Panel board.

4. Remove the two nuts at TB1 and TB2 on the paddle board; separate the associated wires from the paddle board.

5. Remove P11 from J11. Then remove the two paddle board mounting screws and separate the paddle board from the Rear Panel assembly.

6. Remove the jack screws for each connection on the rear panel housing, then gently lift the Rear Panel assembly out from the housing.

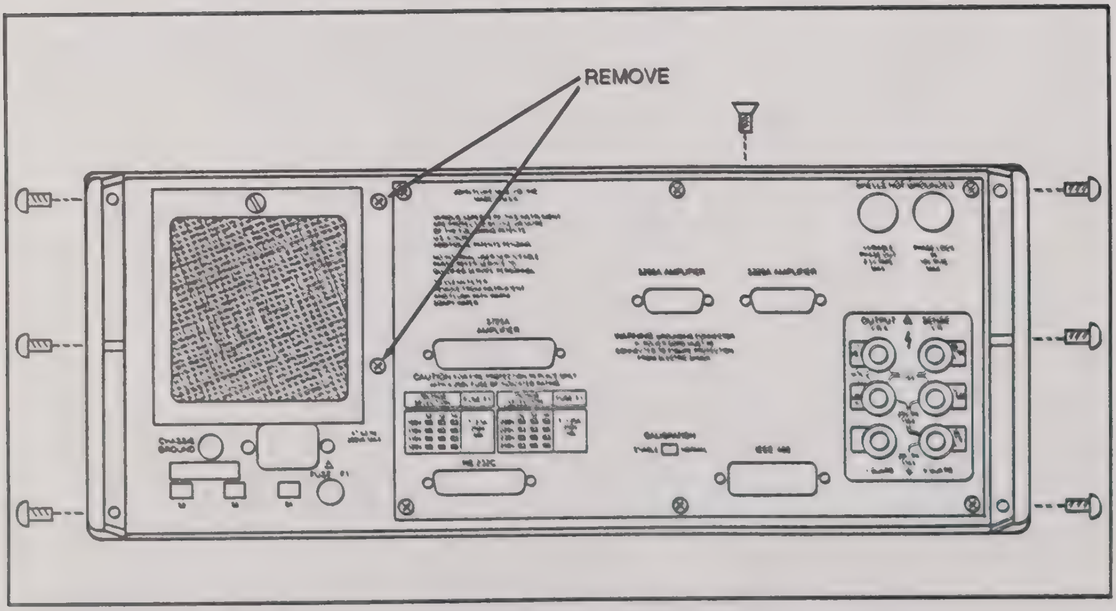
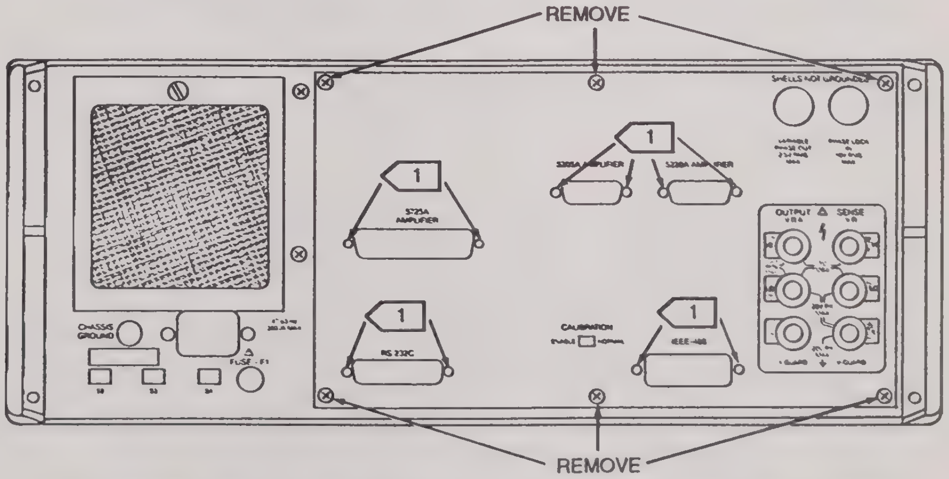

REMOVE
OUTPUT
SENSE
CALIBRATION
RS 232C
IEEE 488
CHASSIS GROUND

Figure 4-2. Rear Panel Removal


REMOVE
1
5725A AMPLIFIER
5205A AMPLIFIER
5220A AMPLIFIER
SHELLS NOT GROUNDED
OUTPUT
SENSE
CHASSIS GROUND
FUSE - F1
RS 232C
CALIBRATION
ENABLE
NORMAL
IEEE-488
REMOVE

1 REMOVE JACK SCREWS TO SEPARATE THE REAR PANEL CIRCUIT BOARD FROM THE METAL HOUSING.

Figure 4-3. Rear Panel Assembly Access

7. Reverse this procedure to install the Rear Panel assembly.

4-10. Front Panel Removal and Installation

Refer to Figure 4-4 during the following procedure:

1. Remove the 5700A top and bottom covers.

2. Remove the single screw at the top of the Front Panel and the six hex screws on the front handle sides. Then grasp both handles and gently tilt the Front Panel away down and away from the mainframe, disengaging the green power button. Position the Front Panel on its handles, in front of the instrument.

3. If you need to completely detach the Front Panel from the 5700A, one, or possibly two, cables must be disconnected. The output cable must be detached in all configurations. If the Wideband Option is installed, you must also detach the related connector from the Front Panel.

Reverse this procedure to install the Front Panel.

4-11. DISPLAY ASSEMBLY REMOVAL AND INSTALLATION

Once the Front Panel has been removed, use the following procedure to access the Display assembly.

1. Remove the ribbon cable connecting the Display assembly to the Motherboard.

2. Remove the six screws securing the Front Panel Display assembly cover shield. Three of these screws are accessed from the inside, and the other three are accessed along the top of the front panel.

3. Remove the seven screws securing the Front Panel Display assembly to the Front Panel. Gently lift the Front Panel Display assembly up, and remove the keyboard ribbon cable. Now remove the Front Panel Display assembly.

Reverse this procedure to install the Front Panel Display assembly.

4-12. KEYBOARD ASSEMBLY REMOVAL AND INSTALLATION

The following procedure assumes that the Display Assembly Removal procedure has already been completed.

1. Remove all output cable connections (including GROUND-to-metal) from the front panel binding posts. Save all removed hardware.

2. Remove the two hex screws at the front of each handle. Then remove the front handles.

3. Gently release the eight plastic hook catches, and separate the front panel plastic from the sheet metal.

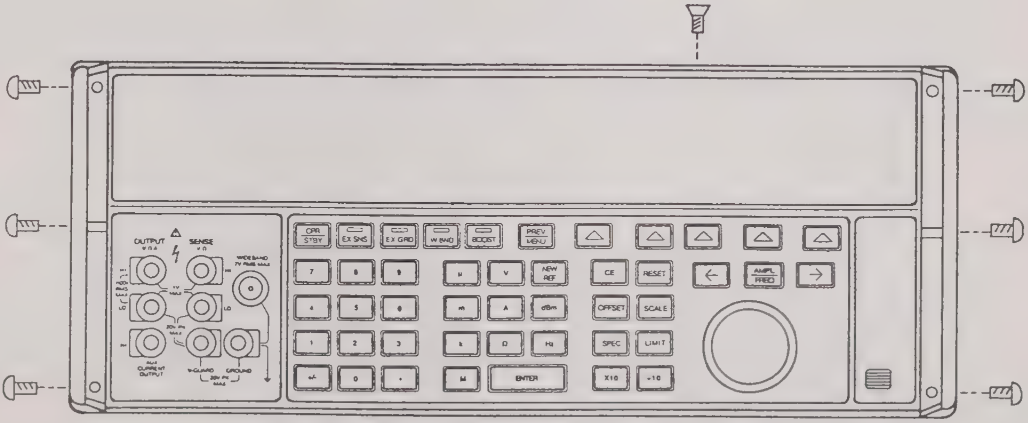

OUTPUT
SENSE
WIDEBAND
OPR
STBY
EX SNS
EX GRD
W BND
BOOST
PREV
MENU
7
8
9
μ
V
NEW
REF
CE
RESET
AMPL
FREQ
4
5
6
m
A
dBm
OFFSET
SCALE
1
2
3
k
Ω
Hz
SPEC
LIMIT
+/-
0
.
M
ENTER
X10
÷10
CURRENT
OUTPUT
GUARD
GROUND
HI
LO

Figure 4-4. Front Panel Removal

4. Remove the output adjustment knob flywheel by taking out its center screw. Hold the wheel in place by inserting a pencil in one of the flywheel holes and pressing on one of the plastic standoffs.

5. Remove the nine self-tapping screws connecting the Keyboard assembly to the front panel plastic.

6. Remove the Keyboard assembly by gently releasing the seven plastic hook catches. Work from one side of the board to the other. Start at either side by simultaneously releasing a catch and lifting on the board.

Reverse this procedure to install the Keyboard assembly. When reconnecting the wires to the binding posts, be sure to include a washer on each side of the ring terminals. Refer to the nearby decal or see sheet 4 of the Analog Motherboard schematic in Section 8 of this manual for proper connection of the output cable to the front binding posts.

CAUTION

Do not tighten the nuts that hold the wires to the binding posts more than 7 in-lb. Force exceeding 7 in-lb can destroy the binding posts.

4-13. Analog Assembly Removal and Installation

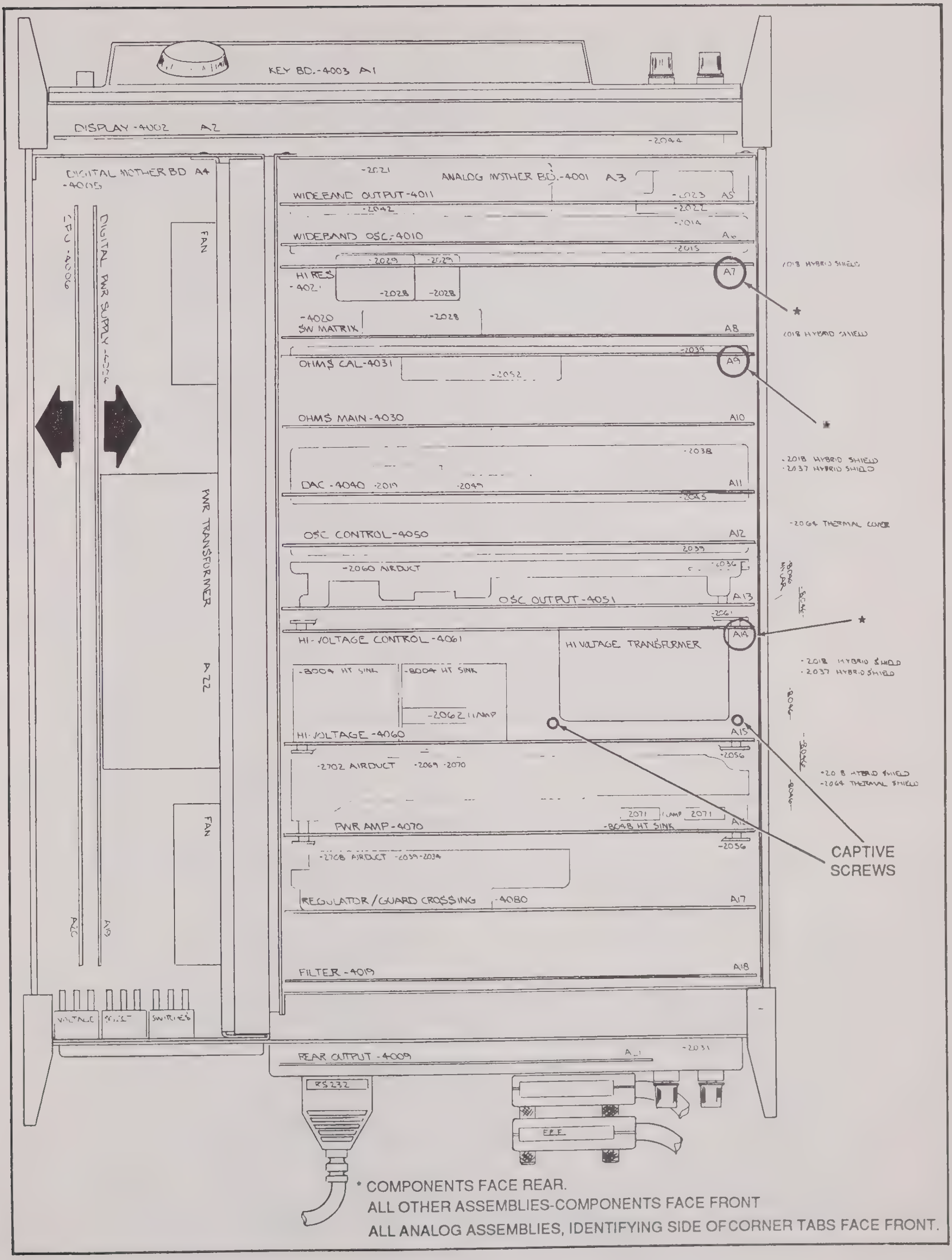
The analog assemblies are installed in the sequence shown in Figure 4-5. Note that each module cannot be positioned in any other slot and that identifying information on the tab for each module faces forward. In most cases, the component side of each module also faces forward. The component side faces to the rear for three modules: Current/High Resolution Oscillator (A7), Ohms Cal (A9), and High Voltage Control (A14). All modules except the High Voltage Control pull straight up to disengage from the Digital Motherboard. For the High Voltage Control module, two Phillips head captive screws at the outer corners of the High Voltage Transformer must be removed before the module can be removed.

CAUTION

Do not touch any circuit area on an analog assembly. Contamination from skin oil can produce high resistance paths, with resulting leakage currents and possible erroneous readings. Always grasp an analog assembly by its upper corner ears.

4-14. Digital Assembly Removal and Installation

Remove the CPU Assembly or the Digital Power Supply Assembly by pulling straight up at the top corners of the assembly. In relation to the chassis side, the CPU Assembly components face toward, and the Digital Power Supply Assembly components face away. See Figure 4-5.


KEY BD.-4003 A1
DISPLAY-4002 A2
-2044
DIGITAL MOTHER BD A4 -4005
CPU-4006
DIGITAL PWR SUPPLY
FAN
PWR TRANSFORMER
A22
FAN
VOLTAGE
SWITCHES
ANALOG MOTHER BD.-4001 A3
-2021
WIDEBAND OUTPUT-4011
-2023 A5
-2042
-2022
-2014
WIDEBAND OSC-4010
A6
-2015
-2029
-2029
HI RES -4021
-2028
-2028
A7
2018 HYBRID SHIELD
-4020 SW MATRIX
-2028
A8
2018 HYBRID SHIELD
-2039
OHMS CAL-4031
-2052
A9
OHMS MAIN-4030
A10
-2038
DAC-4040 -2019 -2049
A11
-2045
-2018 HYBRID SHIELD
-2037 HYBRID SHIELD
OSC CONTROL-4050
A12
-2064 THERMAL COVER
2039
-2060 AIRDUCT
-2036
OSC OUTPUT-4051
A13
-2061
HI-VOLTAGE CONTROL-4061
HI VOLTAGE TRANSFORMER
A14
-2018 HYBRID SHIELD
-2037 HYBRID SHIELD
-8004 HT SINK
-8004 HT SINK
-2062 CLAMP
HI-VOLTAGE-4060
A15
-2056
-2702 AIRDUCT -2069 -2070
-2018 HYBRID SHIELD
-2064 THERMAL SHIELD
2071 CLAMP 2071
PWR AMP-4070
-8048 HT SINK
A16
-2056
CAPTIVE SCREWS
-2708 AIRDUCT -2039-2034
REGULATOR/GUARD CROSSING -4080
A17
FILTER-4019
A18
A20
A19
REAR OUTPUT-4009
-2031
RS232

* COMPONENTS FACE REAR.

ALL OTHER ASSEMBLIES-COMPONENTS FACE FRONT

ALL ANALOG ASSEMBLIES, IDENTIFYING SIDE OF CORNER TABS FACE FRONT.

Figure 4-5. Analog and Digital Assemblies

4-15. Power Transformer Removal and Installation

Use the following procedure to remove the Power Transformer assembly:

1. Remove the 5700A Front and Rear Panels.
2. Remove the Digital Power Supply (A19) and CPU (A20) assemblies.
3. Detach the five connectors leading from the Power Transformer assembly to the Digital Motherboard. The three connectors at the rear of the assembly may not be accessible without first removing the rear fan. With the two digital assemblies (A19 and A20) removed, the four Phillips head screws securing this fan can be accessed through holes in the chassis side.

   Note that no two Power Transformer connectors are the same size and that each connector is keyed; re-connection only involves matching appropriate connectors.
4. Working from the bottom of the instrument, remove the Digital Motherboard (A4) assembly.
5. Remove the eleven screws securing the Power Transformer assembly, as follows:
   - o Rear Panel: two screws, which were removed along with the Rear Panel.
   - o Front Panel: two screws.
   - o Top Edge: four screws.
   - o Bottom Edge: three screws.
6. Remove the Power Transformer assembly.

To install the Power Transformer assembly, reverse the preceding six steps.

4-16. Hybrid Cover Removal

When removing the plastic covers from the hybrid assemblies, push the ends of the cover retainer pins through from the back of the circuit board. The retainer pins can be damaged by attempting to pull the covers off.

4-17. FRONT/REAR BINDING POST RECONFIGURATION

An internal cable can be configured for output connections at either the front or rear binding posts. The front binding posts are usually connected at the factory. If the rear binding posts are connected at the factory, a decal describing this arrangement is attached to the front binding posts. The procedure that follows can be used to swap an existing binding post configuration; it is to be done only at Service

Centers. The following procedure can be used to change front-to-rear or rear-to-front.

Reverse this procedure when changing from rear to front output operation.

1. Remove instrument top and bottom covers and remove bottom analog guard cover.

2. Remove the instrument front panel by removing the three hex screws on each front handle side and a single screw on the top of the front panel. See Figure 4-4 for screw locations. By grasping the handles gently pull the front panel away from the frame and lay it on its handles in front of the instrument.

3. Remove all the wires connecting the ring terminals of the output cable to the front panel binding posts. Save all hardware removed during this step.

4. Remove the two screws and restraining board attaching the toroid to the Front Panel. Save these items.

5. Position the output cable and toroid along the bottom left side of the instrument. In a later step, the output cable will be positioned between the Analog Motherboard and the left side panel.

6. Install the Front Panel.

7. Detach the Rear Panel by removing six hex screws (three on each rear handle side) and two screws near the the fan filter on the Rear Panel. See Figure 4-2 for screw locations. Then grasp the handles and gently pull the Rear Panel away from the frame.

8. Orient the instrument so that it is resting on its right side panel, with its bottom facing you.

9. Route the output cable between the left side panel and the Analog Motherboard, ending at the Rear Panel.

10. Using the items obtained during toroid removal, attach the toroid to the two rear panel standoffs.

11. Attach the color-coded output leads to the rear output binding posts. Use one washer on each side of each connecting ring. Verify connections by checking the decal mounted nearby or by matching lead color to the color on the front of the binding post. (Of the eleven wires, four are clear-insulated shield wires. If necessary, refer to page 4 of the Analog Motherboard schematic in Section 8 to determine these connections.)

CAUTION

Do not overtighten hardware on the binding posts. Torque in excess of seven inch-pounds can damage a binding post.

Note that the I GUARD terminal is not connected at the front binding posts; cut away the I GUARD thermal fit covering to connect this terminal at the rear binding posts. Also, the AUX CURRENT ring terminal is not connected at the rear binding posts; this terminal must be insulated and tied off.

12. Replace the rear panel back, the bottom guard cover, and top and bottom covers to complete this procedure.

4-18. REPLACING THE CLOCK/CALENDAR BACKUP BATTERY

To replace the lithium button-type battery on the CPU Assembly (A20), proceed as follows:

1. Make sure the power is off and the line power cord disconnected.
2. Follow the access procedures to remove the digital side cover.
3. Remove the CPU Assembly (A20).
4. Desolder and remove battery BT1.
5. Solder a replacement battery in place (refer to the parts list for replacement information if necessary.)
6. Replace the CPU Assembly. After replacing the battery, the setting of the time and date the elapsed time counter (read by the remote query ETIME? and set by ETIME) will need to be reprogrammed.

4-19. USING REMOTE COMMANDS RESERVED FOR SERVICING

This information documents remote commands not described in the 5700A Operator Manual, Section 5. The commands described here are useful for servicing the instrument.

4-20. Using the ETIME Command

The ETIME remote command is the companion to ETIME?, the elapsed time query, which is documented in the Operator Manual. The ETIME? query tells you how many minutes the 5700A has been in the power on state since the instrument was built. If you replace the CPU Assembly (A20), the clock/calendar battery (BT1), or the clock/calendar IC (U33), you will lose the setting of ETIME. The ETIME command gives you a way to set this counter to where it was before servicing the instrument. (If possible, read the counter first using ETIME?.) The syntax for this remote command is as follows:

ETIME

Description:

Sets the elapsed time counter to any number of minutes from 0 to 2,147,483,647. The setting of this counter is read by the ETIME? query, described in the 5700A Operator Manual. (Seqential command.)

Parameter:

1. SET_TO
2. Integer, number of minutes

Example:

```
ETIME SET_TO, 4628000
```

4-21. Using the FATALITY? AND FATALCLR Commands

The FATALITY? query recovers fault codes that were logged when a fatal problem occurred. These faults are logged into a separate fault queue. Once the faults are read from the queue, you can clear the queue by sending the FATALCLR command. The syntax for these remote commands are as follows:

FATALITY?

Description:

Returns the list of the fatal faults logged since the list was last cleared by the FATALCLR command. (Seqential command.)

Parameter:

None

Response:

(String) The list of faults, one per line in the following format:

<date> <time> <fault code> <fault description string> <EOL>

Example:

```
"
8/30/88  6:33:49 Fault  4301: Rom Checksum
8/30/88  6:34:05 Fault  4301: Rom Checksum
8/30/88  6:34:12 Fault  4301: Rom Checksum
8/30/88  6:34:13 Fault  4301: Rom Checksum
8/30/88  6:34:14 Fault  4301: Rom Checksum
8/30/88  6:34:15 Fault  4301: Rom Checksum
8/30/88  6:34:16 Fault  4301: Rom Checksum
"
```

FATALCLR?

Description:

Clears the the list of the fatal faults logged since the list was last cleared by the FATALCLR command. The list is read by the FATALITY? query. (Seqential command.)

Parameter:

None

Section 5
Troubleshooting

5-1. INTRODUCTION 5-3
5-2. DIAGNOSTIC FAULT CODES 5-3

5-1. INTRODUCTION

Information in this section provides guidance in using self-diagnostics fault codes to isolate a problem. The descriptive text helps to quickly locate the source of a fault.

5-2. DIAGNOSTIC FAULT CODES

Run self diagnostics by pressing the following sequence of softkeys:

"Setup Menus" ---> "Self Test & Diags"

Self test diagnostics of the analog circuitry are carried out with the 5700A binding posts open circuited. (Cables and test equipment left connected to the binding posts have no effect.)

Test routines connect specific points to the SDL or RCL line and measuring for an expected voltage and tolerance. The SDL and RCL lines are routed to the adc circuit on the DAC assembly for measurement.

Fault code descriptions generally indicate the instrument's test configuration, point being measured, expected voltage, and probable assembly which is at fault. In some cases, an addition manual measurement may be required to determine the faulty assembly. These manual measurements are noted with the related fault code description. In all cases it is assumed that the Motherboard assemblies are fully operational. Power Supply faults assume that other, non-power supply related assemblies are not loading down the Power Supply.

2700 A7: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Current/Hi Res assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2701 A7: 8255 Port A Fault

The diagnostics software writes and reads data to port A of the 8255 IC on the Current/Hi Res assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2702 A7: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the Current/Hi Res assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2703 A7: 8255 Port C Fault

The diagnostics software reads port C of the 8255 IC on the Current/Hi Res assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2704 Spare

This fault code is not used.

2705 A7: Oven Regulation Fault

The heater voltage of the current hybrid is measured by dividing OVEN TEMP down and connecting it to the SDL line where it is measured by the adc circuit on the DAC assembly to ensure the hybrid is warmed up and regulating. OVEN TEMP should be 0.7V ±10% ±0.2V. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2706 A7: Current Compliance Fault

The Current assembly is configured into each of its ranges in both the dc and ac mode. The output current is connected to the 1.2 ohm load resistor. The compliance voltage is determined by measuring the output side of the shunt resistor via the Current/Compliance Voltage Monitor circuit. This fault occurs if the voltage is 10% over the expected. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2707 A7: Hardware Initialization Fault

This fault occurs if the diagnostics software was unable to properly set the Current assembly hardware for diagnostics testing. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2708 Spare

This fault code is not used.

2709 A7: Current Magnitude Fault

The Current assembly is configured into each of its ranges in both the dc and ac mode. The output current is connected to the 1.2 ohm load resistor and the current is calculated by measuring the voltage drop across the shunt resistance. This fault occurs if the voltage is 10% over the expected. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2710 A7: Dummy Load Current Fault

The Current assembly is configured into each of its dc ranges. The output current is connected to the 1.2 ohm load resistor and the resulting voltage on DUMMY LOAD is connected to the SDL line where it is measured by the adc circuit on the DAC assembly. This fault occurs if the current is over 10% ±5 mA of the output current. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2711 Assembly A7 Is Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Current assembly is not responding. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2712 A7: Hi-Res Clock Fault

The Hi Res clock circuit is checked by connecting HI-RES CLOCK to the SDL line which is measured by the adc circuit on the DAC assembly for 2.5V ±200 mV. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2713 A7: Hi-Res Loop In 100HZ Range

The instrument is set for 2.0V at 100 Hz operation. The input voltage to the VCO circuit is resistively divided to create the control line HI-RES LOOP. HI-RES LOOP is connected to the SDL line where it is measured by the adc circuit on the the DAC assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2714 A7: Hi-Res Loop In 1KHz Range

The instrument is set for 2.0V at 900 Hz operation. The input voltage to the VCO circuit is resistively divided to create the control line HI-RES LOOP. HI-RES LOOP is connected to the SDL line where it is measured by the adc circuit on the the DAC assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2715 A7: Hi-Res Loop In 10KHZ Range

The instrument is set for 2.0V at 11 kHz operation. The input voltage to the VCO circuit is resistively divided to create the control line HI-RES LOOP. HI-RES LOOP is connected to the SDL line where it is measured by the adc circuit on the the DAC assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2716 A7: Hi-Res Loop In 100KHZ Range

The instrument is set for 2.0V at 70 kHz operation. The input voltage to the VCO circuit is resistively divided to create the control line HI-RES LOOP. HI-RES LOOP is connected to the SDL line where it is measured by the adc circuit on the the DAC assembly. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2717 A7: Hi-Res Loop In 1MHZ Range

The instrument is set for 2.0V at 121 kHz, 600 kHz, and 1.19 MHz operation. The input voltage to the VCO circuit is resistively divided to create the control line HI-RES LOOP. HI-RES LOOP is connected to the SDL line where it is measured by the adc circuit on the the DAC assembly at each frequency. This fault occurs if the VCO input voltage is not within 25% ±1.0V of the expected voltage. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2718 Fault In Setting Up AC For Diagnostics

This fault occurs if the diagnostics software was unable to properly set the Hi-Resolution Oscillator hardware for diagnostics testing. A failure indicates the Current/Hi Res (A7) assembly is probably at fault.

2719 A7: 8255 Was Reset

The control word of the 8255 on the Current/Hi Res assembly is determined to be incorrect. A failure indicates the Current/Hi Res assembly is probably at fault.

2800 A11: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the DAC assembly. A failure indicates the DAC (A11) assembly is probably at fault.

2801 A11: 8255 Port A Wires

The diagnostics software writes and reads data to port A of the 8255 IC on the DAC assembly. A failure indicates the DAC (A11) assembly is probably at fault.

2802 A11: 8255 Port B Data Bus

The diagnostics software reads port B of the 8255 IC on the DAC assembly. A failure indicates the DAC (A11) assembly is probably at fault.

2903 A11: 82C54 Status Words

The diagnostics software reads the status of the 82C54 IC on the DAC assembly. A failure indicates the DAC (A11) assembly is probably at fault.

2804 A11: DAC Heaters Not Regulated

The instrument is dormant and the heater voltages (REF HEATER and DCAMP HEATER) to the hybrid assemblies are measured to be 0.7V ±10% ±0.2V. A failure indicates the DAC (A11) assembly is probably at fault.

2805 5700 Not Warmed Up

If a heated hybrid assembly in the instrument is detected to not be in regulation the length of time since the last reset is checked. This fault occurs if the time is less than ten minutes since a reset.

2806 A11: ADC Amp Output Noise

The instrument is dormant. The ±inputs of the DACs adc amplifier circuit are connected to common and the adc then takes ten readings. This failure occurs if the difference between the lowest value and highest value of the ten readings is greater than 500uV. A failure indicates the DAC (A11) assembly is probably at fault.

2807 A11: ADC Amp Output Offset

The instrument is dormant. The ±inputs of the DACs adc amplifier circuit are connected to common and the adc then takes ten readings. This failure occurs if the average of the ten readings is greater than 3 mV. A failure indicates the DAC (A11) assembly is probably at fault.

2808 A11: ADC Amp Gain Error

The DAC is set to 0.1V on the 11V range and connected to the +input of the DACs adc amplifier circuit and the -input is connected to common. The adc amplifier has a nominal gain of 11 resulting in 1.1V at the adc amplifier output. This gain is checked to be 11 ±5%. A failure indicates the DAC (A11) assembly is probably at fault.

2809 A11: DAC Monitoring Fault

The DAC is set to 1.0V and routed to the adc circuit via DAC HI DIAG. This 1V from the DAC is divided by R70 and R84 on the DAC before going to the adc circuit where it is measured. The DAC is then set to 10V and another reading is taken by the adc. The exact gain of the divider resistors can now be determined by the formula gain=(10V-1V)/adc10-adc1. A failure occurs if the detected gain is not within 10% of the nominal 22.13. A failure indicates the DAC (A11) assembly is probably at fault.

2810 A11: +11V DC Range Fault

The instrument is configured in the +11V dc range. The DAC is sequentially set to 0V, 1V, and 10V. The DAC output is measure at each setting to be within 7% ±10 mV via DAC HI DIAG by the adc circuit. A failure indicates the DAC (A11) assembly is probably at fault.

2811 **A11: -11V DC Range Fault**

The instrument is configured in the -11V dc range. The DAC is sequentially set to 0V, -1V, and -10V. The DAC output is measure at each setting to be within 7% ±10 mV via DAC HI DIAG by the adc circuit. A failure indicates the DAC (A11) assembly is probably at fault.

2812 **A11: +22V DC Range Fault**

The instrument is configured in the +22V dc range. The DAC is sequentially set to 0V, 2V, and 21.9V. The DAC output is measure at each setting to be within 7.2% ±10 mV via DAC HI DIAG by the adc circuit. A failure indicates the DAC (A11) assembly is probably at fault.

2813 **A11: -22V DC Range Fault**

The instrument is configured in the -22V dc range. The DAC is sequentially set to 0V, -2V, and -21.9V. The DAC output is measure at each setting to be within 7.2% ±10 mV via DAC HI DIAG by the adc circuit. A failure indicates the DAC (A11) assembly is probably at fault.

2814 **A11: 6.5V Buffered Reference Fault**

The DAC's 6.5V buffered reference (BRF6 and BSRF6) is connected to the -input of the adc circuit and the DAC output (DAC SENSE CAL) is connected to the +input. The 6.5V buffered reference is measure by adjusting the DAC until a null is achieved. This fault occurs if the 6.5V buffered reference is over 10% of the nominal. A failure indicates the DAC (A11) assembly is probably at fault.

2815 **A11: 6.5V Reference Fault**

The DAC's 6.5V reference (REF6) is connected to the -input of the adc circuit and the DAC output (DAC SENSE CAL) is connected to the +input. The 6.5V reference is measure by adjusting the DAC until a null is achieved. This fault occurs if the 6.5V reference is over 10% of the nominal. A failure indicates the DAC (A11) assembly is probably at fault.

2816 **A11: 13V Buffered Reference Fault**

The DAC's 13V buffered reference (BRF13 and BSRF13) is connected to the -input of the adc circuit and the DAC output (DAC SENSE CAL) is connected to the +input. The 13V buffered reference is measure by adjusting the DAC until a null is achieved. This fault occurs if the 13V buffered reference is over 10% of the nominal. A failure indicates the DAC (A11) assembly is probably at fault.

2817 A11: 13V Reference Fault

The DAC's 13V reference (REF13) is connected to the -input of the adc circuit and the DAC output (DAC SENSE CAL) is connected to the +input. The 13V reference is measure by adjusting the DAC until a null is achieved. This fault occurs if the 13V reference is over 10% of the nominal. A failure indicates the DAC (A11) assembly is probably at fault.

2818 Assembly A11 Missing

At power up the instrument checks to see what assemblies are not installed. This test verifies that the DAC assembly is not responding. A failure indicates the DAC (A11) assembly is probably at fault.

2819 A11: 8255 Was Reset

The control word of the 8255 on the DAC assembly is read. A failure indicates the DAC (A11) assembly is probably at fault.

2820 A11: Fine Adjust Channel Fault

The 2nd channel of the DAC assembly is tested. The 2nd channel is set to a count which gives 0V at the DAC output. The output is measured by the adc circuit. The 2nd channel count is increased and the increase in the DAC output is verified. A failure indicates the DAC (A11) assembly is probably at fault.

3100 A14: 8255 Control Word

The diagnostics software read the control word of the 8255 IC on the High Voltage Control assembly. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3101 A14: 8255 Port A Fault

The diagnostics software writes and reads data to port A of the 8255 IC on the High Voltage Control assembly. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3102 A14: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the High Voltage Control assembly. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3103 A14: 8255 Port C Fault

The diagnostics software reads port C of the 8255 IC on the High Voltage Control assembly. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3104 A15: HV Oven Regulation Fault

The heater voltage of the High Voltage/High Current assembly HR7 hybrid is divided by 11 and is measured by the adc circuit. The heater voltage should be 0.7V ±10% ±0.2V. If it is out of tolerance, the High Voltage/High Current (A15) assembly is probably at fault.

3105 A15: HV I Oven Regulation Fault

The heater voltage of the High Voltage/High Current assembly H4 hybrid is routed to the High Voltage Control assembly via HV MUX0. The High Voltage Control connects HV MUX0 to the SDL which is routed to the DAC assembly where it is measured by the adc circuit to be 0.7V ±10% ±0.2V. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3106 A15: DC HV Amp Noise Fault

The High Voltage assemblies are configured in the dormant state with the exception that the DAC output, set to 0.0V, is connected to the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly. This circuit is configured as an amplifier with a gain of 100 whose output is connected to the RCL line. The RCL line is routed to the DAC assembly where it is measured by the adc circuit. The adc circuit takes ten readings and this failure occurs if the difference between the lowest value and highest value of the ten readings is over 0.001V. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3107 A15: DC HV Amp Offset Fault

The High Voltage assemblies are configured in the dormant state with the exception that the DAC output, set to 0.0V, is connected to the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly. This circuit is configured as an amplifier with a gain of 100 whose output is connected to the RCL line. The RCL line is routed to the DAC assembly where it is measured by the adc circuit. The adc circuit takes ten readings and this failure occurs if the average value is over 0.003V. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3108 A15: DC HV Amp Gain Fault

The High Voltage assemblies are configured in the dormant state with the exception that the DAC output, set to -0.001V, is connected to the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly. This circuit is configured as an amplifier with a gain of -100 resulting in 0.1V at the output which is connected to the RCL line. The RCL line is routed to the DAC assembly where it is measured by the adc circuit. The gain of this circuit is determined by this reading along with the previously checked offset. This failure occurs if the determined gain is over 6% of the nominal -100. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3109 A15: HV +DC Preamplifier Fault

The instrument is set to the dc 1100V range with the amplitude set to 220V, 600V, and 1100V. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.55V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3110 A15: HV +DC Series Pass & Current Fault

The instrument is set to the dc 1100V range with the amplitude set to 220V, 600V, and 1100V. HV MUX3 from the HV DC OUTPUT SERIES PASS & CURRENT LIMIT circuit on the High Voltage/High Current assembly is measured for -0.035V ±0.02V. HV MUX3 is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3111 A15: HV +DC High Voltage Output Fault

The instrument is set to the dc 1100V range with the amplitude set to 220V, 600V, and 1100V. This output voltage is divided to create MUX5 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This failure occurs if the expected output voltage is not within 12% of the nominal.

3112 A15: HV +DC Ref/Error Amplitude Fault

The instrument is set to the dc 1100V range with the amplitude set to 220V, 600V, and 1100V. The control signal AMPLITUDE from the Magnitude Control circuitry of the High Voltage Control assembly is measured. The nominal gain from AMPLITUDE to HV OUT is 135. This gain is checked by measuring AMPLITUDE to be 0.0074 of the nominal output ±25%. AMPLITUDE is divided to create MUX7 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3113 A15: HV -DC Preamplifier Fault

The instrument is set to the dc 1100V range with the amplitude set to -220V, -600V, and -1100V. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 2.3V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3114 A15: HV -DC Series Pass & Current Fault

The instrument is set to the dc 1100V range with the amplitude set to -220V, -600V, and -1100V. HV MUX3 from the HV DC OUTPUT SERIES PASS & CURRENT LIMIT circuit on the High Voltage/High Current assembly is measured for -0.035V ±0.02V. HV MUX3 is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3115 A15: HV -DC High Voltage Output Fault

The instrument is set to the dc 1100V range with the amplitude set to -220V, -600V, and -1100V. This output voltage is divided to create MUX5 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This failure occurs if the expected output voltage is not within 12% of the nominal.

3116 A15: HV -DC Reference/Error Amp Fault

The instrument is set to the dc 1100V range with the amplitude set to -220V, -600V, and -1100V. The control signal AMPLITUDE from the Magnitude Control circuitry of the High Voltage Control assembly is measured. The nominal gain from AMPLITUDE to HV OUT is 135. This gain is checked by measuring AMPLITUDE to be 0.0074 of the nominal output ±25%. AMPLITUDE is divided to create MUX7 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3117 A14/A15: HV +DC Current Error Amp Fault

The 5700A is set to the dc +2.2A current range with the amplitude set to +0.22A, +0.6A, and +1.2A. The control signal AMPLITUDE from the magnitude control circuitry of the High Voltage Control assembly is measured to be within 25% of the expected value. AMPLITUDE is divided to create MUX7 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3118 A14/A15: HV -DC Current Error Amp Fault

The 5700A is set to the dc -2.2A current range with the amplitude set to -1.2A. The control signal AMPLITUDE from the magnitude control circuitry of the High Voltage Control assembly is measured to be within 25% of the expected value. AMPLITUDE is divided to create MUX7 which is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3119 A14/A15: HV +DC Current Abs. Value

The instrument is configured to the +DC 2.2A range and set for an output of 0.22A, 0.60A, and 1.2A. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The Current control signal G OUT from the High Voltage/High Current assembly is routed to the Absolute Value Circuit on the High Voltage Control. The output from the Absolute Value circuit should be = 2.17 * I, ±25%, where "I" is the output current. This voltage is divided creating MUX6 which is connected to the SDL line where it is measured by the adc circuit on the DAC assembly.

3120 A14/A15: HV -DC Current Abs. Value

The instrument is configured to the -DC 2.2A range and set for an output of -1.2A. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The Current control signal G OUT from the High Voltage/High Current assembly is routed to the Absolute Value Circuit on the High Voltage Control. The output from the Absolute Value circuit is a positive voltage which should be = 2.17 * I, ±25%, where "I" is the output current. This voltage is divided creating MUX6 which is connected to the SDL line where it is measured by the adc circuit on the DAC assembly.

3121 Spare

This fault code is not used.

3122 A14/A15: HV AC 1KHZ, Preamp (lo)

The instrument is configured to the ac 1100V range with on amplitude of 220V @ 1 kHz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3123 A14/A15: HV AC 1KHZ, Preamp (mid)

The instrument is configured to the ac 1100V range with on amplitude of 600V @ 1 kHz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3124 A14/A15: HV AC 1KHZ, Preamp (hi)

The instrument is configured to the ac 1100V range with on amplitude of 1100V @ 1 kHz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3125 A14/A15: HV AC 100HZ, Preamp (lo)

The instrument is configured to the ac 1100V range with on amplitude of 220V @ 50 Hz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage id divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3126 A14/A15: HV AC 100HZ, Preamp Fault

The instrument is configured to the ac 1100V range with on amplitude of 600V @ 50 Hz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3127 A14/A15: HV AC 100HZ, Preamp (hi)

The instrument is configured to the ac 1100V range with on amplitude of 1100V @ 50 Hz. The output of the DC HV AMPLIFIER/AC SENSE BUFFER circuit of the High Voltage/High Current assembly is measured for 0.0V ±0.2V. This voltage is divided to create HV MUX2 which is routed to Diagnostic circuit on the High Voltage Control assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly.

3128 A14/A15: HV AC 1KHZ, Output (lo)

The instrument is configured to the ac 1100V range with on amplitude of 220V @ 1 kHz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 220V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3129 A14/A15: HV AC 1KHZ, Output (mid)

The instrument is configured to the ac 1100V range with on amplitude of 600V @ 1 kHz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 600V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3130 A14/A15: HV AC 1KHZ, Output (hi)

The instrument is configured to the ac 1100V range with on amplitude of 1100V @ 1 kHz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 1100V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3131 A14/A15: HV AC 100HZ, Output (lo)

The instrument is configured to the ac 1100V range with on amplitude of 220V @ 50 Hz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 220V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3132 A14/A15: HV AC 100HZ, Output (mid)

The instrument is configured to the ac 1100V range with on amplitude of 600V @ 50 Hz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 600V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3133 A14/A15: HV AC 100HZ, Output (hi)

The instrument is configured to the ac 1100V range with on amplitude of 1100V @ 50 Hz. The high voltage output is divided and converted to a dc voltage by the OUTPUT PEAK MEASURE circuit to create MUX5. This dc voltage is equal to the positive peaks of the ac amplitude. MUX5 is connected to the SDL line for measurement by the adc circuit on the DAC assembly. The high voltage output is measured for 1100V ±12%. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3134 Spare

This fault code is not used.

3135 Assembly A14 Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the High Voltage Control assembly is not responding. A failure indicates the High Voltage Control assembly is probably at fault.

3136 A14: 8255 Was Reset

The control word for the 8255 on the High Voltage Control assembly is read. A failure indicates the High Voltage Control (A14) assembly is probably at fault.

3137 A14/A15/A16: 2.2A AC Range Mag. Fault

The instrument is configured to the ac 2.2A range and set to 0.22A @ 1 kHz, 0.6A @ 1 kHz, 1.1A @ 1 kHz, 0.6A @ 40 Hz, and 1.1A @ 50 Hz. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The input current from the Current assembly is is measured at each setting by measuring the voltage drop across the 22 mA range shunt resistor on the Current assembly. This voltage drop is measured to be within 10% ±20 uV of the nominal. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3138 A14/A15/A16: 2.2A AC Range Compliance

The instrument is configured to the ac 2.2A range and set to 0.22A @ 1 kHz, 0.6A @ 1 kHz, 1.1A @ 1 kHz, 0.6A @ 40 Hz, and 1.1A @ 50 Hz. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The compliance voltage is determined by measuring the output side of the 22 mA range shunt resistor on the Current assembly. This is done via the Current Compliance Monitor circuit on the Current assembly and is checked to be less than 10V. A failure indicates the High Voltage/High Current assembly is probably at fault.

3139 A14/A15/A16: 2.2A AC Range Amplitude

The instrument is configured to the ac 2.2A range and set for an output current of 0.22A @ 1 kHz, 0.6A @ 1 kHz, 1.1A @ 1 kHz, 0.6A @ 40 Hz, and 1.1A @ 50 Hz. The output current from the High Voltage / High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The Current control signal G OUT from the High Voltage/High Current assembly is routed to the Magnitude Control circuit of the High Voltage Control assembly. The control signal AMPLITUDE is measured to be = I * 4.23 + 4.447, ±20%. This voltage is divided creating MUX7 which is connected to the SDL line where it is measured by the adc circuit on the DAC assembly.

3140 A14/A15/A16: 2.2A AC Range Abs. Value

The instrument is configured to the ac 2.2A range and set for an output current of 0.22A @ 1 kHz, 0.6A @ 1 kHz, 1.1A @ 1 kHz, 0.6A @ 40 Hz, and 1.1A @ 50 Hz. The output current from the High Voltage / High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The Current control signal G OUT from the High Voltage/High Current assembly is routed to the Absolute Value Circuit on the High Voltage Control. The output from the Absolute Value circuit is a positive voltage which should be = 3.07 * I, ±10%, where "I" is the output current. This voltage is divided creating MUX6 which is connected to the SDL line where it is measured by the adc circuit on the DAC assembly.

3141 A14/A15/A16: 2.2A DC Range Dummy Load

The instrument is configured to the dc 2.2A range. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The resulting voltage across this load resistor is measured by connected DUMMY LOAD on the Current assembly to the SDL line where it is measured by the adc circuit on the DAC assembly. This fault occurs if the determined current is over 10% ±5 mA of the nominal. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3142 A14/A15/A16: 2.2A DC Range Compliance

The instrument is configured to the dc 2.2A range. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The compliance voltage is determined by measuring the output side of the 22 mA range shunt resistor on the Current assembly. This is done via the Current Compliance Monitor circuit on the Current assembly and is checked to be less than 10V. A failure indicates the High Voltage/High Current assembly is probably at fault.

3143 A14/A15/A16: 2.2A DC Range Magnitude

The instrument is configured to the dc 2.2A range. The output current from the High Voltage/High Current assembly is routed to the Current assembly where it is connected to the 1.2 ohm load resistor. The output current is calculated by measuring the voltage drop across the 22 mA range shunt resistor on the Current assembly. This fault occurs if the determined current is over 10% of the nominal. A failure indicates the High Voltage/High Current (A15) assembly is probably at fault.

3300 A9: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Ohms Cal (A9) assembly. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3301 A9: 8255 Port A Fault

The diagnostics software writes and reads data to port A of the 8255 IC on the Ohms Cal (A9) assembly. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3302 A9: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the Ohms Cal (A9) assembly during the instruments dormant state. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3303 A9: 8255 Port C Fault

The diagnostics software reads port C of the 8255 IC on the Ohms Cal (A9) assembly during the instruments dormant state. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3304 A9: 10V Source Fault

The 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is set for 10V and routed to the adc circuit on the DAC assembly, via the SDL line, where it is measured for 10V ±7%. This 10V can be verified with a DMM, hi to TP13 and low to TP12. If the measured voltage is out of tolerance, the 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is faulty. If the measured voltage is within tolerance, the diagnostic circuit on the Ohms Cal (A9) assembly is probably at fault.

NOTE

If extender cards are available, verify that 10V SENSE LO is tied to SCOM. This connection is done with relays on both the Ohms assemblies.

3305 A9: 5V Source Fault

The 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is set for 5V and routed to the adc circuit on the DAC assembly, via the SDL line, where it is measured for 5V ±7%. A failure indicates the 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is probably at fault.

NOTE

> If extender cards are available verify that 10V SENSE LO is tied to SCOM. This connection is done with relays on both the Ohms assemblies.

3306 A9: 2V Source Fault

The 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is set for 2V and routed to the adc circuit on the DAC assembly, via the SDL line, where it is measured for 2V ±7%. A failure indicates the 2/5/10V SOURCE circuit on the Ohms Cal (A9) assembly is probably at fault.

NOTE

> If extender cards are available verify that 10V SENSE LO is tied to SCOM. This connection is done with relays on both the Ohms assemblies.

3307 Spare

This fault code is not used.

3308 A9: Diff Amp Offset Fault

The offset of the Differential Amplifier circuit on the Ohms Cal (A9) assembly is checked. The DAC output is set to 0V and connected to both the ±inputs of the Differential Amplifier circuit. The output is routed to the adc circuit on the DAC assembly via the RCL line. Ten reading are taken and this fault occurs of the difference between the lowest and highest value if over 1 mV or if the absolute value is over 10 mV. A failure indicates the Differential Amplifier circuit on the Ohms Cal (A9) assembly is probably at fault.

3309 A9: Diff Amp Gain Fault

The gain (nominal gain of 75) Differential Amplifier circuits on the Ohms Cal (A) assembly is checked. The DAC output is set to 86.7 mV and connected to the -input of the Diff Amp circuit with the +input connected to RCOM. The output of the Diff Amp circuit is routed to the adc circuit on the DAC assembly, via the RCL line, where it is compared to the 6.5V reference. This fault occurs if the determined gain is over 6% from the nominal 75. A failure indicates the Differential Amplifier circuit on the Ohms Cal (A9) assembly is probably at fault.

3310 A9: Diff Amp Noise Fault

The noise of the differential amplifier circuit on the Ohms Cal (A9) assembly is checked. The DAC output is set to 0V and connected to both the ±inputs of the differential amplifier circuit. The output is routed to the adc circuit on the DAC assembly via the RCL line. Ten readings are taken and this fault occurs if the difference between the lowest and highest value if over 1 mV. A failure indicates the differential amplifier circuit on the Ohms Cal (A9) assembly is probably at fault.

3311 A9/A10: Ohms 10:1 Divider Fault

The 2/5/10V SOURCE circuit is set for 10V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal (A9) assembly. The resulting 1V across the 10 kilohm portion is measure for 1V ±3% ±15 mV. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3312 A9/A10: Ohms 1:1 Divider Fault

The 2/5/10V SOURCE circuit is set for 10V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal (A9) assembly. This arrangement is measured for 10V ±3% ±15 mV. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3313 A9/A10: 10 Kilohm Diagnostic Fault

The 2/5/10V SOURCE circuit is set for 10V and connected across the 20 kilohm resistance made from the 10 kilohm in Z5 on the Ohms Cal (A9) assembly, and the 10 kilohm string on the Ohms Main (A10) assembly connected in series. The resulting 5V across the 10 kilohm string on the Ohms Main assembly is measured for 5V ±3% ±15 mV. Measure the 5V across the 10 kilohm string by connecting a DMM hi to TP2 and low to TP1 on the Ohms Cal (A9) assembly. If this voltage is greater than 5V the Ohms Main (A10) assembly is probably at fault. If the voltage is less than or equal to 5V the Ohms Cal (A9) assembly is probably at fault.

3314 A9/A10: 19 Kilohm Cal Diag Fault

The 2/5/10V SOURCE circuit is set for 10V and connected across the 29 kilohm resistance made from the 10 kilohm in Z5 on the Ohms Cal (A9) assembly, and the 19 kilohm string on the Ohms Main (A10) assembly connected in series. The resulting 6.55V across the 19k ohm string on the Ohms Main assembly is measured for 6.55V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3315 A9/A10: 10 Ohm Cal Diag Fault

The 2/5/10V SOURCE circuit is set for 2V and connected across the 100 ohm string on the Ohms Main assembly. The resulting 0.2 V across the 10 ohm portion is connected to the -input of the Differential Amplifier on the Ohms Cal assembly. The output of the DAC assembly is set to 2V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal assembly. The resulting 0.2V across the 10 kilohm portion of Z5 is connected to the +input of the Differential Amplifier. The output of the Differential Amplifier is routed to the adc circuit on the DAC assembly, via the RCL line, and measured for 0V ±3% ±15 mV. Verify that the divided DAC voltage of 0.2V ±5% is at the +input of the Diff Amp by connecting DMM hi to TP20 and low to TP10 of the Ohms Cal assembly. If this measured voltage is out of tolerance, the Ohms Cal (A9) assembly is probably at fault.

3316 A9/A10: 19 Ohm Cal Diag Fault

The 2/5/10V SOURCE circuit is set for 2V and connected across the 190 ohm string on the Ohms Main assembly. The resulting 0.2V across the 10 ohm portion is connected to the -input of the Differential Amplifier on the Ohms Cal assembly. The output of the DAC assembly is set to 2V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal assembly. The resulting 0.2V across the 10 kilohm portion of Z5 is connected to the +input of the Differential Amplifier. The output of the Differential Amplifier is routed to the adc circuit on the DAC assembly, via the RCL line, and measured for 0V ±3% ±15 mV. A failure indicates the calibration of the 19 ohm resistance on the Ohms Main (A10) assembly is probably at fault.

3317 A9/A10: 100 Kilohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 100k ohm string. The resulting 1V across the 10 kilohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3318 A9/A10: 190 Kilohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 190k ohm string. The resulting 1V across the 19 kilohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3319 A9/A10: 1M Ohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 1M ohm string. The resulting 1V across the 100 kilohm portion is measured for 1V ±3% ±15 mV. Measure the 1 volt across the 100k ohm string by connecting a DMM hi to TP14 and low to TP2 of the Ohms Cal (A9) assembly. If the voltage is out of tolerance, the Ohms Main (A10) assembly is probably at fault. If the voltage is within tolerance, the Ohms Cal (A9) assembly if probably at fault.

3320 A9/A10: 1.9M Ohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 1.9M ohm string. The resulting 1V across the 190 kilohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3321 A9/A10: 10M Ohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 10M ohm string. The resulting 1V across the 1 megohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3322 A9/A10: 19M Ohm Ratio 1

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 19M ohm string. The resulting 1V across the 1.9 megohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3323 A9/A10: 19M Ohm Ratio 2

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 19M ohm string. This 10V across the 19 megohm portion is measured for 10V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3324 A9/A10: 100M Ohm Ratio Fault

The 2/5/10V SOURCE circuit on the Ohms Cal assembly is set to 10V which is routed to the Ohms Main assembly and connected to the 10M ohm string. The resulting 1V across the 1 megohm portion is measured for 1V ±3% ±15 mV. A failure indicated the Ohms Main (A10) assembly is probably at fault.

3325 A9/A10: 10 Kilohm Check Fault

The Current (A7) assembly outputs 0.13 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 10 kilohm string. The voltage drop across the 10 kilohm string is measured for 1.3V ±3% ±15 mV. Measure this voltage drop by connecting the DMM hi to TP5 and the low to TP6 of the Ohms Cal (A9) assembly. If the voltage is out of tolerance, the Ohms Main (A10) assembly is probably at fault. If the voltage is within tolerance, the Ohms Cal (A9) assembly is probably at fault.

3326 A9/A10: 19 Kilohm Check Fault

The Current (A7) assembly outputs 0.13 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 19 kilohm string. The voltage drop across the 19 kilohms string is measured for 2.47V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3327 A9/A10: 1 Kilohm Check Fault

The Current (A7) assembly outputs 1.3 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 1 kilohm string. The voltage drop across the 1 kilohm string is measured for 1.3V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3328 A9/A10: 1.9 Kilohm Check Fault

The Current (A7) assembly outputs 1.3 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 1.9 kilohm string. The voltage drop across the 1.9 kilohm string is measured for 2.47V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3329 A9/A10: 100 Ohm Check Fault

The Current (A7) assembly outputs 13 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 100 ohm string. The voltage drop across the 100 ohm string is measured for 1.3V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3330 A9/A10: 190 Ohm Check Fault

The Current (A7) assembly outputs 13 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 190 ohm string. The voltage drop across the 190 ohm string is measured for 2.47V ±3% ±15mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3331 A9/A10: 10 Ohm Check Fault

The Current (A7) assembly outputs 130 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 10 Ohm resistance. The voltage drop across the 10 ohm resistance is measured for 1.3V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3332 A9/A10: 19 Ohm Check Fault

The Current (A7) assembly outputs 130 mA which is routed to the Ohms Main (A10) assembly, via INT OUT HI, where it is connected to the 19 ohm resistance. The voltage drop across the 19 ohm string is measured for 2.47V ±3% ±15 mV. A failure indicates the Ohms Main (A10) assembly is probably at fault.

3333 A9/A10: 1 Ohm Check Fault

The Current (A7) assembly outputs 130 mA which is routed through the Ohms Main (A10) assembly, via INT OUT HI, to the Ohms Cal (A9) assembly where it is connected to the 1 ohm resistance. The voltage drop across the 1 ohm resistance is measured for 0.13V ±3% ±15 mV. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3334 A9/A10: 1.9 Ohm Check Fault

The Current (A7) assembly outputs 13 mA which is routed through the Ohms Main (A10) assembly, via INT OUT HI, to the Ohms Cal (A9) assembly where it is connected to the 1.9 ohm resistance. The voltage drop across the 1.9 ohm resistance is measured for 24.7 mV ±3% ±15 mV. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3335 A9/A10: Ohms Short Check Fault

The Current (A7) assembly outputs 130 mA which is routed through the Ohms Main (A10) assembly, via INT OUT HI, to the Ohms Cal (A9) assembly where it is connected to the short. The voltage drop across the short is measured for 0V ±3% ±15 mV. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3336 A9/A10: 2 Wire Compensation Fault

The Current (A7) assembly outputs 10 mA which is routed through the Ohms Main (A10) assembly, via INT OUT HI, to the Ohms Cal (A9) assembly where it is connected to ACOM. This 10 mA on ACOM causes the 2 Wire Lead Drop Compensation circuit to generates -10V which is used in creating an equal current in the opposite polarity from that current in ACOM. The -10V is routed to the adc circuit on the DAC assembly via the SDL line where it is measure for -10V ±7%. This test is then repeated using -10 mA from the Current assembly with a resulting +10V from the 2 Wire Lead Drop Compensation circuit. A failure with either test indicates the 2 Wire Lead Drop Compensation circuit on the Ohms Cal (A9) assembly is probably at fault.

3337 A9/A10: Ohms Correction Factor Fault

The 13 volt reference on the DAC assembly is checked by the adc circuit on the DAC assembly. A failure indicates the DAC (A11) assembly is probably at fault.

3338 Assembly A9 Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Ohms Cal assembly is not responding. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3339 A9: 8255 Was Reset

The control word of the 8255 on the Ohms Cal assembly is read. A failure indicates the Ohms Cal (A9) assembly is probably at fault.

3340 A9/A10: 100 Ohm Cal Diag Fault

The 2/5/10V SOURCE circuit is set for 2V and connected across the 1 kilohm string on the Ohms Main assembly. The resulting 0.2V across the 100 ohm portion is connected to the -input of the differential amplifier on the Ohms Cal assembly. The output of the DAC assembly is set to 2V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal assembly. The resulting 0.2V across the 10 kilohm portion of Z5 is connected to the +input of the differential amplifier. The output of the differential amplifier is routed to the adc circuit on the DAC assembly, via the RCL line, and measured for 0V ±3% ±15 mV. A failure indicates the calibration of the 100 ohm resistance on the Ohms Main (A10) assembly is probably at fault.

3341 A9/A10: 190 Ohm Cal Diag Fault

The 2/5/10V SOURCE circuit is set for 2V and connected across the 1.9 kilohm string on the Ohms Main assembly. The resulting 0.2V across the 190 ohm portion is connected to the -input of the Differential Amplifier on the Ohms Cal assembly. The output of the DAC assembly is set to 2V and connected across the 100 kilohm resistance in Z5 on the Ohms Cal assembly. The resulting 0.2V across the 10 kilohm portion of Z5 is connected to the +input of the differential amplifier. The output of the differential amplifier is routed to the adc circuit on the DAC assembly, via the RCL line, and measured for 0V ±3% ±15 mV. A failure indicates the calibration of the 190 ohm resistance on the Ohms Main (A10) assembly is probably at fault.

3400 A12: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Oscillator Control assembly. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3401 A12: 8255 Port A

The diagnostics software writes and reads data to port A of the 8255 IC on the Oscillator Control assembly. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3402 A12: 8255 Port B

The diagnostics software reads port B of the 8255 IC on the Oscillator Control assembly during the instruments dormant state. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3403 A12: 8255 Port C

The diagnostics software reads port C of the 8255 IC on the Oscillator Control assembly during the instruments dormant state. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3404 A13: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Oscillator Output assembly. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3405 A13: 8255 Port A

The diagnostics software writes and reads data to port A of the 8255 IC on the Oscillator Output assembly. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3406 A13: 8255 Port B

The diagnostics software reads port B of the 8255 IC on the Oscillator Output assembly during the instruments dormant state. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3407 A13: 8255 Port C

The diagnostics software reads port C of the 8255 IC on the Oscillator Output assembly during the instruments dormant state. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3408 A13: Fixed Ampl. Osc Fault

Instrument set for 1V ac at 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The signal line INTERGRATOR OUT on the Oscillator Output assembly is measured via the SDL line. Each frequency range is tested at the fixed 1V amplitude. INTERGRATOR OUT is measured to be 0V ±1V at the lower three frequency ranges, ±2V at the 100 kHz range, and ±5V at the 1 MHz range. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3409 A13: Phase Lock Loop Fault

Instrument set for 1V ac at 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The signal line LOOP FILTER OUT on the Oscillator Output assembly is measured via the SDL line. Each frequency range is tested at the fixed 1V amplitude. LOOP FILTER OUT is measured to be 0V ±5V. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3410 A12/A13: 22V Amp Bias Adj Error

Instrument set for 1V and 10V at 1 kHz operation. Signal line AMP1 on the Oscillator Output assembly is measured via the SDL line. A failure indicates that AMP1 was measured to be greater than 500 mV but less than 2V. A failure indicates the Oscillator Output (A13) assembly is probably at fault. Check the zero adjustment of potentiometer R30 on the OSC SMD AMP assembly.

3411 A12/A13: 22V Amp Nonfunctional

Instrument set for 1V and 10V at 1 kHz operation. Signal line AMP1 on the Oscillator Output assembly is measured via the SDL line. A failure indicates that AMP1 was measured to be greater than 2V. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3412 A12 To A13 Interface Fault

Instrument set for 1V 1 kHz operation. Signal VREF on the Oscillator Control (A12) assembly is measured via the SDL line to be 3.16V ±100 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3413 A12/A13: 14 bit DAC Nonfunctional

Instrument set for 1V 1 kHz operation. Signal 14 BIT DAC OUT on the Oscillator Control assembly is measured via the SDL line. The 15 bit DAC circuit on the Oscillator Control assembly is set for outputs of 0V, -1.58V, and -3.16V, and is measured to be within ± 100 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3414 A12/A13: Nonlinear Control Loop 2Vrng

Instrument set for 1V 1 kHz operation. Signal ERROR INT. OUT on the Oscillator Control assembly is measured via the SDL line to be 0V ±5.0V. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3415 A12/A13: Nonlinear Control Loop 20Vrng

Instrument set for 10V 1 kHz operation. Signal ERROR INT. OUT on the Oscillator Control assembly is measured via the SDL line to be 0V ±5.0V. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3416 A12/A13: DAC 15th Bit Fault

Instrument set for 1V 1 kHz operation. Bit 14 of the 15 BIT DAC is checked. A failure indicates the Oscillator Control (A12) assembly is probably at fault. Check FET Q19.

3417 A12: DC Sensor Buffer Fault

Instrument set for 1V 1 kHz operation. The output of the DC Sense Buffer, on the Oscillator Control assembly, is measured via the RCL line. This measurement is done by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±500uV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3418 A12: Sensor Loop/Sq. Root Amp Fault

Instrument set for 2.19V 1 kHz operation. The output of the DC Sense Buffer is connected to the main ac/dc sensor on the Oscillator Control assembly. The output of the main sensor is measured via the RCL line by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±100 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3419 A12: AC Sensor Buff (2V Range)

Instrument set for 2.19V 1 kHz operation. The output of the AC Sense Buffer is connected to the main ac/dc sensor on the Oscillator Control assembly. The output of the main sensor is measured via the RCL line by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±160 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3420 A12: AC Sensor Buff (20V Range)

Instrument set for 21.9V 1 kHz operation. The output of the AC Sense Buffer is connected to the main ac/dc sensor on the Oscillator Control assembly. The output of the main sensor is measured via the RCL line by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±160 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3421 A12: AC Cal Sensor (2V Range)

Instrument set for 2.19V 1 kHz and configured as in the 2V range ac/ac calibration. The output of the ac/ac sensor on the Oscillator Control assembly is measured via the RCL line. The output of this ac/ac sensor is measured by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±100 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3422 A12: AC Cal Sensor (20V Range)

Instrument set for 21.9V 1 kHz and configured as in the 20V range ac/ac calibration. The output of the ac/ac sensor on the Oscillator Control assembly is measured via the RCL line. The output of this ac/ac sensor is measured by comparing it to the DAC assembly output voltage. The difference is measured to be 0V ±100 mV. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3423 Assembly A12 Missing

At power up the instrument checks to see what assemblies are not installed. This test confirms that the Oscillator Control assembly is not responding. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3424 Assembly A13 Missing

At power up the instrument checks to see what assemblies are not installed. This test confirms that the Oscillator Output assembly is not responding. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3425 Assembly A12 Or A13 Not Responding

Communication with both Oscillator assemblies is checked. A failure indicates that one or both assemblies are not responding.

3426 A12: 8255 Was Reset

The control word of the 8255 on the Oscillator Control assembly is read. A failure indicates the Oscillator Control (A12) assembly is probably at fault.

3427 A13: 8255 Was Reset

The control word of the 8255 on the Oscillator Output assembly is read. A failure indicates the Oscillator Output (A13) assembly is probably at fault.

3500 A16: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Power Amp assembly. A failure indicates the Power Amp (A16) assembly is probably at fault.

3501 A16: 8255 Port A

The diagnostics software writes and reads data to port A of the 8255 IC on the Power Amp assembly. A failure indicates the Power Amp (A16) assembly is probably at fault.

3502 A16: 8255 Port B

The diagnostics software reads port B of the 8255 IC on the Power Amp assembly. A failure indicates the Power Amp (A16) assembly is probably at fault.

3503 A16: 8255 Port C

The diagnostics software read port C of the 8255 IC on the Power Amp assembly. A failure indicates the Power Amp (A16) assembly is probably at fault.

3504 Spare

This fault code is not used.

3505 Spare

This fault code is not used.

3506 Spare

This fault code is not used.

3507 A16: PA Supplies Are Off

The instrument is dormant. The +PA and -PA supplies are measured by connecting MUX1 and MUX2 respectively to the SDL line where they are measured by the adc circuit on the DAC assembly. This failure occurs if the measured voltage is between 40V-80V. The test switch S201 on the Filter/PA Supply (A18) assembly appears to be in the test position.

3508 A16/A14: 220V AC Range Output Fault

The instrument is configured for operation at 22.1V @ 1 kHz, 22.1V @ 100 Hz, 100V @ 1 kHz, 100V @ 80 Hz, 100V @ 500 Hz, 219V @ 1 kHz, and 219V @ 50 Hz. The output of the Power Amplifier is routed to the High Voltage Control assembly where it is divided and converted to a dc voltage by a peak detector circuit. This dc voltage which is equal to the peaks of the ac amplitude is connected to the SDL line where it is measure by the adc circuit on the DAC assembly to be the nominal ±10%. Exit diagnostics and set the instrument for the previous configuration and using a DMM measure the ac voltage output of the Power Amplifier, COM=TP10 HI=TP6. If the voltage is out of tolerance the Power Amplifier (A16) assembly is probably at fault. If the voltage is within tolerance, the the High Voltage Control (A14) assembly is probably at fault.

3509 A16: Amplifier Loop Not Regulated

The instrument is configured into three modes of operation. The first two modes is with the instrument set to the dc 220V range. The first is with the Power Amplifier input voltage being the 6.5V reference voltage (BRF6, BSRF6) resulting in a -130V Power Amplifier output. The second is the normal 220V dc operation with the input voltage from the DAC assembly. In this mode the Power Amplifier is outputting 22.1V, 100V, 219V, and -219V. The third is the ac 220V range at 22.1V @ 1 kHz, 22.1V @ 100 Hz, 100V @ 1 kHz, 100V @ 80 Hz, 100V @ 500 Hz, 219V @ 1 kHz, and 219V @ 50 Hz. The output of the Power Amplifier input stage is measure to be less than 11V by connecting MUX0 to the SDL line where it is measured by the adc circuit on the DAC assembly. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3510 A16: 220V Amp Fault

The instrument is set to the dc 220V range with two modes of operation. The first is with the Power Amplifier input voltage being the 6.5V reference voltage (BRF6, BSRF6) resulting in a -130V Power Amplifier output. The second is the normal 220V dc operation with the input voltage from the DAC assembly. In this mode the Power Amplifier is outputting 22.1V, 100V, 219V, and -219V. In each mode the Power Amplifier output voltage is measured to be the nominal ±10% by connecting MUX3 to the SDL line where it is measured by the adc circuit on the DAC assembly. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3511 A16: Incorrect PA Input

The instrument is set to the dc 220V range with two modes of operation. The first is with the Power Amplifier input voltage being the 6.5V reference voltage (BRF6, BSRF6) resulting in a -130V Power Amplifier output. The second is the normal 220V dc operation with the input voltage from the DAC assembly. In this mode the Power Amplifier is outputting 22.1V, 100V, 219V, and -219V. The 6.5V reference input or the resulting -1.105V, -5.0V, -10.95V, and 10.95V respectively from the DAC, is measured to be the nominal ±10% by connecting MUX5 to the SDL line where it is measured by the adc circuit on the DAC assembly. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3512 Spare

This fault code is not used.

3513 Spare

This fault code is not used.

3514 Spare

This fault code is not used.

3515 Spare

This fault code is not used.

3516 Spare

This fault code is not used.

3517 Spare

This fault code is not used.

3518 Spare

This fault code is not used.

3519 Spare

This fault code is not used.

3520 A16: PA Oven Regulation Fault

The heater voltage of the Power Amp hybrid is measured by connecting MUX7 to the SDL line where it is measured by the adc circuit on the DAC assembly to ensure the hybrid is warmed up and regulating. The heater voltage is measured to be 0.7V ±10% ±0.2V. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3521 Assembly A16 Is Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Power Amplifier is not responding. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3522 Spare

This fault code is not used.

3523 Spare

This fault code is not used.

3524 A16: Power Amp Is Too Hot

The temperature of the Power Amp assembly is checked by connecting the output of the Temperature Sensor (MUX4) to the SDL line where it is measured by the adc circuit on the DAC assembly. This fault occurs if the measured voltage is over 1.7V. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3525 220V DC Initialization Fault

This fault occurs if the diagnostics software was unable to properly set the Power Amplifier assembly hardware for diagnostics testing. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3526 220V AC Initialization Fault

This fault occurs if the diagnostics software was unable to properly se the Power Amplifier assembly hardware for diagnostics testing in the AC mode. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3527 A16: Power Amp DC Cal Network Zero Fault

The instrument is dormant. The offset of the 220V DC INT. CAL NETWORK circuit on the Power Amplifier is measured by connecting its input to ACOM and the output is connected to the RCL line. RCL is routed to the +input of the adc circuit on the DAC assembly and the -input is connected to the DAC output which is adjusted until a null is achieved. This fault occurs if the DAC assembly was unable to converge. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3528 A16: Power Amp DC Cal Network Gain Fault

The instrument is dormant. The gain of the 220V INT. CAL NETWORK circuit on the Power Amplifier is measured by connecting its input to the 13V reference (BRF13, BSRF13) and the output is connected to the RCL line. RCL is routed to the +input of the adc circuit on the DAC assembly and the -input is connected to the DAC output which is adjusted until a null is achieved. This fault occurs if the nominal gain of 0.125 is over 7%. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3529 A16: Power Amp 220V Range Attenuator Fault

The Power Amplifier is configured to the dc 220V range with the input voltage being the 6.5V reference BRF6 and BSRF6. The resulting -130V at the output is connected to the input of the 220V RANGE AC ATTENUATOR circuit which has a nominal gain of -.01. The resulting +1.3V at its output is measured to be within 10% by connecting it to the RCL line and routing it to the +input of the adc circuit on the DAC assembly. The DAC output is connected to the -input and adjusted until a null is achieved. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3530 A16: 8255 Was Reset

The control word of the 8255 on the Power Amplifier is read. A failure indicates the Power Amplifier (A16) assembly is probably at fault.

3600 +17S Supply Fault

The instrument is dormant and the +17 S supply is out of tolerance. Measure the +17 S voltage on the Regulator/Guard Crossing (A17) assembly. COM = TP9, HI = TP8. The voltage should be +17.0V to +18.0V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Switch Matrix (A8) assembly is faulty.

3601 -17S Supply Fault

The instrument is dormant and the -17 S supply is out of tolerance. Measure the -17 S voltage on the Regulator/Guard Crossing (A17) assembly. COM = TP9, HI = TP12. The voltage should be -17.0V to -18.7V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Switch Matrix (A8) assembly is faulty.

3602 +15S Supply Fault

The instrument is dormant and the +15 S supply is out of tolerance. Measure the +15 S voltage on the Regulator/Guard Crossing (A17) assembly. COM = TP9, HI = TP18. The voltage should be +14.2V to +15.8V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Output (A13) assembly is faulty.

3603 -15S Supply Fault

The instrument is dormant and the -15 S supply is out of tolerance. Measure the -15 S voltage on the Regulator/Guard Crossing (A17) assembly. COM = TP9, HI = TP19. The voltage should be -14.2V to -15.8V. If the voltage is out of tolerance, the Regulator/Guard Crossing is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Output (A13) assembly is faulty.

3604 +42S Supply Fault

The instrument is dormant and the +44 S supply is out of tolerance. Measure the unregulated +44 S voltage on the Filter/PA Supply (A18) assembly. COM = TP22, HI = TP7. The voltage should be +45V to +75V. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is faulty. If the voltage is within tolerance, measure the regulated +44 S on the Regulator (A17) assembly. COM = TP9, HI = TP13. The voltage should be +42.0V to +45.6V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Output (A13) assembly is faulty.

3605 -42S Supply Fault

The instrument is dormant and the -44 S supply is out of tolerance. Measure the unregulated -44 S voltage on the Filter/PA Supply (A18) assembly. COM = TP22, HI = TP9. The voltage should be -45V to -75V. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is faulty. If the voltage is within tolerance, measure the regulated -44 S on the Regulator (A17) assembly. COM = TP9, HI = TP16. The voltage should be -42.0V to -45.6V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Output (A13) assembly is faulty.

3606 LH COM Ground Fault

The Current/Hi Res (A7) assembly connects LHCOM to the SDL line where it is measured by the adc circuit on the DAC assembly for 0V ±50 mV relative to RCOM.

3607 -5LH Supply Fault

The instrument is dormant and the -5 LH supply is out of tolerance. Measure the unregulated -5 LH voltage on the Filter/PA Supply (A18) assembly. COM = TP3, HI = TP6. The voltage should be -8V to -16V. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is faulty. If the voltage is within tolerance, measure the regulated -5 LH on the Regulator (A17) assembly. COM = TP10, HI = TP15. The voltage should be -4.7V to -5.3V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Switch Matrix (A8) assembly is faulty.

3608 +5RLH Supply Fault

The instrument is dormant and the +5 RLH supply is out of tolerance. Measure the +5 RLH voltage on the Regulator/Guard Crossing (A17) assembly. COM = TP10, HI = TP14. The voltage should be +4.9V to +5.5V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Switch Matrix (A8) assembly is faulty.

3609 +8RLH Supply Fault

The instrument is dormant and the +8RLH supply is out of tolerance. Measure the +8RLH voltage on the Regulator /Guard Crossing (A17) assembly. COM = TP10, HI = TP17. The voltage should be +10V to +20V. If the voltage is out of tolerance, replace fuse F1 on the Regulator/Guard Crossing (A17) assembly. If the voltage is within tolerance, the diagnostic circuit on the Switch Matrix (A8) assembly is faulty.

3610 +PA Supply Fault

The instrument is configured to the dc 220V range. The Power Amplifier is set for 22.1V, 219V, and -219V and the +PA supply is measured for the nominal +180V and +360V ±10% by connecting MUX1 to the SDL line which is measured by the adc circuit on the DAC assembly. In order to identify the faulty assembly the +PA supply will have to be measured. Power off the instrument and remove the Power Amplifier assembly from the chassis.

NOTE

> All of the following connections and measurements are done on the Filter/PA Supply (A18) assembly in order to verify operation of the +PA supply.

Connect DMM COM to TP203 and the high to TP201. Using a jumper, connect TP207 to TP203 and power on the instrument. The DMM should read +180V ±10%. Using another jumper connect TP205 to TP203. The DMM should read +360V ±10%. If either voltage is out of tolerance the Filter/PA Supply (A18) assembly is probably at fault. If the voltages are within tolerance, the Power Amplifier (A16) assembly is probably at fault.

3611 -PA Supply Fault

The +PA supply is set to +180V and +360V and measured at each setting to be within 10% of the nominal. Reset the instrument. Measure the logic level of TP205 and TP207 on the Filter/PA Supply (A18) assembly. TP205 should be a logic high (8V) and TP207 should be a logic low. If these logic levels are incorrect the Digital Control circuit on the Power Amplifier (A16) assembly is faulty. If these logic levels are correct measure the +PA supply on the Filter/PA Supply assembly. COM = TP203, HI = TP201. The voltage should be 180V ±10%. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is probably at fault. If the voltage is within tolerance, call up 200V via the instrument keyboard. The +PA supply should go the 360V ±10%. If the voltage is within tolerance, the diagnostic circuit on the Power Amplifier (A16) assembly is probably at fault. If the voltage is out of tolerance, check TP205 on the Filter/PA Supply assembly for a logic low before assuming the Filter/PA Supply assembly is at fault.

3612 +15OSC Supply Fault

The instrument is dormant and the +15 OSC supply is measured to be within +14.2 to +15.8V. Measure the unregulated +15 OSC voltage on the Filter/PA Supply (A18) assembly. COM = TP4, HI = TP2. The voltage should be +19V to +35V. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is faulty. If the voltage is within tolerance, measure the regulated +15 OSC on the Regulator (A17) assembly. COM = TP4, HI = TP3. The voltage should be +14.2V to +15.8V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Control (A12) assembly is faulty.

3613 -15OSC Supply Fault

The instrument is dormant and the -15 OSC supply is measured to be within -14.2 to -15.8V. Measure the unregulated -15 OSC voltage on the Filter/PA Supply (A18) assembly. COM = TP4, HI = TP5. The voltage should be -19V to -35V. If the voltage is out of tolerance, the Filter/PA Supply (A18) assembly is faulty. If the voltage is within tolerance, measure the regulated -15 OSC on the Regulator (A17) assembly. COM = TP4, HI = TP5. The voltage should be -14.2V to -15.8V. If the voltage is out of tolerance, the Regulator/Guard Crossing (A17) assembly is faulty. If the voltage is within tolerance, the diagnostic circuit on the Oscillator Control (A12) assembly is faulty.

3614 OSC COM Ground Fault

The Oscillator Control (A12) assembly connects OSC COM to the SDL line where it is measured by the adc circuit on the DAC assembly for 0V ±50 mV relative to RCOM.

3615 S COM Ground Fault

The Current/Hi Res (A7) assembly connects SCOM to the SDL line where it is measured by the adc circuit on the DAC assembly for 0V ±50 mV relative to RCOM.

3700 A21: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Rear Panel assembly. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3701 A21: 8255 Port A Fault

The diagnostics software writes and reads data to port A of the 8255 IC on the Rear Panel assembly. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3702 A21: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the Rear Panel assembly. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3703 A21: 8255 Port C Fault

The diagnostics software read port C of the 8255 IC on the Rear Panel assembly. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3704 Assembly A21 Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Rear Panel is not responding. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3705 A21: Rear Panel Data Bus Fault

The diagnostics software writes and reads from a register in the DUART on the Rear Panel assembly. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3706 Spare

This fault code is not used.

3707 Spare

This fault code is not used.

3708 A21: 8255 Was Reset

The control word of the 8255 on the Rear Panel assembly is read. A failure indicates the Rear Panel (A21) assembly is probably at fault.

3800 A8: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Switch Matrix assembly. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3801 A8: 8255 Port A Fault

The diagnostics software writes and reads to port A of the 8255 IC on the Switch Matrix assembly. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3802 A8: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the Switch Matrix assembly. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3803 A8: 8255 Port C Fault

The diagnostics software reads port C of the 8255 IC on the Switch Matrix assembly. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3804 A8: Zero Amp Lo Noise Fault

The Internal Cal Zero Amplifier circuit on the Switch Matrix assembly is tested for noise in the low gain configuration. This is done by connecting the circuit input to RCOM, by turning on Q7, and connecting the output to the RCL line where it is measured by the adc circuit on the DAC assembly. The adc circuit takes ten readings and this failure occurs if the difference between the lowest value and highest value of the ten readings is over 0.0001V. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3805 A8: Zero Amp Lo Offset

The Internal Cal Zero Amplifier circuit on the Switch Matrix assembly is tested for excessive offset in the low gain configuration. This is done by connecting the circuit input to RCOM, by turning on Q7, and connecting the output to the RCL line where it is measured by the adc circuit on the DAC assembly. The adc circuit takes ten readings and this failure occurs if the average value is over 0.035V. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3806 A8: Zero Amp Lo Gain Fault

The gain of the Internal Cal Zero Amplifier circuit in the low gain (10) configuration is tested. The circuit input is connected to the output of the DAC assembly and the circuit output is connected to the RCL line. The RCL line is connected to the +input of the adc circuit and the -input is connected to the 6.5V reference. The gain of the Internal Cal Zero Amplifier is determined by setting the DAC output to the nominal 0.65V and then adjusted it until a null is achieved. The gain is tested to be 10 ±6%. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3807 A8: Zero Amp Hi Noise Fault

The Internal Cal Zero Amplifier circuit on the Switch Matrix assembly is tested for noise in the high gain configuration. This is done by connecting the circuit input to RCOM, by turning on Q7, and connecting the output to the RCL line where it is measured by the adc circuit on the DAC assembly. The adc circuit takes ten readings and this failure occurs if the difference between the lowest value and highest value of the ten readings is over 0.0015V. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3808 A8: Zero Amp Hi Offset

The Internal Cal Zero Amplifier circuit on the Switch Matrix assembly is tested for excessive offset in the high gain configuration. This is done by connecting the circuit input to RCOM, by turning on Q7, and connecting the output to the RCL line where it is measured by the adc circuit on the DAC assembly. The adc circuit takes ten readings and this failure occurs if the average value is over 0.155V. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3809 A8: Zero Amp Hi Gain Fault

The gain of the Internal Cal Zero Amplifier circuit in the high gain (130) configuration is tested. The circuit input is connected to the output of the DAC assembly and the circuit output is connected to the RCL line. The RCL line is connected to the +input of the adc circuit and the -input is connected to the 6.5V reference. The gain of the Internal Cal Zero Amplifier is determined by setting the DAC output to the nominal 0.05V and then adjusted it until a null is achieved. The gain is tested to be 130 ±6%. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3810 A8: 2.2V Amp Noise Fault

3811 A8: Zero Amp Offset

3812 A8: 2.2V Gain Fault

3813 A8: 220mV Offset Fault

3814 A8: 220mV Divider Fault

3815 A8: 22mV Divider Fault

3816 Spare

This fault code is not used.

3817 Spare

This fault code is not used.

3818 A8: Out Lo To Sense Lo Continuity Fault

3819 A8: Relay Fault

A fault occurred while doing relay testing on the Switch Matrix assembly.

3820 Spare

This fault code is not used.

3821 Spare

This fault code is not used.

3822 Spare

This fault code is not used.

3823 Spare

This fault code is not used.

3824 A8: Oven Regulation Fault

The heater voltage of the Switch Matrix HR1 hybrid assembly is measured to ensure it is warmed up and regulating by connecting OVEN TEMP to the SDL line where it is measured by the adc circuit on the DAC assembly. OVEN TEMP is measured to be 0.7V ±10% ±0.2V. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3825 Assembly A8 Not Responding

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Switch Matrix assembly is not responding. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3826 A8: 8255 Was Reset

The control word of the 8255 on the Switch Matrix assembly is read. A failure indicates the Switch Matrix (A8) assembly is probably at fault.

3827 Assembly A8 Too Hot

3900 A5: 8255 Control Word

The diagnostics software reads the control word of the 8255 IC on the Wideband Output assembly. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3901 A5: 8255 Port A Fault

The diagnostics software writes and reads data to port A of the 8255 IC on the Wideband Output assembly. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3902 A5: 8255 Port B Fault

The diagnostics software reads port B of the 8255 IC on the Wideband Output assembly. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3903 A5: 8255 Port C Fault

The diagnostics software reads port C of the 8255 IC on the Wideband Output assembly. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3904 Optional Assemblies A5/A6 Are Missing

At power up the instrument checks to see what assemblies are not installed. This test verifies that the Wideband Output is not responding. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3905 A6: Phase Lock Loop At 10Mhz

The Wideband assemblies are configured to 3.5V @ 1.3 MHz, 1.2V @ 1.3 MHz, 2.0V @ 3.0 MHz, 1.0V @ 4.1 MHz, 3.3V @ 5.0 MHz, 2.0V @ 6.0 MHz, 2.0V @ 7.0 MHz, and 2.0V @ 7.9 MHz. The input voltage to the VCO circuit on the Wideband Oscillator assembly is resistively divided creating WB PLL DIAGNOSTICS which is routed to the Wideband Output assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This fault occurs if the input voltage to the VCO is not within 25% ±0.75V of the expected value. A failure indicates the Wideband Oscillator (A6) assembly is probably at fault.

3906 A6: Phase Lock Loop At 30Mhz

The Wideband assemblies are configured to 3.5V @ 30.0 MHz and 1.2V @ 30.0 MHz. The input voltage to the VCO circuit on the Wideband Oscillator assembly is resistively divided creating WB PLL DIAGNOSTICS which is routed to the Wideband Output assembly where it is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This fault occurs if the input voltage to the VCO is not within 25% ±0.75V of the expected value. A failure indicates the Wideband Oscillator (A6) assembly is probably at fault.

3907 A5: RMS Sensor At 10Mhz

The Wideband assemblies are configured to 3.5V @ 1.3 MHz, 1.2V @ 1.3 MHz, 2.0V @ 3.0 MHz, 1.0V @ 4.1 MHz, 3.3V @ 5.0 MHz, 2.0V @ 6.0 MHz, 2.0V @ 7.0 MHz, and 2.0V @ 7.9 MHz. SENSOR CAL which is the output from the RMS Sensor and Amplitude Control circuit on the Wideband Output assembly is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This fault occurs if RMS Sensor output is not within 15% of the expected value. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3908 A5: RMS Sensor At 30Mhz

The Wideband assemblies are configured to 3.5V @ 30.0 MHz and 1.2V @ 30.0 MHz. SENSOR CAL which is he output from the RMS Sensor and Amplitude Control circuit on the Wideband Output assembly is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This fault occurs if RMS Sensor output is not within 15% of the expected value. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3909 A5: RMS Sensor At 6.5V DC in

The 6.5V reference (BRF6, BSRF6) is connected to the input of the RMS Sensor circuit on the Wideband Output assembly. The nominal 6.5V output of the Sensor is divided and buffered before being measured via the SENSOR CAL line. SENSOR CAL is connected to the SDL line for measurement by the adc circuit on the DAC assembly. This fault occurs if the output of the Sensor is not 6.5V ±0.47V. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3910 A5/A6: Ampl. Control At 10Mhz

The Wideband assemblies are configured for a 3.5V and 1.2V output at 1.3 MHz. WB AMPLITUDE CONTROL which is the control signal to the Wideband Oscillator assembly is divided and connected to the SDL line for measurement by the adc circuit on the DAC assembly. At the 3.5V level it is checked to be 4.5V ±1.0V and at the 1.2V level it is checked for 0.0V ±0.7V. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3911 A5/A6: Ampl. Control At 30Mhz

The Wideband assemblies are configured for a 3.5V and 1.2V output at 30.0 MHz. WB AMPLITUDE CONTROL which it the control signal to the Wideband Oscillator assembly is divided and connected to the SDL line for measurement by the adc circuit on the DAC assembly. At the 3.5V level it is checked to be 4.8V ±1.0V and at the 1.2V level it is checked for 0.0V ±0.8V. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3912 A5/A6: Output Offset At 10Mhz

The Wideband assemblies are configured to 3.5V @ 1.3 MHz, 1.2V @ 1.3 MHz, 2.0V @ 3.0 MHz, 1.0V @ 4.1 MHz, 3.3V @ 5.0 MHz, 2.0V @ 6.0 MHz, 2.0V @ 7.0 MHz, and 2.0V @ 7.9 MHz. The output of the Unity Gain Amplifier circuit on the Wideband Output assembly is measured via the OUTPUT OFFSET line to ensure the dc offset is less than 20 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3913 A5/A6: Output Offset At 30Mhz

The Wideband assemblies are configured to 3.5V @ 30.0 MHz and 1.2V @ 30.0 MHz. The output of the Unity Gain Amplifier circuit on the Wideband Output assembly is measured via the OUTPUT OFFSET line to ensure the dc offset is less than 20 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3914 A5: 0DB Output Attenuation Fault

The 6.5V reference (BRF6, BSRF6) is connected to the Unity Gain Amplifier circuit on the Wideband Output assembly which drives the output through the Attenuators. The Wideband Output assembly is set for 0 dB attenuation so the 6.5V input results in a 3.25V output into 50 ohms. This 3.25V is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. The DAC assembly output is connected to the -input of the adc circuit and adjusted until a null is achieved. This determines the exact value of the Wideband output. This fault occurs if the determined Wideband output is over 6% ±1.0 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3915 A5: 10DB Output Attenuation Fault

The 6.5V reference (BRF6, BSRF6) is connected to the Unity Gain Amplifier circuit on the Wideband Output assembly which drives the output through the Attenuators. The Wideband Output assembly is set for 10 dB attenuation so the 6.5V input results in a 1.027V output into 50 ohms. This 1.027V is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. The DAC assembly output is connected to the -input of the adc circuit and adjusted until a null is achieved. This determines the exact value of the Wideband output. This fault occurs if the determined Wideband output is over 6% ±1.0 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3916 A5: 20DB Output Attenuation Fault

The 6.5V reference (BRF6, BSRF6) is connected to the Unity Gain Amplifier circuit on the Wideband Output assembly which drives the output through the Attenuators. The Wideband Output assembly is set for 20 dB attenuation so the 6.5V input results in a 0.325V output into 50 ohms. This 0.325V is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. The DAC assembly output is connected to the -input of the adc circuit and adjusted until a null is achieved. This determines the exact value of the Wideband output. This fault occurs if the determined Wideband output is over 6% ±1.0 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3917 A5: 30DB Output Attenuation Fault

The 6.5V reference (BRF6, BSRF6) is connected to the Unity Gain Amplifier circuit on the Wideband Output assembly which drives the output through the Attenuators. The Wideband Output assembly is set for 30 dB attenuation so the 6.5V input results in a 0.103V output into 50 ohms. This 0.103V is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. The DAC assembly output is connected to the -input of the adc circuit and adjusted until a null is achieved. This determines the exact value of the Wideband output. This fault occurs if the determined Wideband output is over 6% ±1.0 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3918 A5: 40DB Output Attenuation Fault

The 6.5V reference (BRF6, BSRF6) is connected to the Unity Gain Amplifier circuit on the Wideband Output assembly which drives the output through the Attenuators. The Wideband Output assembly is set for 40 dB attenuation so the 6.5V input results in a 0.032V output into 50 ohms. This 0.032V is connected to the RCL line which is routed to the +input of the adc circuit on the DAC assembly. The DAC assembly output is connected to the -input of the adc circuit and adjusted until a null is achieved. This determines the exact value of the Wideband output. This fault occurs if the determined Wideband output is over 6% ±1.0 mV. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3919 Spare

This fault code is not used.

3920 Spare

This fault code is not used.

3921 Spare

This fault code is not used.

3922 A5/A6: Wideband Initialization Fault

This fault occurs if the diagnostics software was unable to properly set the Wideband assembly hardware for diagnostics testing. A failure indicates the Wideband Output (A5) assembly is probably at fault.

3923 A5: 8255 Was Reset

The control word of the 8255 on the Wideband Output is read. A failure indicates the Wideband Output (A5) assembly is probably at fault.

Section 6
List of Replaceable Parts

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6-1. INTRODUCTION

This section contains a complete parts list for the 5700A Calibrator.

Parts list tables are ordered alphabetically assembly number, e.g., A1, following the final assembly parts lists. In the tables, both electrical and mechanical components are listed alphabetically by reference designator, e.g., R1.

The parts lists contain the following information:

- Reference designation
- Description
- Fluke part number
- Total quantity of components per assembly (QTY.)

6-2. HOW TO OBTAIN PARTS

Components may be ordered directly from John Fluke Manufacturing. Co., Inc. or an authorized representative by using the Fluke part number. In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To replace a whole module (PCA), ask a Technical Service Center representative about the Fluke module exchange program.

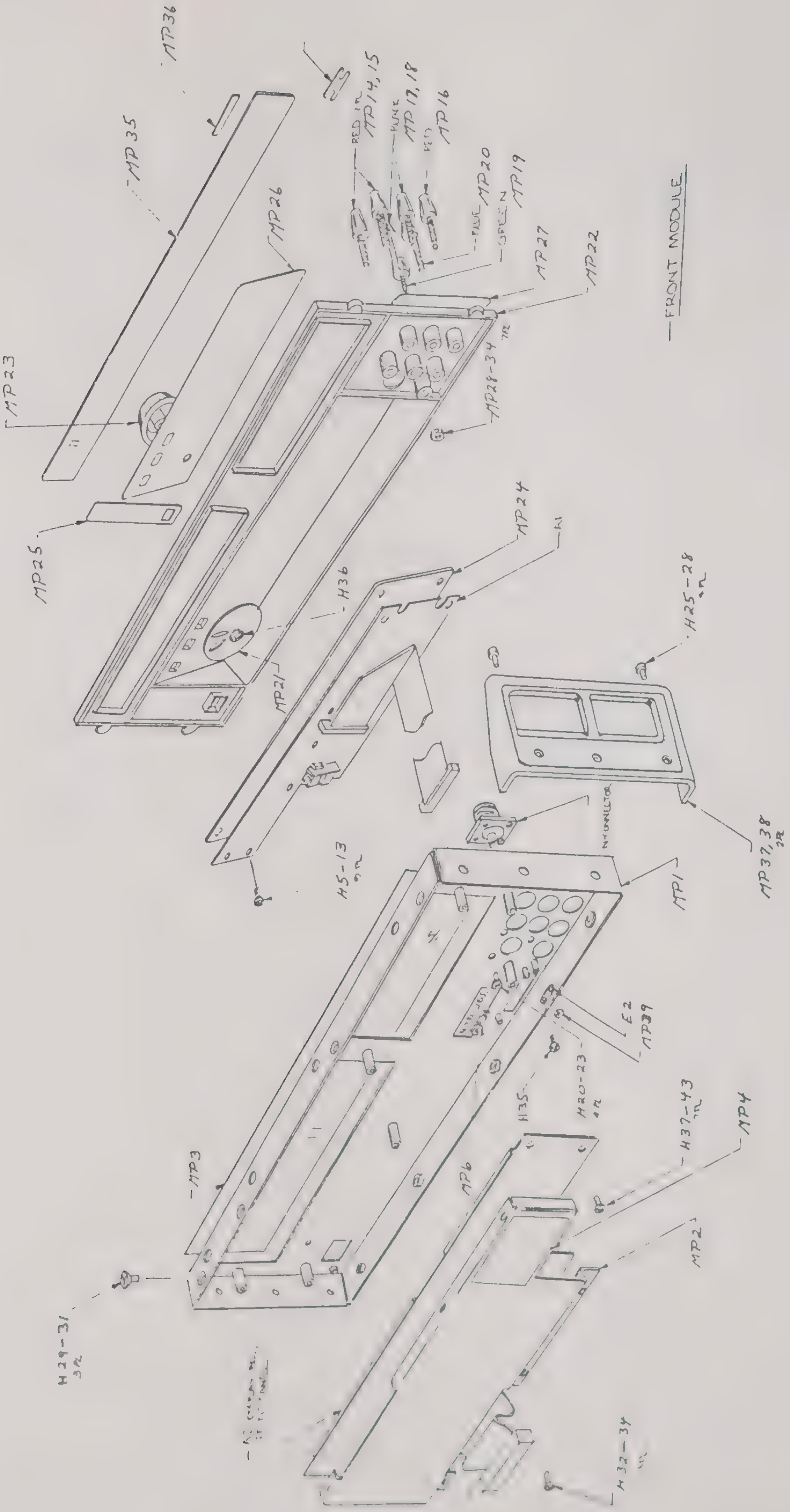
To ensure prompt and efficient handling of your order, please include the following information:

- Quantity
- Fluke part number
- Description
- Reference designator
- Printed circuit assembly (PCA) number and revision letter
- Instrument model number and serial number

Parts price information is available from the John Fluke Manufacturing Co., Inc. or its representative. Prices are also found in the Fluke Replacement Parts Catalog, which is available on request.

Table 6-1. Front Panel Final Assembly

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
CP1	ADAPTOR, COAX, SMA(M), N(M)	516963	1
E1	JUMPER, LINK, BINDING POST	190728	1
E2	TERM, RING .169 & .169, SOLDR	414292	1
H5-13	SCREW, THD FORM, PH, P, STL, 5-20,	494641	9
H20-23	SCREW, MACH, PH, P, STL, 4-40X.187	129882	4
H25-28	SCREW, MACH, CAP, SCKT, SS, 8-32X.	837575	4
H29-31	SCREW, MACH, FHU, P, SS, LOCKIN, 6-3	769893	3
H32-43	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	12
MP1	FRONT PANEL, SHEET METAL	761437	1
MP2	SHIELD, DISPLAY PWB	764514	1
MP3	LENS, SHIELD	760843	1
MP4	DECAL, FRONT OUTPUT CABLE DIAG	802967	1
MP6	GROMMET, NYLON, NAT, .056X.150X.1	285254	1
MP14-16	BINDING POST, RED PYGMY	760967	3
MP17, MP18	BINDING POST, BLACK PYGMY	760975	2
MP19	BINDING POST, GREEN PYGMY	760983	1
MP20	BINDING POST, BLUE PYGMY	760991	1
MP21	ENCODER WHEEL	764548	1
MP22	FRONT PANEL, MOLDED	775627	1
MP23	KNOB, ENCODER	786590	1
MP24	KEYPAD, ELASTOMERIC	813469	1
MP25	DECAL, POWER ON/OFF	775759	1
MP26	DECAL, KEYPAD	775346	1
MP27	DECAL, FRONT OUTPUT	775742	1
MP28-34, MP39	NUT, LOW THERMAL	760876	8
MP35	LENS, DISPLAY	775718	1
MP36	NAMEPLATE, ELECTROFORM	775528	1
MP37, MP38	HANDLE, INSTRUMENT	791897	2

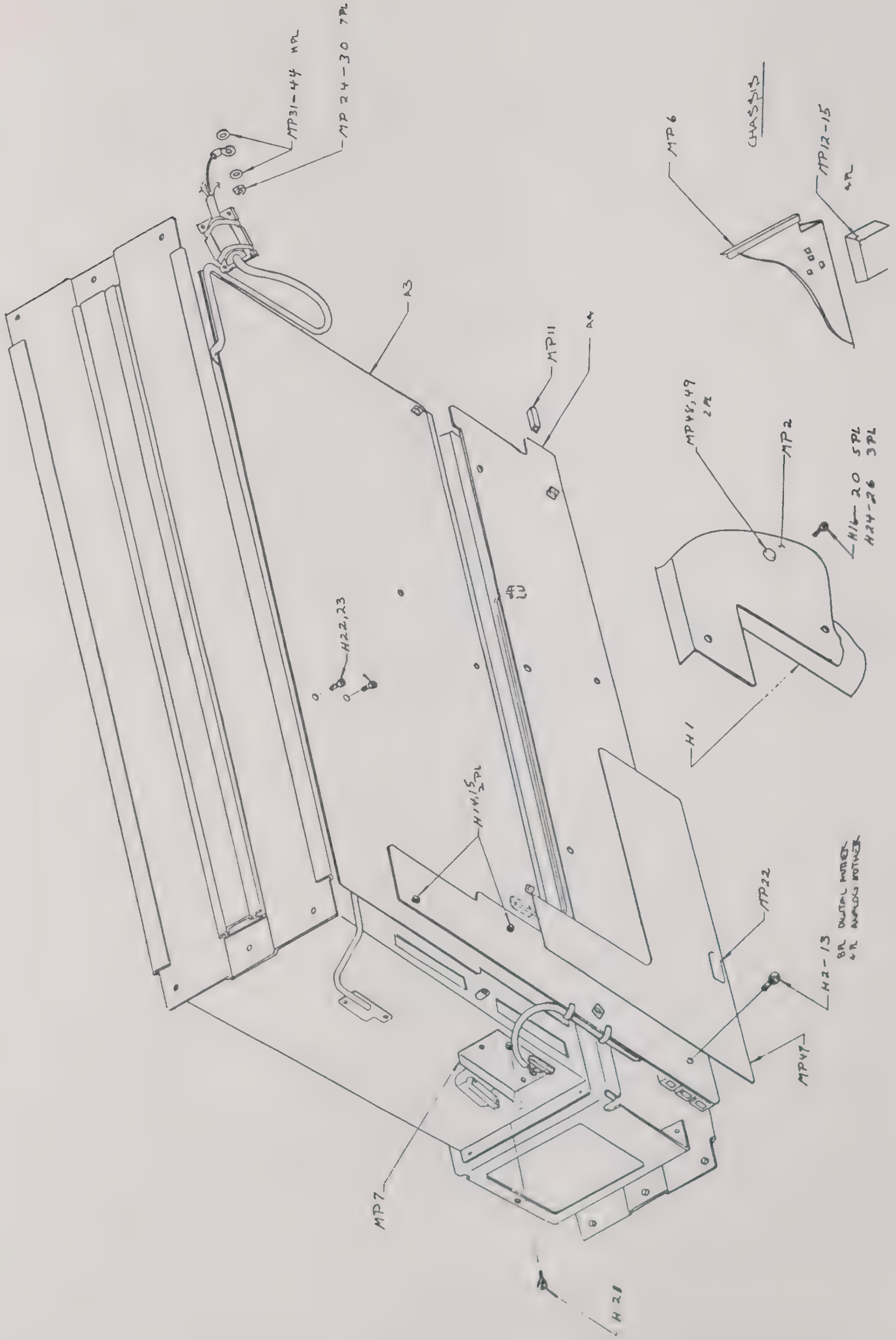


FRONT MODULE

MP36
MP35
MP26
MP23
MP25
RED IN
MP14,15
PINK
MP17,18
RED
MP16
BLUE
MP20
GREEN
MP19
MP27
MP22
MP28-34 7PL
H36
MP21
MP24
H1
H25-28 4PL
CONNECTOR
MP37,38 2PL
MP1
H5-13 9PL
E2
MP39
H35
H20-23 4PL
H37-43 7PL
MP4
MP6
MP3
MP2
H29-31 3PL
H32-34

Table 6-1a. Chassis Final Assembly

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
B1, B2	FAN/CONNECTOR ASSEMBLY	761213	2
E1	BINDING POST PART, HEAD, BRASS, 1	102889	1
H1	INSULATOR, ANALOG BOTTOM	775361	1
H2-13	SCREW, MACH, PH, P, STL, 6-32X.500	152173	12
H14-20, H84	SCREW, MACH, PH, P, STL, 6-32X.750	114223	8
H21-34	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	14
H45-56	SCREW, MACH, CAP, SCKT, SS, 8-32X.	837575	12
H57-73	SCREW, MACH, FHU, P, SS, LOCKIN, 6-3	769893	17
H74-81	SCREW, MACH, PH, P, STL, 6-32X1.250	159756	8
H82, H83	SCREW, MACH, PH, P, STL, 6-32X.375	152165	2
MP1	COVER, DIGITAL	775635	1
MP2	BOTTOM COVER, ANALOG BOX	764530	1
MP3	TOP COVER, ANALOG BOX	764522	1
MP4	RELAY BRACKET	761015	1
MP5	TOP COVER, INSTRUMENT	775817	1
MP6	BOTTOM COVER, INSTRUMENT	775825	1
MP7	SHROUD, CPU CABLE	813519	1
MP8, MP24-30	NUT, LOW THERMAL	760876	8
MP9	NUT, CAP EXT LW, STL, 6-32X.109	152819	1
MP10	CHASSIS SIDE, RIGHT	764456	1
MP11	POWER BUTTON, ON/OFF	775338	1
MP12-15	BOTTOM FOOT, MOLDED	775791	4
MP16, MP17	GASKET/CARD GUIDE	797704	2
MP18, MP19	SIDE TRIM EXTRUSION, MODIFIED	684555	2
MP20, MP21	ADHESIVE SIDE TRIM	698316	2
MP22	DECAL, CAUTION 240V	760926	1
MP23	DECAL, CAUTION 900V	760934	1
MP31-44	WASHER, LOW THERMAL	760892	14
MP45, MP46	SIDE TRIM- INSERT MODIFIED	699082	2
MP47	INSULATOR, DIGITAL MOTHERBOARD	761247	1
MP48, MP49	FOOT, ADHESIVE, RUBBER, GREY, .44X	358341	2
MP54, MP55	AIDE, PCB PULL	541730	2
MP56	ANALOG ENCLOSURE	764480	1
MP57	CARD GUIDE SUPPORT, REAR	775676	1
MP58	CARD GUIDE SUPPORT, FRONT	775767	1
MP59	DIGITAL BULKHEAD	775833	1
MP60	NUT, MACH, HEX, BR, 1/4-28	110619	1
MP61	WASHER, LOCK, INTRNL, STEEL, 0.267	110817	1
MP62	BRACKET, PWB SUPPORT DIG. MOTH	760959	1
MP63	BINDING POST, BRASS, 1/4-28	102707	1
MP64	BINDING POST PART, HEAD, BRASS, 1	102889	1
MP65-89	RIVET, POP, DOME, AL, .125X.316	807347	25
MP90-105	RIVET, POP, RND, AL, .187, .312 GRI	837849	16
MP110	TRANSFROMER/MODULE ASSEMBLY	813527	1
MP111	SHIELD, GUARD CROSSING	761353	1
MP112	CHASSIS SIDE, LEFT	764449	1
MP115-123	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	9
MP124	OSCILLATOR HEAT SINK RETAINER	775296	1
W2	AC LINE FILTER ASSY	775445	1


MP31-44 11PL
MP24-30 7PL
CHASSIS
MP6
MP12-15 4PL
A3
MP11
A4
MP45,49 2PL
MP2
H16-20 5PL
H24-26 3PL
H1
H22,23
43
H14,15 2PL
MP22
H2-13 8PL DIGITAL MOTHER 4PL ANALOG MOTHER
MP47
MP7
H21

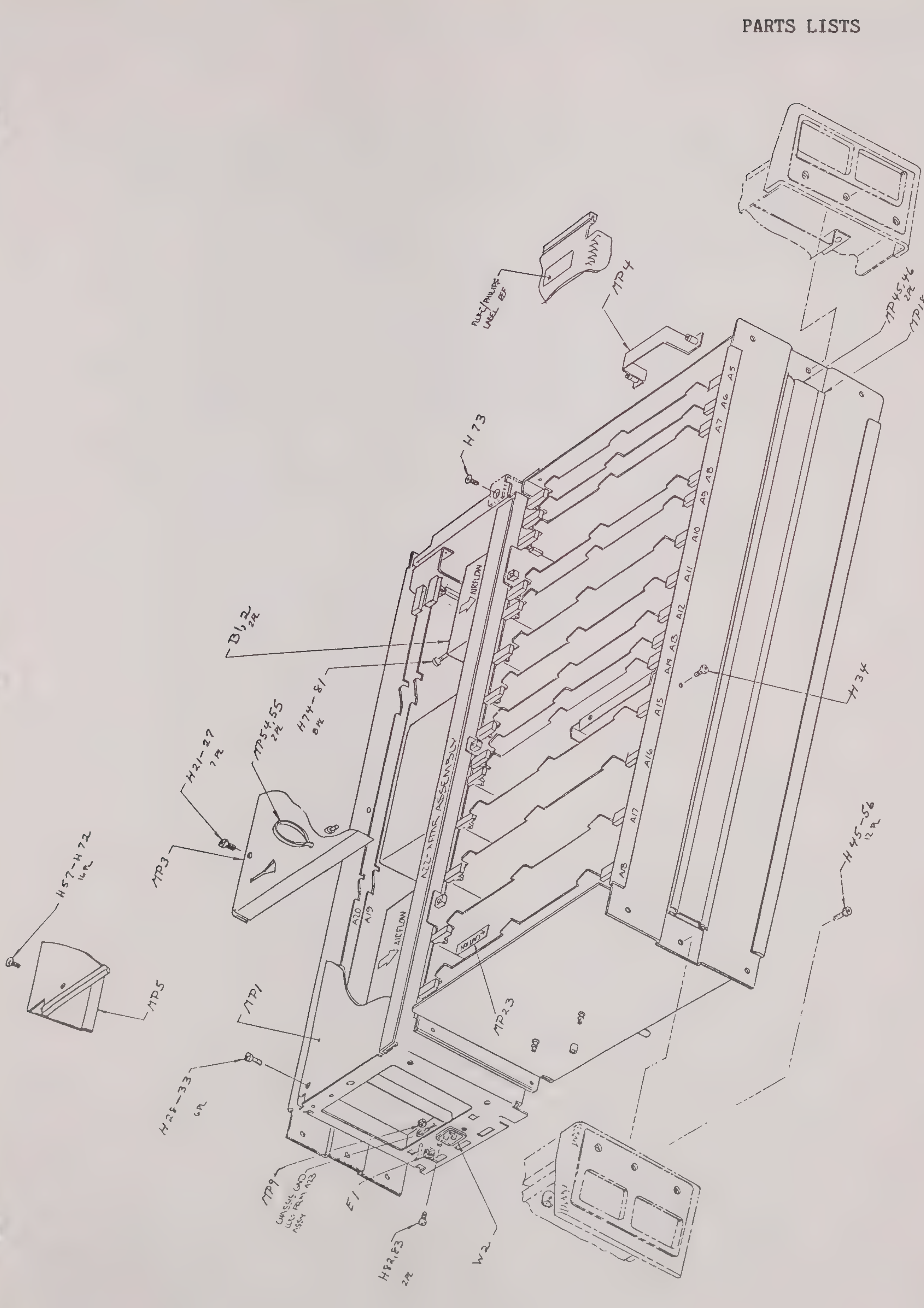
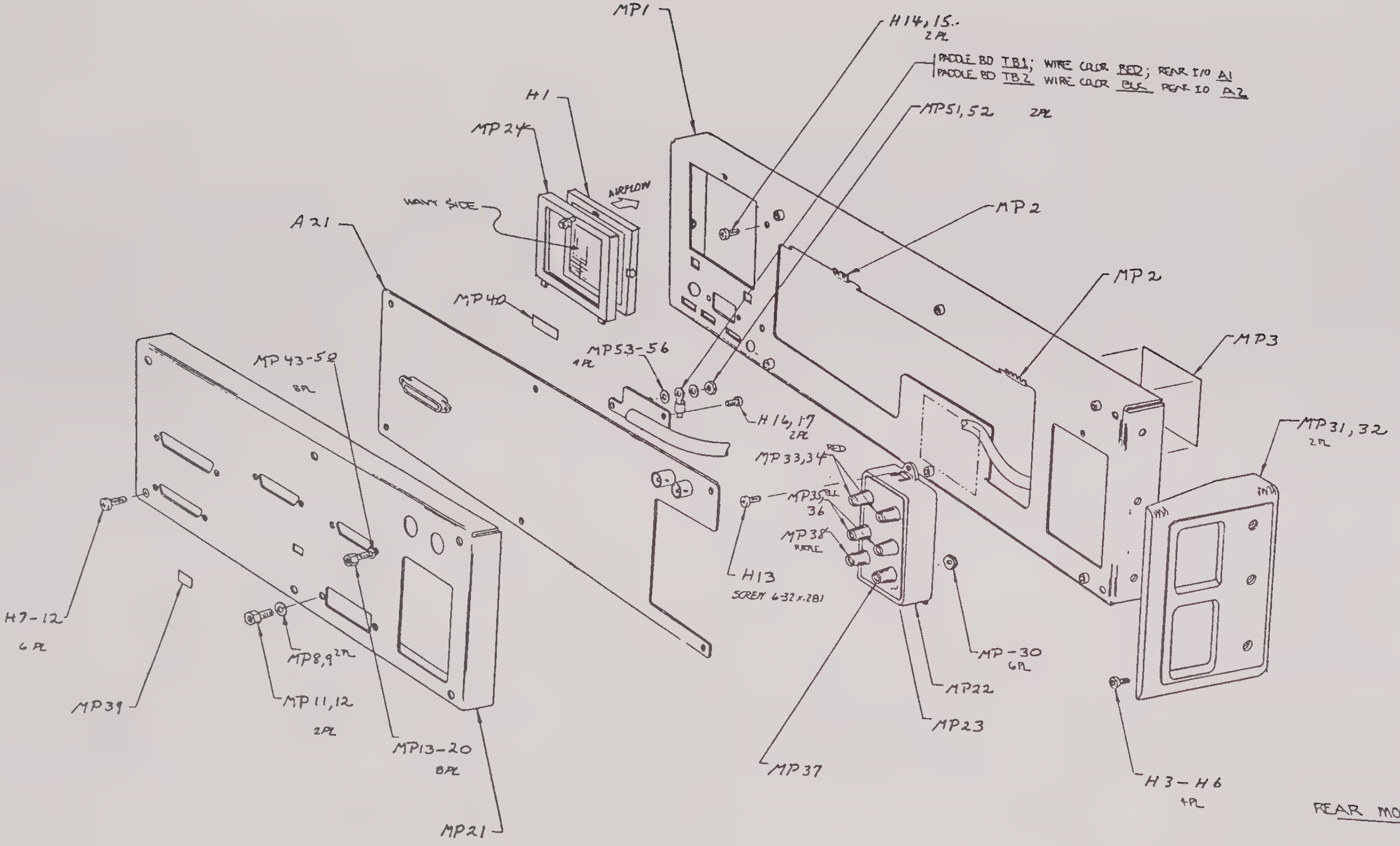

FLUKE/PHILIPS LABEL REF
MP4
MP45,46 2PL
MP18,19 2PL
MP20,21 2PL
H73
B1,2 2PL
H74-81 8PL
MP54,55 2PL
H21-27 7PL
MP3
H57-H72 16PL
MP5
MP1
A22 MTHR ASSEMBLY
AIRFLOW
AIRFLOW
A20
A19
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
H34
H45-56 12PL
CAUTION
MP23
H28-33 6PL
MP9
CHASSIS GND LUG FROM A23 ASSY
E1
H82,83 2PL
W2

Table 6-1b. Rear Panel Final Assembly

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
H1	FILTER, AIR	813493	1
H3-6	SCREW, MACH, CAP, SCKT, SS, 8-32X.	837575	4
H7-12	SCREW, MACH, PH, P, STL, 6-32X.750	114223	6
H13-17	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	5
MP1	REAR PANEL	764464	1
MP2	GROMMET, NYLON, NAT, .056X.150X.1	285254	1
MP3	DECAL, REAR OUTPUT CABLE DIAGR	802975	1
MP8, MP9	WASHER, FLAT, STEEL, #6, 0.010 THK	111005	2
MP11, MP12	CONN ACC, MICRO-RIBBON, JACK SCR	681940	2
MP13-20	CONN ACC, D-SUB, JACK SCREW, 4-40	448092	8
MP21	ALUMINUM REAR OUTPUT HOUSING	775809	1
MP22	MOLDED HOUSING, REAR OUTPUT	775783	1
MP23	DECAL, REAR OUTPUT	813576	1
MP24	FILTER FRAME	775734	1
MP25-30, MP51, MP52	NUT, LOW THERMAL	760876	8
MP31, MP32	HANDLE, INSTRUMENT	791897	2
MP33, MP34	BINDING POST, RED PYGMY	760967	2
MP35, MP36	BINDING POST, BLACK PYGMY	760975	2
MP37	BINDING POST, BLUE PYGMY	760991	1
MP38	BINDING POST, PURPLE PYGMY	761007	1
MP40	LABEL, VINYL, .3, 1.5, BAR CODE	844712	1
MP43-50	WASHER, FLAT, SS, .119X.187X.010	853296	8
MP53-56	WASHER, LOW THERMAL	760892	4


MP1
H14,15..
2 PL
PADDLE BD TB1; WIRE COLOR RED; REAR I/O A1
PADDLE BD TB2 WIRE COLOR BLK REAR IO A2
MP51,52 2PL
H1
MP24
WAVY SIDE
AIRFLOW
MP2
MP2
MP3
A21
MP40
MP53-56
4PL
H16,17
2PL
MP33,34
RED
MP35
BLU
36
MP38
PURPLE
H13
SCREW 6-32x.281
MP31,32
2PL
MP43-50
8PL
H7-12
6PL
MP39
MP8,9
2PL
MP11,12
2PL
MP13-20
8PL
MP21
MP37
MP-30
6PL
MP22
MP23
H3-H6
4PL

REAR MODULE

Table 6-2. A1 Keyboard

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
CR1-4	LED, GREEN, SUBMINIATURE, 4 MCD	822247	4
DT1, DT2	ISOLATOR, OPTO, OPTICAL SWITCH, I	523530	2
MP1	CABLE, KEYBOARD/REAR PANEL	802710	1

Table 6-3. A2 Front Panel PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1	CAP, TA, 47UF, +-20%, 10V	746990	1
C2, C4,C9-20, C28, C30, C35, C37, C39-46, C64	CAP, CER, 0.1UF, +-10%, 25V, X7R, 12	747287	27
C3, C21-27, C29, C31, C36, C38, C47-50, C66	CAP, TA, 10UF, +-20%, 25V	772491	17
C5, C33, C65	CAP, TA, 1.5UF, +-20%, 50V	780478	3
C6, C8, C32, C34, C51-54	CAP, CER, 0.01UF, +-20%, 100V, X7R,	742981	8
C7	CAP, AL, 10UF, +-20%, 100V, SOLV PR	820738	1
C55-62	CAP, CER, 0.68UF, +-20%, 100V, Z5U,	820712	8
C63	CAP, CER, 100PF, +-10%, 50V, CG, 12	740571	1
DS1	TUBE, DISPLAY, VAC FLOR, 2-ROW,	806976	1
DS2	TUBE, DISPLAY, VAC FLUOR, PATTER	832543	1
E1	CABLE, MOTHER BD TO DISPLAY	802694	1
J2	HEADER, 2 ROW, 0.100CTR, 40 PIN	807453	1
M1-10	FOOT, ADHESIVE, RUBBER, BLACK, .50	543488	10
Q1-4, Q7-10	TRANSISTOR, SI, PNP, SMALL SIGNAL	742023	8
Q5, Q6, Q11, Q12	TRANSISTOR, SI, NPN, SMALL SIGNAL	742031	4
R1, R3, R5, R6, R8, R10-12, R20, R28-30, R55-59, R61, R63, R65	RES, CHIP, CERM, 4.7K, +-5%, 0.125W	740522	22
R2, R4, R7 R9, R40, R41, R52, R53, R68	RES, CHIP, CERM, 1.1K, +-5%, 0.125W	746008	9
R13-15, R24, R25, R70, R73-75	RES, CHIP, CERM, 39K, +-5%, 0.125W,	746677	9
R16-19	RES, CHIP, CERM, 100, +-5%, 0.125W,	746297	4
R22, R26, R37-39, R42, R49-51, R54	RES, CHIP, CERM, 6.8K, +-5%, 0.125W	746024	10
R23, R27, R71	RES, CHIP, CERM, 82K, +-5%, 0.125W,	811794	3
R31-34, R43-46, R60, R62, R64, R66	RES, CHIP, CERM, 1K, +-5%, 0.125W, 1	745992	12
R35, R36	RES, CHIP, CERM, 620, +-5%, 0.125W,	745984	2
R47, R48	RES, CERM, 453, +-1%, 0.125W, 1206	801415	2
R67	RES, CHIP, CERM, 200, +-5%, 0.125W,	746339	1
R77	RES, CHIP, CERM, 91, +-5%, 0.125W, 1	756338	1
SP1	AF TRANSD, PIEZO, 24 MM	602490	1
U1, U2	IC, NMOS, 1K X 8 DUAL PORT SRAM,	806653	2
U3	IC, CMOS, 900 GATE PLD, 5700A-907	838607	1
U4	IC, CMOS, 900 GATE PLD, 5700A-907	838615	1
U5	IC, CMOS, 900 GATE PLD, 5700A-907	845375	1
U6	IC, CMOS, 14 STAGE BINARY COUNTE	831081	1
U7	IC, COMPARATOR, DUAL, HIGH SPEED,	831271	1

Table 6-3. A2 Front Panel PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U8	IC, CMOS, 12 STAGE BIN RIPPLE CN	831636	1
U9	IC, CMOS, 900 GATE PLD, 5700A-907	845383	1
U10	IC, LSTTL, OCTL D TRNSPRNT LATCH	742726	1
U11	IC, CMOS, HEX INVERTER, SOIC	742585	1
U12	IC, CMOS, DUAL D F/F, +EDG TRG, SO	782995	1
U13	IC, TTL, HEX INVERTER, W/OPEN COL	741249	1
U14-23	IC, BIMOS, DISPLAY DRIVER, 80V, PL	741231	10
U24	IC, CMOS, 600 GATE PLD, 5700A-907	837369	1
VR1, VR2	ZENER, UNCOMP, 3.9V, 10%, 64.0MA, 1	742015	2
VR3, VR4	ZENER, UNCOMP, 6.8V, 10%, 37MA, 1W,	806927	2
VR5	ZENER, UNCOMP, 6.8V, 5%, 20MA, 350M	837195	1

Table 6-4. A3 Analog Motherboard PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1	CAP, POLYES, 0.1UF, +-10%, 50V	649913	1
C2	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	1
C3	CAP, TA, 1UF, +-20%, 35V	697417	1
C4	CAP, TA, 4.7UF, +-20%, 25V	807644	2
C5	CAP, POLYES, 0.47UF, +-10%, 50V	697409	1
CR1, CR2	DIODE, SI, BV=75V, IO=150MA, 500MW	203323	2
H1, H2	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	2
H3-5	CABLE TIE, 4"L, 0.100"W, 0.75 DIA	172080	3
J8	CABLE, KEYBOARD/REAR PANEL	802710	1
J71	FIBER OPTIC, RECIEVER, 1MBD	822148	1
J72	FIBER OPTIC, TRANSMITTER, 1MBD	822155	1
J101, J111, J201, J202, J211, J212, J301, J302, J311, J312, J401, J402, J501, J502, J511, J512, J601, J602, J611, J612, J701, J702, J801, J802, J901, J902	CONN, DIN41612, TYPE C, 64 SCKT	807818	26
J811, J812, J821, J822	SOCKET, 1 ROW, PWB, .156CTR, 10 PO	851183	4
K1-3	RELAY, ARMATURE, 2 FORM C, 4.5VDC	783746	3
K4, K5, K9, K10	RELAY, REED, 1 FORM A, 5VDC	806950	4
K6-8, K11	RELAY, ARMATURE, 2 FORM C, 5V	733063	4
K12	RELAY, REED, 1 FORM B, 5VDC	845164	1
K13	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	1
MP3-54	RIVET, S-TUB, OVAL, STL, .087, .250	838482	52
MP55, MP56	SPACER, RND, STEEL, 6-32X.375	414508	2
MP57-61	INSERT.STANDOFF, BROACH, SNAP-TO	820613	5
MP101-152	CONN ACC, DIN41612, KEY	832733	52
R1	RES, CF, 75, +-5%, 0.25W	631374	1
R2	RES, CF, 91, +-5%, 0.25W	641076	1
RV1	VARISTOR, 22V, +-20%, 1.0MA	500777	1
W1	CABLE, FRONT/REAR OUTPUT	802835	1
W11	CABLE, BOOST	802744	1
XK1-3	RELAY SOCKET, 4 POLE	441964	3

Table 6-5. A4 Digital Motherboard PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C4	CAP, TA, 10UF, +-20%, 35V	816512	2
C2, C5	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	2
C3	CAP, POLYES, 0.1UF, +-10%, 50V	649913	1
CR3, CR4	DIODE, SI, 100 PIV, 1.0 AMP	742874	3
F1	FUSE, 1/4X1-1/4, SLOW, 2.5A, 250V	851931	1
H8-14	CABLE TIE, 4"L, 0.100"W, 0.75 DIA	172080	7
H19, H20	SCREW, MACH, PH, P, STL, 4-40X.187	129882	2
H21, H22	WASHER, FLAT, STEEL, 0.093X.219X	306415	2
J11	HEADER, 1 ROW, 0.156CTR, 12 PIN	831354	1
J13	HEADER, 1 ROW, 0.156 CTR, 10 PIN	446724	1
J14	HEADER, 1 ROW, 0.156CTR, 16 PIN	831370	1
J15	HEADER, 1 ROW, 0.156CTR, 14 PIN	831362	1
J16	HEADER, 1 ROW, 0.156 CTR, 8 PIN	385435	1
J21	CONN, DIN41612, TYPE C, RT ANG, 64	853437	1
J31	HEADER, 1 ROW, .156CTR, RT ANG, 5	844717	1
J41, J61, J62	CONN, DIN41612, TYPE C, 64 SCKT	807818	3
J51, J52	HEADER, 1 ROW, .100CTR, 3 PIN	837351	2
J73	FIBER OPTIC, TRANSMITTER, 1MBD	822155	1
J74	FIBER OPTIC, RECIEVER, 1MBD	822148	1
J91	HEADER, 2 ROW, .100CTR, 34 PIN	851696	1
MP1	HLDR PART, FUSE, BODY, PWB MT	602763	1
MP2	HLDR PART, FUSE, CAP, 1/4X1-1/4	460238	1
MP3-12	RIVET, S-TUB, OVAL, STL, .087, .250	838482	10
MP13, MP14	CABLE ACCESSORY, CLAMP, ADHESIVE	838300	2
MP15	CABLE, FIBER OPTIC	802769	1
MP16	BRACKET, POWER SWITCH	764621	1
MP17, MP18, MP20	SPACER, SWAGED, RND, BR, .177 ID,	837864	3
MP19	SWITCH PART, ACTUATOR	836460	1
MP21	SWITCH PART, FLEX LINKAGE, 396MM	836478	1
P81, P82	HEADER, 1 ROW, 0.156CTR, 20 PIN	831222	2
R1	RES, CF, 91, +-5%, 0.25W	641076	1
R2, R3	RES, WW, 2, +-1%, 2W	229542	2
RV1	VARISTOR, 22V, +-20%, 1.0MA	500777	1
RV2	VARISTOR, 430V, +-20%, 1.0MA	519355	1
SW1	SWITCH PART, SWITCH, DPST	831826	1
SW2-4	SWITCH, SLIDE, DPDT, LINE SELECT,	817353	3
W90	CABLE, REAR PANEL-CPU	802728	1

Table 6-6. A5 Wideband Output PCA, Option -03

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1	CAP, CER, 4.7PF, +-0.25PF, 50V, COG	721837	1
C2	CAP, CER, 22PF, +-2%, 100V, COG	512871	1
C3	CAP, POLYES, 0.047UF, +-10%, 50V	820548	1
C4, C11-13 C66	CAP, CER, 100PF, +-5%, 50V, CG	831495	5
C5	CAP, CER, 470PF, +-10%, 50V, COG	733071	1
C6, C52, C53, C79	CAP, POLYES, 0.033UF, +-10%, 50V	715276	4
C7, C10, C15, C23, C81	CAP, POLYES, 0.47UF, +-10%, 50V	697409	5
C8, C9, C25-37, C45-51, C55-63, C72-76, C80	CAP, POLYES, 0.1UF, +-10%, 50V	649913	37
C14	CAP, POLYES, 0.22UF, +-5%, 50V	747519	1
C16-18, C21, C39-44	CAP, TA, 4.7UF, +-20%, 25V	807644	10
C19, C77, C78	CAP, POLYES, 0.001UF, +-10%, 50V	720938	3
C20, C22	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C38	CAP, CER, 5.6PF, +-0.25PF, 100V, CO	512954	1
C64, C65	CAP, POLYES, 1.0UF, +-10%, 50V	733089	2
C67	CAP, CER, 33PF, +-2%, 50V, COG	715292	1
C68	CAP, CER, 39PF, +-2%, 50V, COG	714840	1
C82	CAP, AL, 47UF, +-20%, 16V, SOLV PRO	643304	1
C83	CAP, CER, 270PF, +-5%, 50V, COG	658898	1
CP1	ADAPTER, BNC(F), BANANA PLUG(M)	528802	1
CP2	ADAPTOR, COAX, BNC(M), N(F)	756775	1
CR1-4, CR7	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	5
CR5	DIODE, SI, N-JFET, CURRENT REG, IF	334714	1
CR6	DIODE, SI, BV= 75.0V, IO=150MA, 50	698720	1
E3	JUMPER, REC, 2 POS, .100CTR, .025	757294	1
H7-9	SCREW, MACH, PH, P, STL, 6-32X.500	152173	4
H10-19	SPACER, TRANSISTOR MOUNT, DAP	152207	10
J1, J2	CONN, COAX, SMB(M), PWB, RT ANG	353243	2
J3	HEADER, 1 ROW, 0.100CTR, 2 PIN	643916	1
K1, K11	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	2
K2, K3, K9, K10, K12	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	5
K4-8	RELAY, ARMATURE, 2 FORM C, 5VDC	806810	5
L1-14, L16-18	CHOKE, 6TURN	320911	17
L19	INDUCTOR, 100 UH, +/-10%, 12 MHZ,	249102	1
L20-22	INDUCTOR, 220 UH, +/-5%, 9.4 MHZ,	147835	3
L23-25	CORE, TOROID, FERRITE, .047X.138X	321182	3
M2	SHIELD, WB OUTPUT, REAR	764498	1
M3	SHIELD, WB AMP, FRONT	775643	1
M4	SHIELD, WB OUTPUT, ATTENUATOR,	775650	1
M5	SHIELD, WB OUTPUT, ATTENUATOR,	775668	1
MP1	TERMINATION, 50 OHM, N(M), N(F)	853429	1
MP2, MP3	RIVET, S-TUB, OVAL, STL, .087, .343	838458	2
MP4, MP5	EJECTOR, PWB, NYLON	494724	2
MP6	SCREW, MACH, PH, P, STL, 6-32X.250	152140	1
MP10-14	RELAY WASHER	803247	5
MP15-24	HEAT DIS, PRESS ON, TO-5	418384	10
P111	CONN, DIN41612, TYPE C, RT ANG, 64	807800	1
Q1	TRANSISTOR, SI, NPN, SMALL SIGNAL	698241	1
Q2, Q3	TRANSISTOR, SI, N-DMOS FET, TO-72	394122	2
Q4-6	TRANSISTOR, SI, NPN, HI-FREQ, SMAL	659417	3
Q7, Q8	TRANSISTOR, SI, PNP, SMALL SIG, RF	800201	2
Q9, Q10, Q14-16	TRANSISTOR, SI, NPN, RF, 120V, TO-3	806588	5
Q11-13	TRANSISTOR, SI, PNP, RF, 80V, TO-39	806596	3
Q17	TRANSISTOR, SI, N-JFET, TO-92	816314	1

Table 6-6. A5 Wideband Output PCA, Option -03 (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q18	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	1
R1	RES, MF, 866, +-1%, 0.125W, 50PPM	320390	1
R2	RES, MF, 200, +-1%, 0.125W, 100PPM	245340	1
R3	RES, MF, 412K, +-1%, 0.125W, 50PPM	714287	1
R7, R8	RES, MF, 698K, +-1%, 0.125W, 100PPM	757252	2
R9, R24, R27, R42, R102	RES, CF, 20K, +-5%, 0.25W	697110	5
R10	RES, CF, 3M, +-5%, 0.25W	746172	1
R11	RES, MF, 20.5K, +-1%, 0.125W, 100PP	655233	1
R12, R111-113	RES, CF, 2K, +-5%, 0.25W	810457	4
R13	RES, MF, 14.3K, +-1%, 0.125W, 100PP	721803	1
R14, R28, R114	RES, MF, 10K, +-1%, 0.125W, 100PPM	658914	3
R15, R38	RES, CF, 3K, +-5%, 0.25W	810366	2
R16	RES, CF, 620, +-5%, 0.25W	810408	1
R17	RES, MF, 866, +-1%, 0.125W, 50PPM	816603	1
R18	RES, MF, 200, +-1%, 0.125W, 100PPM	820282	1
R19	RES, CF, 12K, +-5%, 0.25W	757799	1
R20, R31	RES, CF, 4.7K, +-5%, 0.25W	721571	2
R21, R104	RES, MF, 10.5K, +-1%, 0.125W, 100PP	816611	2
R22, R35	RES, CF, 9.1K, +-5%, 0.25W	706663	2
R23	RES, CF, 1M, +-5%, 0.25W	649970	1
R25	RES, MF, 205K, +-1%, 0.125W, 100PPM	706234	1
R26	RES, CF, 43K, +-5%, 0.25W	821777	1
R29, R121	RES, MF, 56.2K, +-1%, 0.125W, 100PP	706242	2
R30, R103, R105, R106	RES, CF, 150K, +-5%, 0.25W	758219	4
R32, R63	RES, CF, 10K, +-5%, 0.25W	697102	2
R33	RES, CF, 22K, +-5%, 0.25W	747535	1
R34	RES, CF, 24K, +-5%, 0.25W	697599	1
R36, R40, R45, R62	RES, CF, 1K, +-5%, 0.25W	780585	4
R37	RES, MF, 210, +-1%, 0.125W, 100PPM	327999	1
R39	RES, CF, 16K, +-5%, 0.25W	714303	1
R41	RES, CF, 180K, +-5%, 0.25W	573626	1
R43, R44	RES, MF, 100, +-0.1%, 0.125W, 25PPM	357400	2
R46	RES, MF, 1.74K, +-1%, 0.125W, 100PP	344358	1
R47	RES, MF, 1K, +-1%, 0.125W, 100PPM	719468	1
R48, R49, R51, R55, R61, R65, R71, R76, R77, R84, R85, R90, R91	RES, CF, 51, +-5%, 0.25W	572990	13
R50	RES, MF, 499, +-1%, 0.125W, 100PPM	816462	1
R52	RES, MF, 150, +-1%, 0.125W, 100PPM	719674	1
R53	RES, MF, 402, +-1%, 0.125W, 100PPM	720201	1
R54	RES, MF, 576, +-1%, 0.125W, 100PPM	294843	1
R56, R57	RES, MF, 80.6, +-1%, 0.5W, 100PPM	158790	2
R58, R59	RES, MF, 75, +-1%, 0.5W, 100PPM	150870	2
R64	RES, MF, 806, +-1%, 0.6W, 50PPM	851944	1
R66	RES, MF, 49.9, +-1%, 0.125W, 100PPM	720318	1
R67, R68, R120	RES, MF, 21, +-1%, 0.125W, 100PPM	296632	3
R69, R70	RES, MF, 249, +-1%, 0.5W, 100PPM	241281	2
R72, R73	RES, MF, 1.15K, +-1%, 0.5W, 100PPM	155010	2
R74	RES, CF, 20K, +-5%, 0.25W	573444	1
R75	RES, MF, 10K, +-1%, 0.125W, 100PPM	719476	1

Table 6-6. A5 Wideband Output PCA, Option -03 (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R78, R79, R86-89	RES, MF, 12.7, +-1%, 0.125W, 100PPM	441766	6
R80-83	RES, MF, 909, +-1%, 0.5W, 100PPM	178053	4
R92-95	RES, MF, 75, +-5%, 0.125W, 100PPM	306027	4
R96-99	RES, MF, 187, +-0.1%, 0.5W, 25PPM	807750	4
R100	RES, MF, 1.37K, +-1%, 0.125W, 100PP	448241	1
R101	RES, MF, 1.43K, +-1%, 0.125W, 25PPM	447995	1
R107	RES, CF, 100, +-5%, 0.25W	810465	1
R108	RES, MF, 49.9, +-1%, 0.125W, 100PPM	820266	1
R109	RES, MF, 2.15K, +-1%, 0.125W, 50PPM	347039	1
R110	RES, MF, 1K, +-0.1%, 0.125W, 25PPM	340380	1
R115	RES, CF, 200K, +-5%, 0.25W	573634	1
R116	RES, MF, 2K, +-1%, 0.125W, 100PPM	816629	1
R117	RES, MF, 1.69K, +-1%, 0.125W, 100PP	321414	1
R118	RES, CF, 1.5K, +-5%, 0.25W	810432	1
R119	RES, MF, 8.06K, +-1%, 0.125W, 100PP	817619	1
R122	RES, MF, 4.99K, +-1%, 0.125W, 100PP	721548	1
TP1-19	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	19
U1	RMS CONVERTER TESTED 400 OHM-B	767707	1
U2, U11, U12	IC, OP AMP, DUAL, PRECISION, 8-PIN	783696	3
U3	IC, ARRAY, 5 TRANS, NPN, 3 ISO, 2 D	248906	1
U4	IC, COMPARATOR, DUAL, LO-PWR, 8 PI	478354	1
U5	IC, OP AMP, LO-OFFSET VOLTAGE, LO	605980	1
U6	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	1
U7	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U8	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U9, U10	IC, BIMOS, 4 CHNL HI-VOLT DRVR W	820514	2
VR1	ZENER, UNCOMP, 9.1V, 5%, 20.0MA, 0.	369587	1
VR2	ZENER, COMP, 6.4V, 2%, 2 PPM TC	419036	1
VR3	ZENER, UNCOMP, 16.0V, 5%, 15.5MA, 1	313221	1
VR4	ZENER, UNCOMP, 5.6V, 5%, 20MA, 0.5W	820464	1
W1	CABLE, WIDEBAND OUTPUT INTERCO	802876	1
W2	CABLE ASSY, 50 OHM, COAX, N(M), 3F	853432	1
Z1	RES, NET, THK F, 10DB/20DB ATTEN	760728	1
Z2	RES, NET, THK F, 20DB/20DB ATTEN	760769	1

Table 6-7. A6 Wideband Oscillator PCA, Option -03

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1-8, C49-51	CAP, TA, 4.7UF, +-20%, 25V	807644	11
C9, C10	CAP, CER, 2700PF, +-20%, 100V, X7R	362889	2
C11	CAP, CER, 15PF, +-20%, 50V, COG	697524	1
C12, C15, C16, C18-25, C29-33, C35-48, C52, C57, C58, C60, C61, C101, C103, C105-107, C201, C203, C205-207, C301, C303, C305-307, C401, C403, C405-407, C501, C503, C505-507	CAP, POLYES, 0.1UF, +-10%, 50V	649913	60
C13, C14	CAP, CER, 0.047UF, +-10%, 50V, X7R	572263	2
C17	CAP, POLYES, 0.22UF, +-10%, 50V	706028	1
C26-28	CAP, CER, 0.01UF, +-10%, 100V, X7R	557587	3
C34	CAP, CER, 82PF, +-2%, 100V, COG	512350	1
C53	CAP, CER, 6800PF, +-5%, 50V, COG	542894	1
C54, C55, C102, C108, C202, C208, C302, C308, C402, C408, C502, C508	CAP, POLYES, 0.001UF, +-10%, 50V	720938	12
C56, C59	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C62, C409-412	CAP, CER, 390PF, +-2%, 50V, COG	820530	5
C109-112	CAP, CER, 47PF, +-2%, 100V, CG	832295	4
C209-212	CAP, CER, 82PF, +-2%, 50V, COG	714857	4
C309-312	CAP, CER, 180PF, +-2%, 50V, COG	820522	4
C509-512	CAP, CER, 820PF, +-2%, 50V, COG	631002	4
CR1, CR2	DIODE, SILICON, VARACTOR, PIV= 28	598078	2
CR3-9, CR101, CR201, CR301, CR401, CR501	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	12
CR102, CR103, CR202, CR203, CR302, CR303, CR402, CR403, CR502, CR503	DIODE, SI, SWICHING, PIN	334227	10
E2-5	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	4
E6	JUMPER, REC, 2 POS, .100CTR, .025	757294	1
H1-5	SPACER, TRANSISTOR MOUNT, DAP	152207	5
H10	SCREW, MACH, PH, P, STL, 6-32X.750	114223	1
J1	CONN, COAX, SMB(M), PWB, RT ANG	353243	1
J6	HEADER, 1 ROW, 0.100CTR, 2 PIN	643916	1
L1-4, L7-12, L14, L15	CHOKE, 6TURN	320911	12
L5	INDUCTOR, 0.22 UH, +/-10%, 400MHZ	261735	1
L6	INDUCTOR, 1500UH, 5%	806505	1
L16, L102, L104	INDUCTOR, 1UH, 5%, SUBMINIATUR	806562	3
L101, L503	INDUCTOR, 22 UH, +/-10%, 38 MHZ, S	147843	2
L103	INDUCTOR, 1.5UH, +/-5%, 128 MHZ, S	413856	1

Table 6-7. A6 Wideband Oscillator PCA, Option -03 (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
L201	INDUCTOR, 33 UH, +/-10%, 33 MHZ, S	249086	1
L202, L204	INDUCTOR, 2.2UH, 5%, SUBMINIAT	806547	2
L203	INDUCTOR, 3.3 UH, +/-10%, 88 MHZ,	174714	1
L301	INDUCTOR, 82UH, +/-10%, 14 MHZ, SH	542290	1
L302, L304	INDUCTOR, 3.9 UH, +/-5%, 84 MHZ, S	413864	2
L303	INDUCTOR, 5.6UH, +-10%, 69MHZ, SHI	598219	1
L401	INDUCTOR, 120 UF, +/-5%, 11.2 MHZ	321042	1
L402, L404	INDUCTOR, 8.2UH, 5%, SUBMINIAT	806521	2
L403	INDUCTOR, 12 UH, +/-5%, 47 MHZ, SH	820720	1
L501	INDUCTOR, 220 UH, +/-5%, 9.4 MHZ,	147835	1
L502, L504	INDUCTOR, 15UH, 5%, SUBMINIATU	806513	2
MP1	SHIELD, WIDEBAND OSCILLATOR, F	775478	1
MP2	SHIELD, WB OSCILLATOR, REAR	775486	1
MP3, MP4	SHIELD, WIDEBAND MYLAR	802918	2
MP5	CABLE ACCESSORY, CLAMP, ADHESIVE	838300	1
MP6, MP7	RIVET, S-TUB, OVAL, STL, .087, .343	838458	2
MP8, MP9	EJECTOR, PWB, NYLON	494724	2
MP10	CABLE, 75 OHM RF	761304	1
P101	CONN, DIN41612, TYPE C, RT ANG, 64	807800	1
Q2, Q3	TRANSISTOR, SI, NPN, SMALL SIGNAL	698241	2
Q4-7	TRANSISTOR, SI, NPN, HI-FREQ, SMAL	659417	4
Q8, Q9, Q101 Q105, Q201, Q205, Q301, Q305, Q401, Q405, Q501, Q505	TRANSISTOR, SI, N-DMOS FET, TO-72	394122	12
Q102, Q202, Q302, Q402, Q502	TRANSISTOR, SI, NPN, SM SIGNAL, HI	272930	5
Q103, Q104, Q203, Q204, Q303, Q304, Q403, Q404, Q503, Q504	TRANSISTOR, SI, NPN, SMALL SIGNAL	820407	10
R3	RES, CF, 300K, +-5%, 0.25W	732818	1
R4, R5, R39 R41	RES, CF, 12K, +-5%, 0.25W	757799	4
R6, R87	RES, CF, 100, +-5%, 0.25W	810465	2
R7	RES, CF, 9.1K, +-5%, 0.25W	706663	1
R8, R25-27, R38, R52, R66, R67, R79, R80, R83	RES, CF, 1K, +-5%, 0.25W	780585	11
R9	RES, CF, 20K, +-5%, 0.25W	697110	1
R11, R12, R15-18, R21, R22	RES, CF, 51, +-5%, 0.25W	572990	8
R13, R14, R19, R20, R23, R24, R70	RES, CF, 270, +-5%, 0.25W	573071	7
R28-30, R36, R81	RES, CF, 2K, +-5%, 0.25W	810457	5
R31	RES, MF, 8.06K, +-1%, 0.125W, 100PP	817619	1
R32, R53	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	2
R33, R42, R43, R46, R50, R54, R60, R86, R103, R203, R303,	RES, MF, 49.9, +-1%, 0.125W, 100PPM	820266	13

Table 6-7. A6 Wideband Oscillator PCA, Option -03 (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R403, R503			
R34, R57	RES, MF, 30.1, +-1%, 0.125W, 100PPM	820563	2
R35, R55	RES, MF, 3.32K, +-1%, 0.125W, 100PP	817601	2
R37	RES, CF, 3.9K.+-5%, 0.25W	810416	1
R40, R48, R74-78, R102, R110, R111, R113-116, R202, R210, R211, R213-216, R302, R310, R311, R313, R402, R410, R411, R413, R502, R510, R511, R513	RES, CF, 10K, +-5%, 0.25W	697102	33
R44	RES, CF, 4.7K, +-5%, 0.25W	721571	1
R45, R47	RES, MF, 200, +-1%, 0.125W, 100PPM	820282	2
R49	RES, MF, 10K, +-1%, 0.125W, 100PPM	658914	1
R51	RES, MF, 4.99K, +-1%, 0.125W, 100PP	721548	1
R56	RES, CC, 330, +-5%, 0.5W	108936	1
R58, R112, R212, R312, R412, R512	RES, MF, 110, +-1%, 0.125W, 100PPM	820571	6
R59	RES, MF, 14.3K, +-1%, 0.125W, 100PP	721803	1
R61	RES, MF, 2.49K, +-1%, 0.125W, 100PP	810523	1
R62, R64, R65	RES, CC, 680, +-5%, 0.5W	178392	4
R63	RES, CF, 200, +-5%, 0.25W	810390	1
R68	RES, MF, 1.62K, +-1%, 0.125W, 100PP	772004	1
R71	RES, MF, 75, +-1%, 0.125W, 100PPM	820241	1
R72, R73	RES, MF, 6.65K, +-0.1%, 0.125W, 100	772558	2
R82	RES, CF, 6.2K, +-5%, 0.25W	714337	1
R84, R85	RES, CF, 240, +-5%, 0.25W	830588	2
R101, R201, R301, R401, R501	RES, CC, 220, +-5%, 0.5W	186031	5
R104, R204, R304, R404, R504	RES, MF, 249, +-1%, 0.5W, 100PPM	241281	5
R105, R205, R305, R405, R505	RES, MF, 100, +-1%, 0.125W, 100PPM	817627	5
R106, R107, R206, R207, R306, R307, R406, R407, R506, R507	RES, CF, 130, +-5%, 0.25W	817593	10
R108, R208, R308, R408, R508	RES, MF, 523, +-1%, 0.125W, 100PPM	820274	5
R109, R209, R309, R409, R509	RES, MF, 2.67K, +-1%, 0.125W, 100PP	820290	5
TP1-4, TP10-17	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	12
U1	IC, CMOS, 4-BIT PHASE LCKD LOOP	799452	1
U2	IC, OP AMP, JFET INPUT, 8 PIN DIP	472779	1
U3	IC, ECL, VOLTAGE CONTROLLED OSCI	454975	1

Table 6-7. A6 Wideband Oscillator PCA, Option -03 (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U4	IC, ECL, DUAL D M/S F/F, W/SET&RE	454959	1
U5	IC, ECL, 4-BIT BINARY COUNTER, 12	799460	1
U6	IC, ECL, 8-1 LINE MULTIPLEXER (M	799510	1
U7, U10, U11	IC, COMPARATOR, QUAD, 14 PIN DIP	387233	3
U8	IC, CMOS, BCD-DEC & BIN-OCTAL DC	473769	1
U9	IC, PBLR, MONOLITHIC, DIFF. AMP	783738	1
U12, U13	IC, ARRAY, 5 TRANS, NPN, 5 ISOLATE	380188	2
U14	IC, CMOS, QUAD INPUT NOR GATE	811158	1
U15	IC, COMPARATOR, HI-SPEED, 14 PIN	647115	1
VR1, VR4	ZENER, UNCOMP, 5.6V, 5%, 20MA, 0.5W	820464	2
VR2	ZENER, UNCOMP, 10.0V, 5%, 20.0MA, 0	820480	1
VR3	ZENER, UNCOMP, 6.8V, 5%, 20.0MA, 0.	820472	1
VR5	ZENER, UNCOMP, 6.2V, 5%, 200MA, 5W	806802	1
W1	CABLE, WIDEBAND TO FRONT PANEL	802785	1
Z1	RES, NET, SIP, 10 PIN, 9 RES, 10K, +	414003	1
Z2	RES, NET, SIP, 6 PIN, 5 RES, 10K, +-	500876	1

Table 6-8. A7 Current/High-Resolution Oscillator PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C2, C3, C18-20, C29, C32-35, C47, C48, C50, C51, C55, C56	CAP, POLYES, 0.1UF, +-10%, 50V	649913	19
C4, C68	CAP, CER, 150PF, +-2%, 100V, COG	512988	2
C5	CAP, CER, 100PF, +-2%, 100V, CG	812115	1
C6, C7, C21-24, C37, C38, C40, C43, C52, C53, C60, C61	CAP, TA, 4.7UF, +-20%, 25V	807644	14
C8	CAP, CER, 18PF, +-2%, 100V, COG	830638	1
C9	CAP, CER, 47PF, +-20%, 50V, COG	706705	1
C10	CAP, CER, 470PF, +-5%, 50V, CG	830430	1
C11	CAP, CER, 4700PF, +-20%, 100V, COG	743427	1
C12, C13	CAP, AL, 33UF, +-20%, 25V	715250	2
C14	CAP, AL, 6.8UF, +-20%, 35V, SOLV PR	643189	1
C15	CAP, TA, 2.2UF, +-20%, 16V	706804	1
C16	CAP, CER, 1000PF, +-2%, 50V, CG	807966	1
C17, C45, C46, C54	CAP, CER, 33PF, +-5%, 50V, COG	714543	4
C25, C26, C30, C36, C41, C42, C49	CAP, POLYES, 0.047UF, +-10%, 50V	820548	7
C27, C28	CAP, POLYES, 1.0UF, +-10%, 50V	733089	2
C31, C67	CAP, POLYES, 0.22UF, +-5%, 50V	747519	5
C39	CAP, TA, 22UF, +-20%, 25V	845149	1
C44	CAP, CER, 15PF, +-20%, 50V, COG	697524	1
C59	CAP, CER, 390PF, +-2%, 50V, COG	820530	1
C62	CAP, CER, 820PF, +-2%, 50V, COG	631002	1
C65, C66	CAP, CER, 82PF, +-2%, 50V, COG	714857	2
C69	CAP, CER, 47PF, +-2%, 100V, COG	812123	1
C70	CAP, AL, 47UF, +-20%, 50V, SOLV PRO	822403	1
CR3, CR4	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	4
CR9	DIODE, SILICON, VARACTOR, PIV= 28	598078	1
CR10, CR11	DIODE, SI, BV=125.0V, IO=150MA, 50	844647	2
E1, E2	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	7
H1-4	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
HR2	RN/HYBRID CURRENT HYBRID	775387	1
K1-3, K6, K7, K10-13, K16	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	10
K4, K5, K8, K9	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	4
K14, K15, K17	RELAY, ARMATURE, 2 FORM C, 5V	733063	3
L1-3, L5, L7-9	CHOKE, 6TURN	320911	7
L4	INDUCTOR, 3.9 UH, +/-5%, 84 MHZ, S	413864	1
L10	INDUCTOR, 1UH, 5%, SUBMINIATUR	806562	1
L11	INDUCTOR, 150 UH, +/-5%, 10.5 MHZ	174763	1
MP1-5	HEAT DIS, PWB MT, .75X.50X.50, TO	816587	5
MP6	MOLDED COVER, HYBRID, R-NET	775619	1
MP7, MP8	SHIELD, HIGH RES, FRONT	775684	2
MP9, MP10	SHIELD, HIGH RES, REAR	764589	2
MP11, MP12	EJECTOR, PWB, NYLON	494724	2
P211, P212	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1	TRANSISTOR, SI, BV=40V, 40W, TO-22	369660	1
Q2, Q5, Q16 Q18	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	4
Q3, Q4, Q19	TRANSISTOR, SI, PNP, T92	698233	3
Q6, Q7	TRANSISTOR, SI, BV=100V, 10W	495689	2

Table 6-8. A7 Current/High-Resolution Oscillator PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q8, Q9	TRANSISTOR, SI, BV= 80V, 10W, TO-	535468	2
Q10, Q11	TRANSISTOR, SI, BV= 55V, 40W, TO-	325753	2
Q12, Q13	TRANSISTOR, SI, BV= 45V, 30W, TO-	325761	2
Q14, Q25	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	2
Q15	TRANSISTOR, SI, NPN, SMALL SIGNAL	698241	1
Q17	TRANSISTOR, SI, VMOS, PWR, TO-237,	640516	1
Q20-23	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	4
Q24	TRANSISTOR, SI, BV=60V, 65W, T	559989	1
R3, R36	RES, CF, 4.7K, +-5%, 0.25W	721571	2
R4, R9, R94	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	3
R5, R8	RES, CF, 62K, +-5%, 0.25W	713941	2
R6, R7	RES, MF, 8.87K, +-1%, 0.125W, 100PP	658922	2
R10, R12, R29, R32	RES, MF, 8.25K, +-1%, 0.125W, 100PP	820357	4
R11, R13, R81, R82	RES, MF, 909, +-1%, 0.125W, 100PPM	820308	4
R14	RES, WW, 1.2, +-5%, 2W	248658	1
R15, R44	RES, CF, 2K, +-5%, 0.25W	810457	2
R16	RES, CF, 20K, +-5%, 0.25W	697110	1
R17, R37 R50-52	RES, CF, 16K, +-5%, 0.25W	714303	5
R18, R95	RES, CF, 1.5K, +-5%, 0.25W	810432	2
R19	RES, MF, 150, +-1%, 0.125W, 100PPM	822171	1
R20-23	RES, MF, 162, +-1%, 0.125W, 100PPM	820340	4
R24-27	RES, MF, 13, +-1%, 0.5W, 100PPM	820233	4
R28, R30, R33	RES, MF, 10K, +-1%, 0.125W, 100PPM	658914	3
R31	RES, MF, 4.12K, +-1%, 0.125W, 100PP	820381	1
R34	RES, MF, 1.91K, +-1%, 0.125W, 100PP	820365	1
R35, R66, R72, R73, R90	RES, CF, 100, +-5%, 0.25W	810465	5
R38, R54, R55, R61, R62, R65, R78, R91	RES, CF, 1K, +-5%, 0.25W	780585	8
R42	RES, CF, 100K, +-5%, 0.25W	658963	1
R43, R60, R67, R68	RES, CF, 10K, +-5%, 0.25W	697102	5
R45, R46	RES, CF, 33K, +-5%, 0.25W	733667	2
R47, R48	RES, CF, 130K, +-5%, 0.25W	747436	2
R49	RES, CF, 2.4M, +-5%, 0.25W	772566	1
R53	RES, CF, 9.1K, +-5%, 0.25W	706663	1
R56, R57	RES, CC, 470, +-10%, 1W	109710	2
R58	RES, CF, 620, +-5%, 0.25W	810408	1
R59, R63, R93	RES, CF, 3K, +-5%, 0.25W	810366	3
R64	RES, MF, 10, +-1%, 0.125W, 100PPM	820399	1
R70	RES, MF, 100, +-1%, 0.125W, 100PPM	817627	1
R71	RES, MF, 7.32K, +-1%, 0.125W, 100PP	294926	1
R74, R75	RES, CF, 47, +-5%, 0.25W	822189	2
R76, R77, R92	RES, CF, 240, +-5%, 0.25W	830588	3
R79, R80	RES, MF, 787, +-1%, 0.125W, 50PPM	289389	2
R83, R84	RES, CF, 330, +-5%, 0.25W	830596	2
R85, R86	RES, WW, 27, +-5%, 2W	844563	2
R87, R88	RES, CF, 51K+-5%, 0.25W	747550	2
R89	RES, CF, 1.5K, +-5%, 0.25W	810432	1
TP1-13, TP16-20	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	23
U2, U3	IC, OP AMP, PRECISION, LOW NOISE	782920	2
U4, U22	IC, OP AMP, JFET INPUT, 22V SUPPL	832584	2
U5, U18	IC, CMOS, QUAD BILATERAL SWITCH	586735	2
U6, U20	IC, OP AMP, DUAL, PRECISION, 8-PIN	783696	2
U7	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U8-10	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	3
U11	IC, BIMOS, 4 CHNL HI-VOLT DRVR W	820514	1

Table 6-8. A7 Current/High-Resolution Oscillator PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U12	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U13	IC, COMPARATOR, HI-SPEED, 14 PIN	647115	1
U14	IC, CMOS, DUAL D F/F, +EDG TRG, W/	741702	1
U15	IC, CMOS, QUAD INPUT NOR GATE	811158	1
U16	IC, CMOS, 4-BIT PHASE LCKD LOOP	799452	1
U17	IC, CMOS, 4-BIT PHASE LCKD LOOP	820506	1
U19	IC, ECL, VOLTAGE CONTROLLED OSCI	454975	1
U21	IC, LSTTL, DUAL D F/F, +EDG TRG, W	393124	1
VR3	ZENER, UNCOMP, 5.6V, 5%, 20MA, 0.5W	820464	1
Z1	RES, NET, THN F, 40.K(8)+-500/2	760835	1
Z2	RES, NET, SIP, 6 PIN, 5 RES, 10K, +-	500876	1
Z3	RES, NET, SIP, 8 PIN, 4 RES, 10K, +-	513309	1

Table 6-9. A8 Switch Matrix PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C3, C18	CAP, CER, 470PF, +-10%, 50V, COG	733071	3
C2, C5	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C4	CAP, CER, 0.01UF, +80-20%, 50V, Z5V	697284	1
C6-9, C12, C13, C15, C16, C21, C25-27	CAP, POLYES, 0.22UF, +-5%, 50V	747519	12
C10, C29	CAP, CER, 100PF, +-20%, 50V, CG	721605	2
C11	CAP, TA, 4.7UF, +-20%, 25V	807644	1
C14	CAP, CER, 15PF, +-2%, 100V, COG	832287	1
C17	CAP, POLYES, 1.0UF, +-10%, 50V	733089	1
C20	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	1
C22	CAP, TA, 15UF, +-20%, 20V	807610	1
C23	CAP, CER, 22PF, +-2%, 50V, COG	714832	1
CR1, CR3, CR4, CR7-9, CR12, CR13	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	8
CR2, CR10	DIODE, SI, 100 PIV, 1.0 AMP	742874	2
CR5, CR6	DIODE, SI, BV=20V, IO=150MA, 250MW	853523	2
H5-8	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
HR1	RN/HYBRID 2V DC HYBRID	775379	1
K1, K3-6, K13, K15-20, K22, K24, K25	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	15
K2, K7-12, K14, K21, K23, K26-33	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	18
L1-4	CHOKE, 6TURN	320911	4
MP1	HEAT DIS, PWB MT, .75X.50X.50, TO	816587	1
MP2	MOLDED COVER, HYBRID, R-NET	775619	1
MP3	SHIELD, HIGH RES, FRONT	775684	1
MP9, MP10	EJECTOR, PWB, NYLON	494724	2
P201, P202	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1, Q8	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	2
Q2	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	1
Q3	TRANSISTOR, SI, BV=40V, 40W, TO-22	369660	1
Q4	TRANSISTOR, SI, PNP, T92	698233	1
Q6, Q7, Q11	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	3
Q9, Q10	TRANSISTOR, SI, N-JFET, TO92	845073	2
Q12, Q13	TRANSISTOR, SI, N-JFET, HI-VOLTAG	832147	2
R1	RES, MF, 15.4K, +-1%, 0.125W, 100PP	772038	1
R2	RES, MF, 1.21K, +-1%, 0.125W, 100PP	810507	1
R3, R4, R6	RES, CF, 10K, +-5%, 0.25W	697102	3
R5, R7, R10, R19, R34	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	5
R8	RES, MF, 12.7K, +-1%, 0.125W, 25PPM	817510	1
R9, R46, R47	RES, MF, 10K, +-0.1%, 0.125W, 50PPM	733972	3
R11, R20, R35	RES, CF, 560, +-5%, 0.25W	810440	3
R12	RES, CF, 1.5, +-5%, 0.25W	732800	1
R13	RES, CF, 330, +-5%, 0.25W	830596	1
R14, R48	RES, CF, 4.7K, +-5%, 0.25W	721571	2
R15-17, R21	RES, CF, 100K, +-5%, 0.25W	658963	4
R18, R33, R44	RES, MF, 20K, +-0.1%, 0.25W, 25PPM	810564	3
R22, R23, R39, R40	RES, CF, 100, +-5%, 0.25W	810465	4

Table 6-9. A8 Switch Matrix PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R24	RES, MF, 806, +-1%. 0.125W, 100PM	810531	1
R25, R26	RES, CF, 9.1K, +-5%, 0.25W	706663	2
R27, R28	RES, CF, 620, +-5%, 0.25W	810408	2
R29, R30, R37	RES, MF, 14.3, +-1%, 0.125W, 100PPM	831396	3
R31, R32, R36	RES, MF, 10, +-1%, 0.125W, 100PPM	820399	3
R38	RES, MF, 60.4, +-1%, 0.125W, 100PPM	831404	1
R41, R42	RES, CF, 20, +-5%, 0.25W	810382	2
R43	RES, MF, 150, +-1%, 0.125W, 100PPM	822171	1
T1	MV COMMON MODE CHOKE	802751	1
TP1-10	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	10
U1	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U2	IC, CMOS, BCD-DEC & BIN-OCTAL DC	473769	1
U3	IC, BPLR, FAHRENHEIT TEMPERTURE	845156	1
U4	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U5-13	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	9
U15	IC, COMPARATOR, DUAL, LO-PWR, 8 PI	478354	1
U17	IC, OP AMP, GEN PURPOSE, COMPEMSA	402750	1
U19	IC, ARRAY, 5 TRANS, 5 ISO: 2-PNP,	418954	1
U20	IC, OP AMP, PRECISION, LOW NOISE	782920	1
U21	IC, OP AMP, LO-OFFSET VOLTAGE, LO	605980	1
VR1, VR2	ZENER, UNCOMP, 6.8V, 5%, 20.0MA, 0.	820431	2
Z2	RNET, 8840A OUTPUT DIVIDER	655811	1
Z3, Z4	RES, NET, SIP, 6 PIN, 5 RES, 330, +-	408302	2
Z5	RES, NET, SIP, 8 PIN, 4 RES, 10K, +-	513309	1
Z6	RES, NET, SIP, 6 PIN, 5 RES, 1K, +-2	408310	1

Table 6-10. A9 Ohms Cal PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C28, C29, C55	CAP, POLYES, 0.1UF, +-10%, 50V	649913	4
C2	CAP, CER, 100PF, +-20%, 50V, CG	721605	1
C3, C32, C35	CAP, CER, 1000PF, +-20%, 100V, X7R	816181	3
C4, C5, C8, C10, C14, C15, C31, C37-43, C45	CAP, POLYES, 0.22UF, +-5%, 50V	747519	15
C7, C9, C22, C23	CAP, TA, 2.2UF, +-10%, 35V	697433	4
C12, C13	CAP, CER, 220PF, +-20%, 50V, COG	740654	2
C18, C33	CAP, TA, 4.7UF, +-20%, 25V	807644	2
C19, C24, C25	CAP, TA, 10UF, +-20%, 35V	816512	3
C20, C52	CAP, CER, 0.22UF, +80-20%, 50V, Z5U	649939	2
C21	CAP, CER, 2700PF, +-5%, 50V, CG	832303	1
C26, C27	CAP, CER, 1800PF, +-5%, 50V, CG	832717	2
C30	CAP, POLYPR, 0.1UF, +-10%, 160V	446781	1
C34, C51	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C36	CAP, TA, 47UF, +-20%, 10V	733246	1
C48	CAP, POLYPR, 0.47UF, +-10%, 160V	446807	1
C53, C54	CAP, POLYES, 1.0UF, +-10%, 50V	733089	2
CR1-12	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	12
H1-4	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H5	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	1
K1-5, K10, K11, K13, K15-18, K20, K22-27, K31	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	20
K6-9, K12, K14, K19, K21, K28-30	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	11
L2-8	CHOKE, 6TURN	320911	7
M1	SHIELD, ANALOG REAR	797803	1
M4	SHIELD, OHMS CAL	775312	1
MP1, MP2	EJECTOR, PWB, NYLON	494724	2
P311, P312	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	1
Q2-4	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	3
Q5	TRANSISTOR, SI, PNP, T92	698233	1
Q6	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	1
R9, R10, R43, R44	RES, CF, 47, +-5%, 0.25W	822189	4
R11	RES, CC, 330, +-5%, 1W	163394	1
R12, R23	RES, CF, 100K, +-5%, 0.25W	658963	2
R13, R26, R46	RES, CF, 100, +-5%, 0.25W	810465	3
R14, R15	RES, CF, 24, +-5%, 0.25W	817528	2
R16, R17	RES, MF, 10K, +-0.1%, 0.125W, 100PP	658955	2
R18	RES, MF, 76K, +-0.1%, 0.125W, 50PPM	851332	1
R24, R31	RES, CF, 22K, +-5%, 0.25W	747535	2
R25	RES, CC, 150, +-5%, 1W	178566	1
R27	RES, MF, 10K, +-1%, 0.125W, 100PPM	658914	1
R29, R30	RES, CF, 200, +-5%, 0.25W	810390	2
R32, R35, R39, R45	RES, CF, 1K, +-5%, 0.25W	780585	4
R33	RES, CF, 16K, +-5%, 0.25W	714303	1
R41	RESISTOR SET, 1.0 OHM 0.05% 3PP	824193	1
R42	RESISTOR SET, 1.9 OHM 0.05% 3PP	824201	1
R80	RES, CF, 10K, +-5%, 0.25W	697102	1
T1	TRANSFORMER, OHMS 2W COMP	802652	1
TP1, TP2, TP5-20	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	18
U1, U3	IC, OP AMP, LO-OFFSET VOLTAGE, LO	605980	2

Table 6-10. A9 Ohms Cal PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U2, U4	IC, OP AMP, PRECISION, LOW NOISE	782920	2
U5	IC, OP AMP, GEN PURPOSE, COMPEMSA	402750	1
U6	IC, BIPOLAR, REG PULSE WIDTH MOD	811935	1
U7	IC, OP AMP, CHOPPER STABLIZED, LO	810952	1
U8, U9	IC, OP AMP, LO-NOISE, 8 PIN DIP	495051	2
U10	IC, OP AMP, DUAL, PRECISION, MATCH	811851	1
U11	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U12	IC, CMOS, BCD-DEC & BINRY-OCTAL	650689	1
U13	IC, CMOS, 3-8 LINE DCDR W/ENABLE	773036	1
U14-20	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	7
U21	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U22	IC, CMOS, HEX INVERTER, UNBUFFERE	741199	1
VR1-3	ZENER, UNCOMP, 8.2V, 5%, 20MA, 0.4W	810309	3
Z1	RES NET THK FILM TESTED	813659	1
Z2	RES NET THK FILM TESTED	809368	1
Z3	RES, NET, SIP, 10 PIN, 5 RES, 10K, +	529990	1
Z4	RES, NET, SIP, 6 PIN, 5 RES, 1K, +-2	408310	1
Z5	RES NET THN F SUBST TRIMMED TE	828145	1

Table 6-11. A10 Ohms Main PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C2, C7, C10-13, C16	CAP, POLYES, 0.22UF, +-5%, 50V	747519	8
C3, C4	CAP, TA, 10UF, +-20%, 35V	816512	2
C5	CAP, CER, 270PF, +-5%, 50V, COG	658898	1
C6	CAP, TA, 4.7UF, +-20%, 25V	807644	1
H3-6	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
K1-4, K7, K9, K10 K13-17, K28-30, K33-37	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	20
K5	RELAY, REED, 1 FORM A, 5VDC	806950	1
K6, K8, K11, K12	RELAY, REED, 1 FORM A, 4.5VDC	544031	4
K18-27, K31, K32, K39	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	13
K38	RELAY, ARMATURE, 2 FORM C, 5V	733063	1
L4, L5	CHOKE, 6TURN	320911	2
MP1, MP2	SPACER, SWAGED, RND, BRASS, 6-32X	266486	2
MP3, MP4	EJECTOR, PWB, NYLON	494724	2
P301, P302	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
R1	RES, CERM, 90M, +- 0.05%, 0.75W, 10	783654	1
R2, R3	RES, CF, 270, +-5%, 0.25W	810424	2
R5	RES, CF, 100, +-5%, 0.25W	810465	1
R6	RES, MF, 287K, +-1%, 0.125W, 100PPM	851899	1
TP1-5	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	5
U1	IC, OP AMP, JFET INPUT, LOW NOISE	807933	1
U2, U3, U5-8, U11-13	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	9
U9	IC, CMOS, BCD-DEC & BINRY-OCTAL	650689	1
U10	IC, CMOS, 3-8 LINE DCDR W/ENABLE	773036	1
VR1	ZENER, UNCOMP, 3.3V, 5%, 20.0MA, 0.	820423	1
Z1	RES NET THN F TESTED	798330	1
Z2	RES, NET, THN F, 10.MEG, (7)+-250	759753	1
Z3	RES, NET, THN F,	759803	1

Table 6-12. A11 DAC PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C2, C4-8, C10, C11, C13-18, C21, C23-26, C41, C42, C46-49, C53-56, C58, C62, C64, C65, C76, C77, C81, C86-88, C91, C92, C96, C97, C100, C104-109	CAP, CER, 0.22UF, +80-20%, 50V, Y5V	740597	51
C9, C12	CAP, AL, 10UF, +-20%, 63V, SOLV PRO	816843	2
C19, C20	CAP, TA, 2.2UF, +-10%, 35V	697433	2
C27, C28	CAP, CER, 15PF, +-20%, 50V, COG	697524	2
C29	CAP, CER, 220PF, +-2%, 100V, COG	816728	1
C32	CAP, CER, 0.1UF, +-10%, 25V, X7R, 12	747287	1
C40, C80	CAP, CER, 47PF, +-10%, 50V, COG, 120	747352	2
C43	CAP, CER, 0.01UF, +-10%, 50V, X7R, 1	747261	1
C44, C60, C63, C94, C102	CAP, CER, 1000PF, +-10%, 50V, CG, 1	747378	5
C45, C84, C89, C95,	CAP, POLYPR, 0.1UF, +-10%, 160V	446781	4
C52, C101, C103	CAP, CER, 33PF, +-10%, 50V, COG, 120	769240	3
C57, C85	CAP, CER, 22PF, +-5%, 50V, COG	714550	2
C59, C66, C67	CAP, CER, 100PF, +-10%, 50V, CG, 12	740571	3
C78	CAP, POLYES, 0.47UF, +-10%, 50V	697409	1
C79	CAP, CER, 10PF, +-10%, 100V, CG, 12	806943	1
C90	CAP, POLYPR, 0.033UF, +-10%, 63V	721050	1
C93	CAP, CER, 330PF, +-5%, 50V, COG	697441	1
C110, C111	CAP, POLYES, 0.22UF, +-10%, 50V	706028	2
CR1, CR3-6, CR8, CR12, CR13	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	8
CR2	DIODE, SI, N-JFET, CURRENT REG, IF	741512	1
CR7	DIODE, SI, N-JFET, CURRENT REG, IF	832105	1
CR9, CR10	DIODE, SI, BV=75V, IO=250MA, SOT23	830489	2
H1	SCREW, MACH, PH, P, STL, 6-32X.500	152173	1
H9-12	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H21	SCREW, MACH, PH, P, STL, 4-40X.187	129882	1
H26	NUT, MACH, HEX, STL, 4-40	184044	1
H28	TERM, RING 5/64 & .144, SOLDR	101055	1
H32	SHIELD, DAC, FRONT	797761	1
HR5	REF. HYBRID ASSY	761338	1
HR6	DC AMP HYBRID ASSY	761411	1
K1, K2, K4	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	3
K3, K5-8	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	5
L1-7, L10	CHOKE, 6TURN	320911	8
M2	SHIELD, DAC-ADC AMP	775353	1
M3	SHIELD, DAC, REAR	761429	1
MP1	MOLDED COVER, HYBRID, R-NET	775619	1
MP5, MP6	EJECTOR, PWB, NYLON	494724	2
MP7-9	HEAT DIS, PWB MT, .75X.50X.50, TO	816587	3
MP10	HEAT DIS, VERT, 0.75X.52X.50, T	811760	1
MP11	SHIELD, DAC, FRONT, SMALL	797720	1
MP31	MOLDED COVER, REF. HYBRID	797746	1
P401, P402	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1, Q9	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	2
Q2, Q3	TRANSISTOR, SI, BV=40V, 40W, TO-22	369660	2

Table 6-12. A11 DAC PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q4-7, Q11, Q22, Q25, Q26	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	8
Q8	TRANSISTOR, SI, PNP, SMALL SIGNAL	288761	1
Q10, Q19, Q56	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	3
Q12, Q13, Q16, Q17, Q23, Q24	TRANSISTOR, SI, N-JFET, HI-VOLTAG	832147	6
Q14, Q15, Q18, Q20, Q21, Q52, Q53	TRANSISTOR, SI, N-CHAN, TO-92, SWI	832139	7
Q30, Q32	TRANSISTOR, SI, N-JFET, SOT23	844584	2
Q31, Q33, Q35	TRANSISTOR, SI, NPN, SMALL SIGNAL	806463	3
Q34	TRANSISTOR, SI, PNP, SMALL SIGNAL	742684	1
Q57	TRANSISTOR, SI, PNP, T92	698233	1
R1, R28, R33, R39, R44, R83, R84	RES, CHIP, CERM, 4.7K, +-5%, 0.125W	740522	7
R2	RES, CF, 3K, +-5%, 0.25W	810366	1
R3	RES, CF, 2K, +-5%, 0.25W	573238	1
R6	RES, CHIP, CERM, 620, +-5%, 0.125W,	745984	1
R7, R9, R16	RES, CHIP, CERM, 750, +-5%, 0.125W,	746404	3
R10	RES, MF, 2.49K, +-1%, 0.125W, 100PP	810523	1
R12	RES, CHIP, CERM, 200, +-5%, 0.125W,	746339	1
R13	RES, CHIP, CERM, 22, +-5%, 0.125W, 1	746230	1
R14	RES, MF, 61.9M, +-1%, 0.25W, 150PPM	851741	1
R15	RES, MF, 1.21K, +-1%, 0.125W, 100PP	810507	1
R19-21, R29, R31, R41, R48, R115, R116	RES, CHIP, CERM, 10K, +-5%, 0.125W,	746610	9
R22, R124, R125	RES, CF, 20K, +-5%, 0.25W	697110	3
R23, R32	RES, CHIP, CERM, 10, +-5%, 0.125W, 1	746214	2
R24	RES, CERM, 2.49K, +-1%, 0.125W, 120	806448	1
R25	RES, CERM, 51.1, +-1%, 0.125W, 1206	806422	1
R26, R27, R69, R70, R89, R90	RES, MF, 20K, +-0.1%, 0.25W, 25PPM	810564	6
R30, R50, R85	RES, CHIP, CERM, 510, +-5%, 0.125W,	746388	3
R36, R103, R105	RES, CHIP, CERM, 1.2K, +-5%, 0.125W	746412	3
R37, R106, R110	RES, CHIP, CERM, 12, +-5%, 0.125W, 1	845458	3
R38, R49	RES, CHIP, CERM, 270, +-5%, 0.125W,	746354	2
R40	RES, CHIP, CERM, 100K, +-5%, 0.125W	740548	1
R42, R46	RES, CHIP, CERM, 470, +-5%, 0.125W,	740506	2
R43, R52, R109	RES, CHIP, CERM, 3K, +-5%, 0.125W, 1	746511	3
R45	RES, CHIP, CERM, 2.7K, +-5%, 0.125W	746503	1
R47, R60, R62, R66, R75, R76	RES, CHIP, CERM, 100, +-5%, 0.125W,	746297	6
R51	RES, CERM, 150, +-1%, 0.125W, 1206	772780	1
R53, R71	RES, CHIP, CERM, 5.1K, +-5%, 0.125W	746560	2
R58, R59, R64, R73	RES, CHIP, CERM, 56K, +-5%, 0.125W,	746701	4
R61	RES, CF, 1.5K, +-5%, 0.25W	810432	1
R63, R65, R95, R96,	RES, CHIP, CERM, 1K, +-5%, 0.125W, 1	745992	5

Table 6-12. A11 DAC PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R99			
R67	RES, MF, 806, +-1%, 0.125W, 100PM	810531	1
R68	RES, MF, 43.2K, +-0.1%, 0.25W, 25PP	810572	1
R72	RES, CF, 200, +-5%, 0.25W	810390	1
R74, R79-81	RES, CERM, 100K, +-1%, 0.125W, 1206	769802	4
R77, R92, R94	RES, CHIP, CERM, 2K, +-5%, 0.125W, 1	746461	3
R86, R87, R100	RES, CHIP, CERM, 330, +-5%, 0.125W,	746370	3
R88	RES, MF, 50K, +-0.1%, 0.25W, 25PPM	810580	1
R91	RES, MF, 4.12K, +-1%, 0.125W, 100PP	820381	1
R93	RES, CERM, 8.06K, +-1%, 0.125W, 120	806356	1
R97, R98, R114	RES, CHIP, CERM, 22K, +-5%, 0.125W,	746651	3
R104	RES, CHIP, CERM, 15K, +-5%, 0.125W,	746628	1
R107, R108	RES, CHIP, CERM, 1.8K, +-5%, 0.125W	746453	2
R111	RES, CF, 22K, +-5%, 0.25W	747535	1
R112, R113	RES, CF, 10K, +-5%, 0.25W	697102	2
R117-119, R123	RES, CHIP, CERM, 7.5K, +-5%, 0.125W	746586	4
T1	PULSE TRANSFORMER	802892	1
TP1, TP3	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	6
U1, U27, U28	IC, OP AMP, DUAL, LO OFFST VOLT, L	851704	3
U2, U20	IC, OP AMP, DUAL, PRECISION, 8-PIN	783696	2
U5	IC, OP AMP, POWER, IO=325MA	807917	1
U6	IC, CMOS, PROGRMBL INTERVAL TIME	806612	1
U7	IC, COMPARATOR, HI-SPEED, PRECISI	822197	1
U8	IC, CMOS, OCTL INV LINE DRVR, SOI	782938	1
U9	IC, CMOS, QUAD 2 INPUT OR GATE, S	783712	1
U10	IC, COMPARATOR, HI-SPEED, 14 PIN	647115	1
U11	IC, OP AMP, SINGLE, LOW NOISE FAS	783720	1
U12, U37	ISOLATOR, OPTO, LED TO TRANSISTO	454330	2
U13	ISOLATOR, OPTO, HI-SPEED, LED TO	504522	1
U14	IC, CMOS, DUAL D F/F, +EDG TRG, SO	782995	1
U15	IC, CMOS, DUAL MONOSTB MULTIVBRT	806620	1
U19	IC, OP AMP, DUAL, PRECISION MATCH	782375	1
U22	IC, OP AMP, JFET INPUT, 22V SUPPL	832584	1
U23	IC, DMOS, QUAD ANALOG SWITCH, SOI	806687	1
U24	IC, OP AMP, PRECISION, JFET INPUT	808097	1
U25	IC, CMOS, RR A/D CONVERTER	715680	1
U26	IC OP AMP, DUAL, HIGH SPEED	707976	1
U29, U38	IC, OP AMP, JFET INPUT, 8 PIN DIP	472779	2
U31	IC, CMOS, PROGRAMBL PERIPH INTRF	806604	1
U32	IC, CMOS, 3-8 LINE DCDR W ENABLE	783019	1
U33, U34	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	2
U35, U36	IC, COMPARATOR, QUAD, 14 PIN, SOIC	741561	2
VR1, VR4, VR31, VR32	ZENER, UNCOMP, 20.0V, 5%, 6.2MA, 0	810275	4
VR2, VR8, VR24	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	810267	3
VR3	ZENER, UNCOMP, 16.0V, 7.8MA, 0.4W	822205	1
VR5	ZENER, UNCOMP, 6.2V, 5%, 20.0MA, 0.	810283	1
VR6, VR11, VR30	ZENER, UNCOMP, 12.0V, 10%, 10.5MA,	741074	3
VR7, VR16	ZENER, UNCOMP, 22.0V, 5%, 5.6MA, 0.	811927	2
VR10, VR12	ZENER, UNCOMP, 10V, 10%, 20MA, 350M	783704	2
VR13	ZENER, UNCOMP, 13V, 5%, 9.5MA, 0.5W	820456	1
VR17, VR21	ZENER, UNCOMP, 18.0V, 5%, 7.0MA, 0.	810325	2
VR18, VR22	ZENER, UNCOMP, 15.0V, 5%, 8.5MA, 0.	820415	2
VR19, VR20	ZENER, UNCOMP, 3.3V, 5%, 20.0MA, 0.	820423	4
VR25	ZENER, UNCOMP, 3.3V, 10%, 20.0MA, 0	698647	1
VR26	ZENER, UNCOMP, 3.3V, 5%, 2MA, .350W	807008	1
VR27	ZENER, UNCOMP, 7.5V, 5%, 20MA, 350M	837138	1
VR28	ZENER, UNCOMP, 8.2V, 5%, 20MA, 350M	837146	1
VR29	ZENER, COMP, 6.4V, 2%, 2 PPM TC, 1.	810259	1
VR33, VR34	ZENER, UNCOMP, 7.5V, 5%, 20.0MA, 0.	810291	2

Table 6-12. A11 DAC PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
X1	SOCKET, IC, 40PIN, DUAL WIPE, BEAM	747170	1
Z2	REF DIVIDER RES NET ASSY TESTE	645341	1
Z4	RES, NET, SIP, 10 PIN, 5 RES, 56K, +	529131	1
Z5	RES, NET, SIP, 6 PIN, 5 RES, 510, +-	459974	1
Z8	RES NET THN F TESTED	809418	1
Z10	RES NET THN F TESTED	833830	1
Z12	RES, NET, SIP, 6 PIN, 5 RES, 10K, +-	500876	1

Table 6-13. A11A1 DAC Filter SIP PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1-9, C12, C13	CAP, CER, 0.22UF, +80-20%, 50V, Y5V	740597	11
C10, C11	CAP, POLYPR, 1.0UF, +-5%, 50V, HERM	783811	2
C14	CAP, CER, 100PF, +-10%, 50V, CG, 12	740571	1
P21, P22	HEADER, 2 ROW, 0.100CTR, RT ANG, 6	806919	2
R1, R2	RES, CHIP, CERM, 11K, +-5%, 0.125W,	769752	2
R3, R5	RES, CHIP, CERM, 18K, +-5%, 0.125W,	746636	2
R4	RES, CHIP, CERM, 22K, +-5%, 0.125W,	746651	1
U1	IC, OP AMP, ULTRA-LOW-NOISE, SOIC	783001	1
U2	IC, OP AMP, PRECISION, LOW NOISE	782920	1
VR1	ZENER, UNCOMP, 15.0V, 5%, 8.5MA, 0.	698704	1

Table 6-14. A11A2 DAC Buffered Reference SIP PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C5	CAP, CER, 10PF, +-10%, 100V, CG, 12	806943	2
C2, C3	CAP, CER, 0.22UF, +80-20%, 50V, Y5V	740597	2
C4, C6	CAP, CER, 1000PF, +-10%, 50V, CG, 1	747378	2
P11	HEADER, 2 ROW, 0.100CTR, RT ANG, 1	658112	1
P12	HEADER, 2 ROW, 0.100CTR, RT ANG,	424200	1
Q1-15	TRANSISTOR, SI, N-JFET, HI-VOLTAG	832147	15
R1, R7	RES, CHIP, CERM, 1K, +-5%, 0.125W, 1	745992	2
R5	RES, CHIP, CERM, 10, +-5%, 0.125W, 1	746214	1
R6, R8	RES, CHIP, CERM, 200, +-5%, 0.125W,	746339	2
R9	RES, CERM, 100K, +-1%, 0.125W, 1206	769802	1
U1	IC, OP AMP, DUAL, PRECISION, 8-PIN	783696	1
U2	IC OP AMP, DUAL, HIGH SPEED	707976	1
VR1	ZENER, UNCOMP, 22.0V, 5%, 5.6MA, 0.	181073	1
Z1	RES, NET, SIP, 10 PIN, 5 RES, 56K, +	529131	1
Z2	RES, NET, SIP, 6 PIN, 5 RES, 51K, +-	514042	1

Table 6-15. A12 Oscillator Control PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1-4, C12, C14, C16, C18, C48	CAP, TA, 4.7UF, +-20%, 25V	807644	9
C5, C23, C24, C36-38, C44-47, C49, C50, C56, C57, C61, C64, C65, C67, C68, C70-72, C76-81	CAP, POLYES, 0.22UF, +-5%, 50V	747519	28
C8, C10	CAP, AL, 2.2UF, +-20%, 50V, SOLV PR	769687	2
C21	CAP, CER, 10PF, +-10%, 3000V, CG	817049	1
C22, C25	CAP, TA, 330UF, +-20%, 3V	385963	2
C26, C29, C30, C42, C60	CAP, POLYES, 0.47UF, +-10%, 50V	697409	5
C27, C28, C31, C43, C63	CAP, POLYES, 0.047UF, +-10%, 50V	820548	5
C33, C58, C59	CAP, CER, 120PF, +-5%, 50V, COG	721142	3
C34, C35, C86, C87	CAP, TA, 47UF, +-20%, 20V	348516	4
C39, C53	CAP, CER, 330PF, +-5%, 50V, COG	697441	2
C40, C41	CAP, TA, 10UF, +-20%, 25V	714774	2
C51, C52, C66	CAP, CER, 82PF, +-2%, 50V, COG	714857	3
C54	CAP, CER, 3.3PF, +0.25PF, 100V, COJ	816678	1
C55	CAP, CER, 6.8PF, +-0.25PF, 50V, COG	715243	1
C62	CAP, POLYES, 1.0UF, +-10%, 50V	733089	1
C69, C90, C91	CAP, POLYES, 0.01UF, +-10%, 50V	715037	3
C74	CAP, CER, 3300PF, +-5%, 50V, CG	830612	1
C75, C88	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C82, C85	CAP, POLYES, 0.022UF, +-10%, 50V	715268	2
C83	CAP, CER, 150PF, +-10%, 50V, X7R	682377	1
C84	CAP, POLYPR, 0.47UF, +-10%, 160V	446807	1
CR1-3	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	3
CR4, CR5	DIODE, SI, SCHOTTKY BARRIER, SMAL	408815	2
CR6-8	DIODE, SI, BV= 75.0V, IO=150MA, 50	698720	3
CR12-15	DIODE, SI, BV= 70.0V, 500 MW	851910	4
H4-7	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H13	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	1
HS1	HEAT DIS, RADIAL, 0.54X1.25X.35	808204	1
K1	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	1
K2-9	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	8
L1-4	CHOKE, 6TURN	320911	4
M10	SHIELD, ANALOG REAR	797803	1
M12	OSCILLATOR THERMAL COVER	797696	1
MP8, MP9	EJECTOR, PWB, NYLON	494724	2
MP14	SPACER, TRANSISTOR, TO-5, DAP, .17	837823	1
P501, P502	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1	TRANSISTOR, SI, 100V, 1W, CASE	806497	1
Q2	TRANSISTOR, SI, 100V, 1W, CASE	806489	1
Q3	TRANSITOR, SI, PNP, SMALL SIG, SEL	851977	1
Q4	TRANSISTOR, SI, NPN SMALL SIGNAL	853478	1
Q5, Q9, Q11	TRANSISTOR, SI, N-JFET, TO-92	832162	3
Q6, Q7, Q12, Q18, Q20	TRANSISTOR, SI, N-CHAN, TO-92, SWI	832139	[illegible]
Q8, Q13	TRANSITOR, SI, N-JFET, UHF/VHF US	851972	2

Table 6-15. A12 Oscillator Control PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q10	TRANSISTOR, SI, P-MOS, ZENER PROT	306142	1
Q14	TRANSISTO, SI, NMOS, 1W, 4 PIN DIP	853692	1
Q19	TRANSISTOR, SI, N-DMOS FET, TO-72	394122	1
R1, R2, R55	RES, CF, 30K, +-5%, 0.25W	574251	3
R3	RES, MF, 143K, +-1%, 0.125W, 100PPM	719641	1
R4, R12	RES, CF, 3K, +-5%, 0.25W	573279	2
R5, R13, R25, R52, R53, R68, R69	RES, CF, 1K, +-5%, 0.25W	573170	7
R6	RES, CF, 750, +-5%, 0.25W	810374	1
R7	RES, CF, 200, +-5%, 0.25W	810390	1
R8-10	RES, MF, 113K, +-1%, 0.125W, 100PPM	291302	3
R11	RES, CF, 20K, +-5%, 0.25W	697110	1
R14	RES, CF, 22K, +-5%, 0.25W	573451	1
R15	RES, CF, 5.1K, +-5%, 0.25W	573329	1
R16	RES, CF, 15, +-5%, 0.25W	641043	1
R17, R39	RES, CF, 510, +-5%, 0.25W	573139	2
R18	RES, CF, 47, +-5%, 0.25W	822189	1
R19	RES, CF, 10, +-5%, 0.25W	807669	1
R20	RES, MF, 301K, +-1%, 0.125W, 25PPM	379156	1
R21	RES, CF, 2K, +-5%, 0.25W	573238	1
R22, R24, R29, R66	RES, CF, 100K, +-5%, 0.25W	573584	4
R23, R30, R33	RES, CF, 100K, +-5%, 0.25W	658963	3
R26	RES, MF, 316K, +-1%, 0.125W, 100PPM	720078	1
R27, R28	RES, CF, 1K, +-5%, 0.25W	780585	2
R31, R37, R45	RES, MF, 866, +-0.1%, 0.125W, 50PPM	838441	3
R32, R50	RES, CF, 120, +-5%, 0.25W	643494	2
R34	RES, MF, 3.61K, +-0.25%, 0.25W, 100	832394	1
R35, R36, R40, R41	RES, MF, 649K, +-1%, 0.125W, 100PPM	721597	4
R38, R42	RES, MF, 357K, +-1%, 0.125W, 25PPM	312793	2
R43, R63-65	RES, CF, 20K, +-5%, 0.25W	573444	4
R44	RES, CF, 2.2K, +-5%, 0.25W	573246	1
R46	RES, CF, 12K, +-5%, 0.25W	573402	1
R47	RES, CF, 560, +-5%, 0.25W	573147	1
R48	RES, MF, 1.15K, +-1%, 0.125W, 50PPM	347187	1
R49	RES, MF, 11.8K, +-1%, 0.125W, 100PP	720615	1
R54, R56	RES, CF, 10K, +-5%, 0.25W	573394	2
R57	RES, CF, 75K, +-5%, 0.25W	641134	1
R58	RES, MF, 1K, +-1%, 0.125W, 100PPM	719468	1
R62	RES, CF, 4.7K, +-5%, 0.25W	573311	1
R67	RES, MF, 562K, +-1%, 0.125W, 100PPM	757815	1
TP1-8	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	8
U1, U2, U7	IC, OP AMP, HI-SLEW RATE, 8 PIN D	386268	3
U3	IC, OP AMP, 50MHZ, CURRENT FEEDBA	836262	1
U5, U26	IC, OP AMP, LO-OFFSET VOLTAGE, LO	605980	2
U8, U19	IC, CMOS, QUAD BILATERAL SWITCH	586735	2
U9	IC, OP AMP, DUAL, JFET INPUT, 8 PI	495192	1
U10	IC, CMOS, 14BIT DAC, 12BIT ACC, CU	773101	1
U11, U30, U31	IC, OP AMP, PRECISION, LOW NOISE	782920	3
U12	IC, OP AMP, DUAL, PRECISION MATCH	782375	1
U13	IC, OP AMP, JFET INPUT, WIDE BAND	808105	1
U14	RMS CONVERTER TESTED 400 OHM-A	842596	1
U15	IC, OP AMP, QUAD JFET INPUT, 14 P	659748	1
U16	RMS CONVERTER TESTED 400 OHM-A	842591	1
U17	IC, ARRAY, 5 TRANS, NPN, 3 ISO, 2 D	248906	1
U18	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U20	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U21, U22	IC, COMPARATOR, QUAD, 14 PIN DIP	387233	2

Table 6-15. A12 Oscillator Control PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U23, U24	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	2
U25	IC, VOLT REG, FIXED, +5 VOLTS, 1.5	428847	1
VR1, VR2	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	698696	2
VR3	ZENER, UNCOMP, 5.1V, 5%, 20MA, 0.4W	722926	1
VR4	ZENER, UNCOMP, 6.8V, 2%, 175.0MA, 5	325845	1
VR5, VR6	ZENER, UNCOMP, 3.9V, 5%, 64.0MA, 1.	836700	2
Z1	RES, NET, THK F,	760686	1
Z2, Z4	RNET, 8840A OUTPUT DIVIDER	655811	2
Z3	RES, NET, THN F FINAL TEST	760645	1
Z5	RES, NET, DIP, 14 PIN, 7 RES, 10K, +	364000	1
Z6	RES, NET, SIP, 8 PIN, 7 RES, 1K, +-2	414557	1
Z7, Z8	RES NET THK F,	785105	2
Z9	RES, NET, DIP, 16 PIN, 8 RES, 5.1K,	544130	1
Z10	RES, NET, SIP, 8 PIN, 4 RES, 4.7K, +	573881	1

Table 6-16. A13 Oscillator Output PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C2-4, C16, C20, C23,C26-28, C32, C33, C46, C47, C51, C52, C54, C55, C68-71, C88-92, C102-104, C110, C111, C113, C114	CAP, POLYES, 0.22UF, +-5%, 50V	747519	33
C5, C14, C30	CAP, CER, 15PF, +-20%, 50V, COG	697524	3
C6, C15, C31	CAP, CER, 82PF, +-2%, 50V, COG	714857	3
C17, C29	CAP, CER, 2.7PF, +-0.25PF, 50V, COG	773044	2
C19, C34, C85	CAP, CER, 56PF, +-2%, 50V, COG	714378	3
C21, C37	CAP, MICA, 560PF, +-1%, 300V	494609	2
C22, C38	CAP, POLYCA, 6150PF, +-1%, 50V	800466	2
C24, C40	CAP, POLYCA, 0.0621UF, +-1%, 50V	800482	2
C25, C41	CAP, POLYCA, 0.622UF, +-1%, 50V	800474	2
C44, C123	CAP, CER, 10PF, +-20%, 50V, CG	721589	2
C45	CAP, POLYPR, 0.033UF, +-10%, 63V	721050	1
C48, C84	CAP, AL, 10UF, +-20%, 16V, NON-POLA	697177	2
C49	CAP, AL, 470UF, +-20%, 10V, SOLV PR	822387	1
C56-59	CAP, TA, 22UF, +-20%, 10V	658971	4
C60, C61, C108, C109	CAP, TA, 4.7UF, +-20%, 25V	807644	4
C62	CAP, POLYES, 0.47UF, +-10%, 50V	697409	1
C75	CAP, CER, 120PF, +-5%, 50V, COG	721142	1
C76, C77	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	2
C78, C79	CAP, POLYES, 0.01UF, +-10%, 50V	715037	2
C80, C81	CAP, POLYES, 0.1UF, +-10%, 50V	649913	2
C82, C83	CAP, POLYES, 1.0UF, +-10%, 50V	733089	2
C93-99, C106, C107	CAP, TA, 10UF, +-20%, 25V	714774	9
C100, C101, C118	CAP, AL, 2.2UF, +-20%, 50V, SOLV PR	769687	3
C105	CAP, CER, 3300PF, +-5%, 50V, CG	830612	1
C112	CAP, CER, 4.7PF, +-0.25PF, 50V, COG	721837	1
C115	CAP, CER, 6800PF, +-5%, 100V, COG	816710	1
C116, C117	CAP, TA, 4.7UF, +-20%, 50V	832675	2
C119, C120	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C122	CAP, CER, 27PF, +-2%, 100V, COG	816652	1
CR1-11, CR22, CR23	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	13
CR13-20	DIODE, SI, N-JFET, CURRENT REG, IF	852116	8
H4-7	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H9-12	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	4
HS1-3	HEAT DIS, RADIAL, 0.54X1.25X.35	808204	3
HS4-7	HEAT DIS, 0.80X.85X.30, CASE 1	800136	4
HS9, HS10	HEAT DIS, SLEEVE, TO-5	380220	2
HS58	HEAT DIS, VERT, 0.83X.50X.395,	800144	1
K1	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	1
K2-4	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	3
L1-5, L13, L14	CHOKE, 6TURN	320911	7
L6-12	CORE, TOROID, FERRITE, .047X.138X	321182	7
L15	TRANSFORMER, PULSE	660589	1
MP2, MP3	EJECTOR, PWB, NYLON	494724	2
MP4-6	SPACER, TRANSISTOR MOUNT, DAP	152207	3
MP8	AIR DUCT, OSCILLATOR	802959	1
MP13-15	SPACER, TRANSISTOR, TO-5, DAP, .17	837823	3
MP16, MP17	SPACER, SWAGED, RND, BRASS, 6-32X	544254	2
P511, P512	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q6	TRANSISTOR, SI, N-JFET, TO-92	832162	1
Q7	TRANSISTOR, SI, N-DMOS FET, TO-72	394122	1
Q8	TRANSISTOR, SI, NPN, SM SIGNAL, HI	272930	1
Q9	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	1

Table 6-16. A13 Oscillator Output PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q10, Q11	TRANSISTOR, SI, 100V, 1W, CASE	806497	2
Q13	TRANSISTOR, SI, NPN, HI-CURRENT	402602	1
Q14	TRANSISTOR, SI, PNP, SMALL SIG, RF	800201	1
Q15	TRANSISTOR, SI, PNP, T92	698233	1
Q16, Q17	TRANSISTOR, SI, 100V, 1W, CASE	806489	2
R1, R6, R43, R60, R65	RES, MF, 2K, +-1%, 0.125W, 100PPM	816629	5
R7, R9, R11, R18	RES, CF, 200, +-5%, 0.25W	810390	4
R12, R13, R83	RES, MF, 4.99K, +-1%, 0.125W, 100PP	721548	3
R19, R24, R25, R37, R50, R70, R79	RES, CF, 10K, +-5%, 0.25W	697102	7
R21	RES, CF, 3.9K.+-5%, 0.25W	810416	1
R22, R40, R64, R67, R69, R72, R108-110	RES, CF, 1K, +-5%, 0.25W	780585	9
R23, R27, R33, R38, R51, R78	RES, CF, 16K, +-5%, 0.25W	714303	6
R26	RES, CF, 9.1K, +-5%, 0.25W	706663	1
R28	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	1
R29, R62, R68	RES, MF, 10K, +-1%, 0.125W, 100PPM	658914	3
R32	RES, CF, 20K, +-5%, 0.25W	697110	1
R35, R36, R47, R52, R53, R59, R63, R74, R75	RES, CF, 4.7K, +-5%, 0.25W	721571	13
R39, R54, R76	RES, CF, 12K, +-5%, 0.25W	757799	3
R41	RES, CF, 100K, +-5%, 0.25W	658963	1
R42	RES, MF, 10.5K, +-1%, 0.125W, 100PP	816611	1
R48	RES, CF, 51K+-5%, 0.25W	747550	1
R49	RES, CF, 270, +-5%, 0.25W	810424	1
R55, R77	RES, CF, 22K, +-5%, 0.25W	747535	2
R56	RES, MF, 34.8K, +-0.1%, 0.125W, 50P	772582	1
R57	RES, CF, 43K, +-5%, 0.25W	821777	1
R58	RES, CF, 47K, +-5%, 0.25W	721787	1
R61, R66	RES, MF, 7.87K, +-1%, 0.125W, 100PP	810549	2
R71, R73	RES, CF, 3K, +-5%, 0.25W	810366	2
R84, R85	RES, CF, 33K, +-5%, 0.25W	733667	2
R87, R94	RES, CF, 100, +-5%, 0.25W	810465	2
R88	RES, CF, 4.7, +-5%, 0.25W	816637	1
R89, R90, R97, R98	RES, CF, 10, +-5%, 0.25W	807669	4
R91, R99	RES, CF, 2.7, +-5%, 0.25W	640953	2
R92, R93, R95, R96	RES, CF, 3.9, +-5%, 0.25W	810473	4
R100, R101	RES, MF, 30.1K, +-1%, 0.125W, 100PP	772061	2
S1	SWITCH, SLIDE, SPDT	477984	1
TP1-10	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	10
U2	IC, VOLT REG, FIXED, -12 VOLTS, 1.	381665	1
U3, U6, U9	IC, OP AMP, JFET INPUT, WIDE BAND	808105	3
U5, U7, U11	RES. NET HYBRID, ASSEMBLED	793885	3
U8, U29	IC, OP AMP, HI-SLEW RATE, 8 PIN D	386268	2
U10, U15, U16, U19	IC, BPLR, FOUR-QUADRANT MULT, 16	343335	4
U12, U32, U33	IC, CMOS, OCTL D F/F W/3-STATE, +	585364	3
U17, U27	IC, CMOS, DUAL 4-1 LINE MUX/DMUX	429886	2

Table 6-16. A13 Oscillator Output PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U18	IC, OP AMP, JFET INPUT, 8 PIN DIP	472779	1
U20	IC, COMPARATOR, DUAL, LO-PWR, 8 PI	478354	1
U21	IC, FTTL, QUAD 2 INPUT NAND GATE	654640	1
U22	IC, FTTL, DUAL JK F/F, -EDG TRIG	781211	1
U23	IC, COMPARATOR, DUAL, HI-SPEED, 14	647123	1
U24	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	1
U25	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
U26	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U28	IC, CMOS, DUAL 8 BIT DAC, CURRENT	722272	1
U31	IC, OP AMP, DUAL, JFET INPUT, 8 PI	495192	1
VR3, VR4	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	810267	2
VR7	ZENER, UNCOMP, 8.2V, 5%, 20MA, 0.4W	810309	1
Z1	RES, NET, SIP, 6 PIN, 5 RES, 39K	831065	1
Z2	RES, NET, DIP, 14 PIN, 7 RES, 10K, +	364000	1
Z3	RES, NET, SIP, 8 PIN, 7 RES, 1K, +-2	414557	1
Z4, Z5	RES, NET, SIP, 8 PIN, 4 RES, 10K, +-	513309	2
Z6	RES, NET, SIP, 6 PIN, 5 RES, 3.6K, +	478818	1

Table 6-17. A13A1 Oscillator Wideband SMD

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C3, C4, C6-8, C12, C13	CAP, CER, 0.22UF, +80-20%, 50V, Y5V	740597	8
C2	CAP, CER, 100PF, +-10%, 50V, CG, 12	740571	1
C5	CAP, CER, 10PF, +-10%, 100V, CG, 12	806943	1
C9	CAP, CER, 470PF, +-10%, 50V, COG, 12	747360	1
C10	CAP, CER, 1000PF, +-10%, 50V, CG, 1	747378	1
C11	CAP, CER, 0.01UF, +-10%, 50V, X7R, 1	747261	1
CR4-6, CR9, CR10	DIODE, SI, BV=70.0V, IO=50MA, DUAL	742320	5
P1, P2	HEADER, 2 ROW, 0.100CTR, RT ANG, 1	806935	2
Q1	TRANSISTOR, SI, N-JFET, SOT23	844584	1
Q2, Q4, Q5, Q7	TRANSISTOR, SI, NPN, SMALL SIGNAL	845438	4
Q3	TRANSISTOR, SI, PNP, SMALL SIGNAL	742684	1
Q6, Q8	TRANSISTOR, SI, PNP, SMALL SIGNAL	838516	2
Q9	TRANSISTOR, SI, NPN, SMALL SIGNAL	742676	1
R1, R9, R25	RES, CHIP, CERM, 2K, +-5%, 0.125W, 1	746461	3
R2	RES, CHIP, CERM, 2.7K, +-5%, 0.125W	746503	1
R3, R22	RES, CHIP, CERM, 330, +-5%, 0.125W,	746370	2
R4, R26	RES, CHIP, CERM, 510, +-5%, 0.125W,	746388	2
R5	RES, CHIP, CERM, 5.1K, +-5%, 0.125W	746560	1
R6, R23, R31	RES, CHIP, CERM, 3.9K, +-5%, 0.125W	746545	3
R7, R16, R18, R19, R21, R27-29	RES, CHIP, CERM, 47, +-5%, 0.125W, 1	746263	8
R8	RES, CHIP, CERM, 100K, +-5%, 0.125W	740548	1
R10	RES, CHIP, CERM, 56, +-5%, 0.125W, 1	807727	1
R11, R17	RES, CERM, 150, +-1%, 0.125W, 1206	772780	2
R12	RES, CHIP, CERM, 27, +-5%, 0.125W, 1	807735	1
R13	RES, CHIP, CERM, 100, +-5%, 0.125W,	746297	1
R14	RES, CHIP, CERM, 620, +-5%, 0.125W,	745984	1
R15	RES, CHIP, CERM, 15K, +-5%, 0.125W,	746628	1
R20	RES, CHIP, CERM, 390, +-5%, 0.125W,	740498	1
R24	RES, CHIP, CERM, 910, +-5%, 0.125W,	769257	1
R30	RES, VAR, CERM, 500, +-20%, 0.3W	853515	1
U1	IC, OP AMP, ULTRA-LOW-NOISE, SOIC	783001	1
U2	IC, OP AMP, SINGLE, LOW NOISE FAS	783720	1
VR1, VR5-7	ZENER, UNCOMP, 6.2V, 5%, 20MA, .35W	782441	4
VR2	ZENER, UNCOMP, 22.0V, 5%, 5.6MA, SO	831230	1
VR3, VR4	ZENER, UNCOMP, 3.3V, 5%, 2MA, .350W	807008	2

Table 6-18. A14 High Voltage Control PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1	CAP, POLYES, 0.33UF, +-20%, 2000V	423301	1
C2	CAP, POLYES, 0.10UF, +-20%, 1400V	821512	1
C3, C4	CAP, AL, 470UF, +-20%, 16V, SOLV PR	772855	2
C5	CAP, POLYES, 1.0UF, +-10%, 50V	733089	1
C6, C7	CAP, TA, 10UF, +-20%, 35V	816512	2
C8, C9	CAP, TA, 4.7UF, +-20%, 50V	832675	2
C10, C20, C24-32	CAP, POLYES, 0.1UF, +-10%, 50V	649913	11
C11-13	CAP, TA, 22UF, +-20%, 10V	658971	3
C14	CAP, CER, 330PF, +-5%, 50V, COG	697441	1
C15	CAP, CER, 120PF, +-5%, 50V, COG	721142	1
C17	CAP, POLYES, 2200PF, +-10%, 50V	832683	1
C18	CAP, TA, 1UF, +-20%, 35V	697417	1
C21, C22	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C23	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	1
C33	CAP, CER, 27PF, +-2%, 100V, COG	816652	1
CR1-4	DIODE, SI, HIGH VOLTAGE, PIV=2K, 4	851956	4
CR5	DIODE, SI, RECT, BRIDGE, BV= 50V, I	586115	1
CR6-12	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	7
E1	CABLE TIE, 4"L, 0.100"W, 0.75 DIA	172080	1
H4-7	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H8, H9, H11	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	3
J1	CONN, MATE-N-LOK, HEADER, 14 PIN	845318	1
K1, K2, K4, K8, K10, K11, K14	RELAY, ARMATURE, 2 FORM C, 5V	733063	7
K3, K5, K6, K9, K12, K13,K15, K16	RELAY, ARMATURE, 1 FORM A/1 FORM	831545	8
K7	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	1
L1	CHOKE, 6TURN	320911	1
MP1, MP2	EJECTOR, PWB, NYLON	494724	2
MP3	SHIELD, HIGH VOLTAGE CONTROL	761197	1
MP4	SHIELD, HIGH VOLTAGE MYLAR	775775	1
MP8	HEAT DIS, PRESS ON, TO-5	418384	1
MP10, MP13	WASHER, FLAT, STL, .149, .375, .031	110270	2
P611, P612	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q2	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	1
Q3, Q4	TRANSISTOR, SI, P-JFET, TO-92	852111	2
R1, R2	RES, CF, 47, +-5%, 0.25W	822189	2
R3-5	RES, CC, 200K, +-5%, 1W	109926	3
R6, R8, R65, R66	RES, CF, 10, +-5%, 0.25W	807669	4
R7	RES, CF, 22K, +-5%, 0.25W	747535	1
R9-12, R64	RES, CF, 1.5M, +-5%, 0.25W	649962	5
R13	RES, CF, 9.1K, +-5%, 0.25W	706663	1
R14, R15	RES, CF, 620, +-5%, 0.25W	810408	2
R17, R46, R55	RES, CF, 100K, +-5%, 0.25W	658963	3
R18	RES, CF, 100, +-5%, 0.25W	810465	1
R19	RES, MF, 162K, +-1%, 0.125W, 100PPM	817569	1
R20	RES, MF, 412K, +-1%, 0.125W, 50PPM	714287	1
R21, R24, R33, R34, R47, R56	RES, CF, 10K, +-5%, 0.25W	697102	6
R23	RES, CF, 200K, +-5%, 0.25W	681841	1
R25	RES, CF, 750K, +-5%, 0.25W	747543	1
R26, R44, R45	RES, MF, 100K, +-1%, 0.125W, 100PPM	757807	3
R27, R29	RES, MF, 36.5K, +-1%, 0.125W, 100PP	820324	2
R28	RES, MF, 20.5K, +-1%, 0.125W, 100PP	655233	1

Table 6-18. A14 High Voltage Control PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R30-32	RES, MF, 18.2K, +-1%, 0.125W, 100PP	756429	3
R35-39, R50, R52	RES, MF, 196K, +-1%, 0.125W, 100PPM	769984	7
R40, R41	RES, MF, 464K, +-1%, 0.125W, 100PPM	772020	2
R42	RES, CF, 1.5K, +-5%, 0.25W	810432	1
R43	RES, MF, 301K, +-1%, 0.125W, 100PPM	655274	1
R54	RES, CF, 2K, +-5%, 0.25W	810457	1
R57, R58	RES, CF, 750, +-5%, 0.25W	810374	2
R59	RES, CF, 16K, +-5%, 0.25W	714303	1
R60, R61	RES, CF, 20K, +-5%, 0.25W	697110	2
R62, R63	RES, CF, 3K, +-5%, 0.25W	810366	2
R67	RES, CF, 3.9, +-5%, 0.25W	810473	1
T1	TRANSFORMER, HIGH VOLTAGE	775288	1
TP1-6	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	6
U1	IC, OP AMP, DUAL, LO OFFST, VOLT, L	685164	1
U2	IC, OP AMP, QUAD, JFET INPUT, 14 P	483438	1
U3	IC, OP AMP, SINGLE, HIGH VOLTAGE	782342	1
U4	IC, CMOS, MONOSTABL/ASTABL MULTI	535575	1
U6, U7	IC, CMOS, QUAD BILATERAL SWITCH	586735	2
U8	IC, CMOS, HEX INVERTER, UNBUFFERE	741199	1
U9	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U10-13	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	4
U14	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
VR1	ZENER, UNCOMP, 6.8V, 5%, 20.0MA, 0.	820431	1
VR2, VR3	DIODE, TRANS SUPPRESSOR, 400V, 5%	845003	2
VR4, VR5	ZENER, UNCOMP, 16.0V, 5%, 15.5MA, 1	313221	2
VR6, VR7	ZENER, UNCOMP, 3.3V, 5%, 20.0MA, 0.	820423	2
Z1	RES, NET, SIP, 8 PIN, 7 RES, 10K, +-	412924	1

Table 6-19. A15 High Voltage/High Current PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C2, C22, C29, C42	CAP, POLYES, 0.01UF, +-10%, 50V	715037	4
C4	CAP, POLYPR, 0.022UF, +-5%, 1500V	806968	1
C5	CAP, CER, 4700PF, +-20%, 100V, COG	743427	1
C6	CAP, POLYES, 0.047UF, +-10%, 50V	820548	1
C7	CAP, CER, 180PF, +-2%, 50V, COG	820522	1
C8, C10	CAP, CER, 680PF, +-5%, 50V, COG	743351	2
C11	CAP, CER, 330PF, +-5%, 50V, COG	697441	1
C12, C13, C43	CAP, POLYES, 0.47UF, +-10%, 50V	697409	3
C14, C19	CAP, TA, 2.2UF, +-10%, 35V	697433	2
C15-17, C20, C21, C23-28, C32, C33, C35, C38, C40	CAP, POLYES, 0.1UF, +-10%, 50V	649913	16
C18	CAP, CER, 100PF, +-5%, 50V, CG	831495	1
C30, C31, C37, C39	CAP, TA, 10UF, +-20%, 35V	816512	4
C34	CAP, TA, 22UF, +-20%, 10V	658971	1
C41	CAP, POLYES, 0.22UF, +-10%, 50V	706028	1
CR1, CR4, CR11-16	DIODE, SI, BV= 75.0V, IO=150MA, 50	698720	8
CR5, CR6, CR9, CR10	DIODE, SI, 100 PIV, 1.0 AMP	742874	4
CR17, CR18	DIODE, SI, N-JFET, CURRENT REG, IF	852116	2
CR19	DIODE, SI, N-JFET, CURRENT REG, IF	852124	1
H1, H2	SCREW, MACH, PH, P, STL, 6-32X.500	152173	2
H4	DC AMP HYBRID C	813444	1
H6-10, H21	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	6
H17-20	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
HR7	HIGH VOLTAGE DC HYBRID	775254	1
K1	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	1
K2, K3	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	2
K4, K5, K8, K9, K12	RELAY, ARMATURE, 2 FORM C, 5V	733063	5
K6, K7, K10, K11, K14	RELAY, ARMATURE, 1 FORM A/1 FORM	831545	5
L4, L5	CHOKE, 6TURN	320911	2
MP1, MP2	EJECTOR, PWB, NYLON	494724	2
MP3	SHIELD, HIGH VOLTAGE, REAR	791921	1
MP4	MOLDED COVER, REF. HYBRID	797746	1
MP5	MOLDED COVER, HYBRID, R-NET	775619	1
MP6-9	INSERT, STANDOFF, BROACH, SNAP TO	832469	4
MP10	THERMAL INSULATOR, HIGH VOLTAG	797829	1
MP11, MP12	SCREW, MACH, PH, P, STL, 4-40X.250	558791	2
MP15	SHIELD, HIGH VOLTAGE MYLAR	775775	1
MP16-19	SPACER, TRANSISTOR MOUNT, DAP	152207	4
MP22	HI VOLT CLAMP BAR	760850	1
P601, P602	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q3, Q13	TRANSISTOR, SI, NPN, SMALL SIGNAL	346916	2
Q4, Q15, Q22, Q23	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	4
Q6, Q12	TRANSISTOR, SI, PNP, SMALL SIGNAL	402586	2
Q8, Q18	TRANSISTOR, SI, BV=40V, 40W, TO-22	369660	2
Q9, Q19	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	2
Q10	TRANSISTOR, SI, P-JFET, TO-92	852111	1
Q11	TRANSISTOR, SI, BV=100V, 2W, TO-	454041	1
Q14	TRANSISTOR, SI, BV=100V, 40W, TO-	454033	1
Q16, Q24	TRANSISTOR, SI, PNP, T92	698233	2
Q20, Q21	TRANSISTOR, SI, N-JFET, LOW IGSS,	707703	2
R1, R11, R71, R72	RES, CF, 1K, +-5%, 0.25W	573170	4
R2, R15, R39	RES, CF, 100K, +-5%, 0.25W	573584	3

Table 6-19. A15 High Voltage/High Current PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R4, R51, R53 R61-64, R74	RES, CF, 100, +-5%, 0.25W	573014	8
R5	RES, CF, 1.5K, +-5%, 0.25W	810432	1
R6, R9	RES, CF, 1M, +-5%, 0.25W	573691	2
R7	RES, CF, 51K+-5%, 0.25W	747550	1
R8, R19	RES, CF, 3K, +-5%, 0.25W	573279	2
R10	RES, CF, 820, +-5%, 0.25W	574970	1
R12	RES, CF, 33K, +-5%, 0.25W	733667	1
R13	RES, MF, 34.8K, +-1%, 0.125W, 100PP	772319	1
R14, R16, R21, R27, R28, R40, R44, R52, R54	RES, CF, 10K, +-5%, 0.25W	573394	9
R17, R41	RES, CF, 4.7K, +-5%, 0.25W	573311	2
R18	RES, CF, 22K, +-5%, 0.25W	573451	1
R20	RES, CF, 1.5K, +-5%, 0.25W	573212	1
R22	RES, CF, 16K, +-5%, 0.25W	641118	1
R23, R24, R60, R65	RES, CF, 10, +-5%, 0.25W	572941	4
R25, R26	RES, MF, 16.9, +-1%, 0.125W, 100PPM	281790	2
R29, R30	RES, CF, 8.2K, +-5%, 0.25W	573378	2
R31, R32	RES, CC, 2K, +-5%, 0.5W	169854	2
R33-35	RES, CC, 470, +-10%, 0.5W	108415	3
R36	RES, CF, 47, +-5%, 0.25W	572982	1
R37, R38	RES, MF, 825, +-1%, 0.125W, 100PPM	294892	2
R42, R43, R45, R46	RES, MF, 10K, +-1%, 0.125W, 100PPM	719476	4
R47	RES, CF, 160, +-5%, 0.25W	641084	1
R48, R50	RES, MF, 2.21K, +-1%, 0.125W, 100PP	347476	2
R56, R69	RES, MF, 191, +-1%, 0.125W, 100PPM	719799	2
R57, R68, R77, R78	RES, WW, 0.1, +-3%, 0.7W	255679	4
R58, R67	RES, CF, 330K, +-5%, 0.25W	641159	2
R59, R66	RES, CF, 68, +-5%, 0.25W	643783	2
R73, R75	RES, CF, 2K, +-5%, 0.25W	573238	2
R76	RES, CF, 3.3, +-5%, 0.25W	348730	1
R79, R82	RES, CF, 1K, +-5%, 0.25W	780585	2
R80, R83	RES, CF, 4.7K, +-5%, 0.25W	721571	2
R81, R84	RES, CF, 10K, +-5%, 0.25W	697102	2
TP1, TP3-11	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	10
TP2	SOCKET, SINGLE, PWB, FOR 0.080 PI	170480	1
U1	IC, OP AMP, JFET INPUT, 22V SUPPL	832584	1
U2, U4, U5	IC, OP AMP, JFET INPUT, 8 PIN DIP	472779	3
U3	IC, OP AMP, DUAL, LO OFFST, VOLT, L	685164	1
VR1, VR2, VR5, VR6	ZENER, UNCOMP, 16.0V, 5%, 15.5MA, 1	313221	4
VR3, VR4	ZENER, UNCOMP, 20.0V, 5%, 6.2MA, 0.	832576	2
VR7, VR8	ZENER, UNCOMP, 16.0V, 5%, 7.8MA, 0.	698712	2
Z5	R-NET/HEAT SINK ASSY-4R3	761288	1
Z6	R-NET/HEAT SINK ASSY-4R23	761296	1

Table 6-20. A16 Power Amplifier PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C2, C63	CAP, CER, 10PF, +-10%, 3000V, CG	817049	3
C3	CAP, MICA, 560PF, +-5%, 500V	170431	1
C4, C28	CAP, CER, 0.02UF, +-20%, 500V, Z5U	407403	2
C6, C17, C23	CAP, CER, 22PF, +-10%, 1000V, COG	817023	3
C7, C24, C43	CAP, CER, 1000PF, +-20%, 50V, X7R	697458	3
C8, C13, C16, C20, C47, C49, C60, C61 C68-71	CAP, POLYES, 0.22UF, +-5%, 50V	747519	12
C9, C21, C31-34	CAP, TA, 15UF, +-20%, 20V	807610	6
C10, C25	CAP, TA, 1UF, +-20%, 35V	697417	2
C11	CAP, CER, 22PF, +-2%, 50V, COG	714832	1
C12	CAP, CER, 2000PF, +-20%, 100V, Z5U	757096	1
C15	CAP, CER, 0.01UF, +80-20%, 500V, Z5	816991	1
C18	CAP, CER, 3.3PF, +-0.25PF, 1000V, C	178483	1
C19	CAP, CER, 100PF, +-2%, 100V, CG	812115	1
C22	CAP, MICA, 2PF, +-0.5PF, 500V	175208	1
C26	CAP, CER, 1000PF, +-20%, 3000V, Z5U	832709	1
C27, C78, C79	CAP, AL, 3.3UF, +30-20%, 450V, SOLV	782524	3
C40	CAP, POLYES, 1.0UF, +-10%, 50V	733089	1
C41	CAP, POLYPR, 0.15UF, +-10%, 400V	557504	1
C42	CAP, CER, 470PF, +-10%, 50V, COG	733071	1
C45	CAP, TA, 2.2UF, +-10%, 35V	697433	1
C48, C72	CAP, CER, 1.2PF, +-0.25PF, 50V, M7J	715235	2
C57	CAP, CER, 100PF, +-10%, 1000V, S3N	816983	1
C65, C67	CAP, TA, 4.7UF, +-20%, 25V	807644	2
C73	CAP, CER, 0.05UF, +80-20%, 500V, Z5	105676	1
C74	CAP, POLYES, 0.1UF, +-10%, 50V	649913	1
C75	CAP, POLYES, 0.047UF, +-10%, 50V	820548	1
C80, C81	CAP, POLYES, 0.47UF, +-10%, 50V	697409	2
C82	CAP, CER, 10PF, +-2%, 50V, CG	713875	1
CR1-5, CR7, CR10, CR12-14, CR16, CR20 CR21, CR23-25, CR27, CR29-31, CR61-67	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	27
CR33, CR68	DIODE, SI, N-JFET, CURRENT REG, IF	852116	2
CR53	DIODE, SI, N-JFET, CURRENT REG, IF	334839	1
H1, H2	SCREW, MACH, PH, P, STL, 6-32X.500	152173	2
H3, H4	SCREW, MACH, PH, P, STL, 6-32X.750	114223	2
H10, H48, H59, H60	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	4
H13-16	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
HR8	PWR AMP DC HYBRID	775437	1
K1, K2	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	2
K3, K4	RELAY, ARMATURE, 2 FORM C, 5V, LAT	769307	2
K10-17	RELAY, ARMATURE, 2 FORM C, 5V	733063	8
L1, L2	CHOKE, 6TURN	320911	2
L10	INDUCTOR, 1.5UH, +/-5%, 128 MHZ, S	413856	1
L11	INDUCTOR, 33 UH, +/-10%, 33 MHZ, S	249086	1
L12	CHOKE, 2TURN	417196	1
M17	OSCILLATOR THERMAL COVER	797696	1
MP4	MOLDED COVER, HYBRID, R-NET	775619	1
MP5-8	HEAT DIS, PRESS ON, TO-5	418384	4
MP20-23	SPACER, TRANSISTOR MOUNT, DAP	152207	4
MP43, MP44	EJECTOR, PWB, NYLON	494724	2
MP45-47, MP61-64	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	7
MP49	HEATSINK, POWER AMP	803007	1

Table 6-20. A16 Power Amplifier PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
MP50	SHIELD, HIGH VOLTAGE, REAR	791921	1
MP51-54	INSUL PART, TRANSISTOR, NYL, .4, .	844837	4
MP55	THERMAL INSULATOR, POWER AMP	791988	1
MP56, MP57	POWER AMP CLAMP BAR	803015	2
MP58	AIR DUCT POWER AMP	775601	1
P701, P702	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q1, Q3	TRANSISTOR, SI, N-MOS, 30W, 500V, T	782540	2
Q2	TRANSITOR, SI, N-JFET, UHF/VHF US	851972	1
Q4, Q7, Q32, Q54, Q60, Q62	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	6
Q5	TRANSISTOR, SI, NPN, SM SIGNAL, HI	272930	1
Q6	TRANSISTOR, SI, PNP, SMALL SIGNAL	844993	1
Q8	TRANSISTOR, SI, N-DMOS FET, TO-72	394122	1
Q9, Q16	TRANSISTOR, SI, NPN SMALL SIGNAL	853478	2
Q10	TRANSISTOR, SI, PNP, SMALL SIGNAL	402578	1
Q11	TRANSISTOR, SI, PNP, SWITCHING, TO	831446	1
Q12, Q14	TRANSISTOR, SI, N-DMOS, 400V, TO-3	783753	2
Q13	TRANSISTOR, SI, P-MOS, 500V, TO-92	782508	1
Q15, Q17	TRANSISTOR, SI, P-MOS, POWER, 500V	782482	2
Q31	TRANSISTOR, SI, VMOS, PWR, TO-237,	640516	1
Q33, Q34	TRANSISTOR, SI, N-JFET, LOW IGSS,	707703	2
Q35	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	1
Q38	TRANSISTOR, SI, BV=40V, 40W, TO-22	369660	1
Q39, Q40, Q50, Q51, Q57, Q58	TRANSISTOR, SI, N-DMOS PWR FET, T	782565	6
Q61	TRANSISTOR, SI, PNP, T92	698233	1
R1	RES, CF, 9.1K, +-5%, 0.25W	706663	1
R3, R4, R81-83	RES, MF, 100K, +-0.1%, 0.5W, 50PPM	369371	5
R5	RES, MF, 30.1K, +-1%, 0.125W, 100PP	772061	1
R7	RES, MF, 1.5M, +-1%, 0.125W, 100PPM	714998	1
R8, R86	RES, MF, 10K, +-0.1%, 0.125W, 50PPM	733972	2
R9, R10, R16, R33, R40, R50 R59, R115, R148, R149	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	10
R11, R12	RES, MF, 16.5K, +-1%, 0.5W, 100PPM	162529	2
R13	RES, MF, 17.4K, +-1%, 0.5W, 100PPM	247270	1
R14, R73, R137	RES, CF, 43K, +-5%, 0.25W	821777	3
R15, R19, R52, R57	RES, CC, 68K, +-10%, 1W	109629	4
R17, R53	RES, MF, 4.99K, +-1%, 0.125W, 100PP	721548	2
R18, R23, R54, R56, R89, R90, R134, R13	RES, CF, 10K, +-5%, 0.25W	697102	8
R20	RES, CF, 3.9K.+-5%, 0.25W	810416	1
R22, R109, R133	RES, CF, 430, +-5%, 0.25W	817577	3
R24, R138	RES, CF, 200, +-5%, 0.25W	810390	2
R25	RES, CF, 750, +-5%, 0.25W	810374	1
R26, R116, R129	RES, CF, 4.7K, +-5%, 0.25W	721571	3
R27	RES, CC, 1K, +-5%, 0.5W	108597	1
R30	RES, CF, 330, +-5%, 0.25W	830596	1
R31	RES, CF, 100K, +-5%, 0.25W	658963	1
R32	RES, CF, 3K, +-5%, 0.25W	810366	1
R34, R47	RES, CF, 1M, +-5%, 0.25W	649970	2

Table 6-20. A16 Power Amplifier PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R35, R74, R139	RES, CF, 20, +-5%, 0.25W	810382	3
R36	RES, CF, 47, +-5%, 0.25W	822189	1
R37	RES, CF, 12K, +-5%, 0.25W	757799	1
R38, R118	RES, CF, 47K, +-5%, 0.25W	721787	2
R41, R51, R55	RES, CC, 200K, +-5%, 1W	109926	3
R46, R108, R110-113, R123, R141, R151, R152	RES, CF, 100, +-5%, 0.25W	810465	10
R58	RES, CF, 33, +-5%, 0.25W	631366	1
R61	RES, CF, 750K, +-5%, 0.25W	747543	1
R84	RES, MF, 22.1K, +-1%, 0.125W, 100PP	655266	1
R85	RES, CC, 27M, +-5%, 0.25W	221994	1
R87	RES, MF, 84.5, +-1%, 0.125W, 100PPM	832055	1
R88, R91, R97, R98	RES, MF, 10, +-1%, 0.125W, 100PPM	820399	4
R92	RES JUMPER, 0.02, 0.25W	682575	1
R117	RES, CF, 24K, +-5%, 0.25W	697599	1
R120	RES, CC, 47, +-5%, 0.5W	159608	1
R125	RES, CF, 2K, +-5%, 0.25W	810457	1
R126, R128	RES, CF, 620, +-5%, 0.25W	810408	2
R132	RES, MF, 20K, +-0.1%, 0.25W, 25PPM	810564	1
R142	RES, CF, 200K, +-5%, 0.25W	681841	1
R143	RES, CF, 300K, +-5%, 0.25W	732818	1
R144	RES, CF, 1K, +-5%, 0.25W	780585	1
R145	RES, CF, 1.5K, +-5%, 0.25W	810432	1
R146, R147	RES, CF, 3, +-5%, 0.25W	442079	2
R150	RES, CF, 15, +-5%, 0.25W	641043	1
TP1-5, TP7-13, TP16, TP17	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	14
TP6	SOCKET, SINGLE, PWB, FOR 0.080 PI	170480	1
TP14	SOCKET, SINGLE, PWB, FOR 0.080 PI	149138	1
TP15	SOCKET, SINGLE, PWB, FOR 0.080 PI	149120	1
U1	IC, OP AMP, PRGRBL OUT CURRNT, 8	418913	1
U2, U5	IC, CMOS, QUAD BILATERAL SWITCH	586735	2
U4	IC, OP AMP, LOW NOISE, SELECTED S	807024	1
U7	IC, OP AMP, JFET INPUT, 22V SUPPL	832584	1
U8	IC, CMOS, HEX INVERTER	381848	1
U9	IC, OP AMP, CHOPPER STABLIZED, 8	831263	1
U10	IC, BPLR, FAHRENHEIT TEMPERTURE	845156	1
VR6, VR11, VR19, VR22, VR26, VR28 VR32	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	810267	7
VR15	ZENER, UNCOMP, 18.0V, 5%, 7.0MA, 0.	810325	1
VR18	ZENER, UNCOMP, 15.0V, 5%, 8.5MA, 0.	820415	1
VR51, VR52 VR57, VR58	ZENER, UNCOMP, 6.8V, 5%, 20.0MA, 0.	820431	4
VR61, VR62	ZENER, UNCOMP, 3.3V, 5%, 20.0MA, 0.	820423	2
VR64	ZENER, UNCOMP, 24.0V, 5%, 20MA, 0, 4	810317	1
VR65	ZENER, UNCOMP, 12.0V, 10%, 10.5MA,	741074	1
Z1	RES, NET, THN F. 396K, (2)+-500/5	764399	1

Table 6-21. A16A1 Power Amplifier Digital Control SIP PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C52	CAP, AL, 15UF, +-20%, 35V	614024	1
C53, C56	CAP, CER, 33PF, +-5%, 50V, COG	714543	2
C54	CAP, CER, 470PF, +-10%, 50V, COG	733071	1
C55, C57	CAP, POLYES, 0.22UF, +-5%, 50V	747519	2
L4	CHOKE, 6TURN	320911	1
MP3	HEADER, 2 ROW, 0.100CTR, RT ANG, 1	658112	1
P1, P2	HEADER, 2 ROW, 0.100CTR, RT ANG, 2	512590	2
R101, R105	RES, MF, 1K, +-1%, 0.125W, 100PPM	816595	2
R102	RES, CF, 16K, +-5%, 0.25W	714303	1
R103	RES, CF, 10K, +-5%, 0.25W	697102	1
R104	RES, CF, 4.7K, +-5%, 0.25W	721571	1
U9	IC, LSTTL, 3-8 LINE DCDR W/ENABL	407585	1
U10, U12	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	2
U11	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U13, U15	IC, COMPARATOR, QUAD, 14 PIN DIP	387233	2
U14	IC, CMOS, 8-1 LINE MUX/DEMUX ANA	836304	1
Z1	RES, NET, SIP, 10 PIN, 9 RES, 47K, +	485193	1
Z2	RES, NET, SIP, 10 PIN, 9 RES, 4.7K,	484063	1

Table 6-22. A17 Regulator/Guard Crossing PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C2, C4, C6, C7, C9, C11, C12, C14-17, C19-23 C26-28, C65, C66	CAP, AL, 10UF, +-20%, 63V, SOLV PRO	816843	22
C3, C10, C18, C25	CAP, CER, 0.05UF, +-20%, 100V, Z5V	149161	4
C5, C24, C29, C102	CAP, AL, 22UF, +-20%, 35V, SOLV PRO	851766	4
C8, C13	CAP, TA, 22UF, +-20%, 25V	845149	2
C52, C53	CAP, CER, 15PF, +-20%, 50V, COG	697524	2
C54, C56, C59, C60, C101 C104-107, C109, C110, C112-114	CAP, POLYES, 0.1UF, +-10%, 50V	649913	14
C55, C58	CAP, TA, 10UF, +-20%, 10V	714766	2
C57	CAP, TA, 47UF, +-20%, 10V	733246	1
C61, C62	CAP, CER, 22PF, +-5%, 50V, COG	714550	2
C63, C64	CAP, CER, 100PF, +-2%, 50V, T2J	362665	2
C67-70	CAP, TA, 22UF, +-20%, 25V	357780	4
CR1-34	DIODE, SI, 100 PIV, 1.0 AMP	742874	34
CR35	DIODE, SI, SCHOTTKY BARRIER, SMAL	313247	1
F1	FUSE, SUB MIN, SLOW, 3.15A, 250V, P	832253	1
H19-22	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H45-48	SCREW, MACH, PH, P, STL, 6-32X.500	152173	4
H49-52	HEAT, DIS, ACC, NYL, TO-3	851907	4
H53-60	NUT, CAP EXT LW, STL, 6-32X7/64	152819	8
J801, J802	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
L51	CHOKE, 3 TURN	452888	1
L53, L54	CHOKE, 2TURN	417196	2
MP1, MP5	HEAT DIS, RADIAL FIN, 0.255 ID, 0	104646	2
MP2-4, MP9, MP37	HEAT DIS, PWB MT, .75X.50X.50, TO	816587	5
MP6-8, MP11	HEAT DIS, HORIZ, 1.88X1.40X1.25,	643593	4
MP10	HEAT DIS, SNAP ON, .75, TO-5	853283	1
MP12	HEAT DIS, CLIP, 1.00X1.18X.50, T	643353	1
MP13	HEAT DIS, PRESS ON, TO-5	418384	1
MP14	HEAT DIS, VERTICAL, 1.00X.31X.81	853395	1
MP15-22	SPACER, SWAGED, RND, BRASS, 6-32X	435578	8
MP35, MP36	EJECTOR, PWB, NYLON	494724	2
MP38	AIR DUCT, FILTER ASSY	802884	1
MP39-42	INSUL PART, TRANS, SILICONE, TO-3	473165	4
MP59-62, MP73-76	SPACER, TRANSISTOR MOUNT, DAP	152207	8
MP71, MP72	PAD, ADHESIVE	735365	2
Q1	TRANSISTOR, SI, BV=60V, 65W, T	559989	1
Q2	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	1
R1, R4	RES, MF, 113, +-0.1%, 0.125W, 100PP	484238	2
R2, R8	RES, MF, 2.67K, +-1%, 0.5W, 100PPM	161430	2
R5, R11	RES, MF, 203, +-.1%, .125W, 100PPM	851191	2
R6	RES, MF, 2.61K, +-0.1%, 0.125W, 100	851571	1
R10	RES, MF, 2.67K, +-0.1%, 0.125W, 25P	340596	1
R13	RES, CF, 10, +-5%, 0.25W	572941	1
R14, R18	RES, MF, 150, +-0.1%, 0.125W, 100PP	851279	2
R15, R17	RES, MF, 5.11K, 0.1%, 0.5W,	832378	2
R19	RES, CC, 3K, +-5%, 0.5W	109090	1
R20, R58, R59	RES, CF, 3K, +-5%, 0.25W	573279	3
R52	RES, MF, 1K, +-1%, 0.125W, 100PPM	719468	1
R53	RES, CF, 10M, +-5%, 0.25W	696971	1
R54	RES, CF, 1.8K, +-5%, 0.25W	573220	1
R56	RES, CF, 150, +-5%, 0.25W	573030	1

Table 6-22. A17 Regulator/Guard Crossing PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R57	RES, CF, 100, +-5%, 0.25W	573014	1
R60, R61	THERMISTOR, DISC, POS, 100, +-20%,	851303	2
SW51	SWITCH, PUSHBUTTON, SPST, MOMENTA	782656	1
T51	RF TRANSFORMER, 8 MHZ	813477	1
TP1, TP4, TP6, TP8-10, TP12, TP55 TP58	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	9
U1, U5, U10	IC, VOLT REG, HIGH VOLTAGE	723445	3
U2, U4	IC, VOLT REG, FIXED, +15 VOLTS, 1.	413187	2
U3, U9	IC, VOLT REG, FIXED, -15 VOLTS, 1.	413179	2
U6	IC, VOLT REG, ADJ, POS, LOW DROPOU	851717	1
U7	IC, VOLT REG, ADJ, NEG, LOW DROPOU	851720	1
U8, U11	IC, VOLT REG, FIXED, +5 VOLTS, 1.0	327981	2
U12	IC, VOLT REG, FIXED, -5 VOLTS, 1.5	394551	1
U13	IC, VOLT REG, ADJ, -1.2 TO 47V, TO	845276	1
U51	IC, CMOS, HEX INVERTER, UNBUFFERE	741199	1
U52	IC, CMOS, OCTL LINE DRVR W/3-ST	741892	1
U53, U54	IC, CMOS, 3-8 LINE DECODER/DEMUX	799478	2
U55	IC, CMOS, OCTAL BUS TRANSCEIVER	722017	1
U56	8 BIT MPU, PROGRAMMED 637Y	775270	1
U57	IC, TTL, DUAL AND DRVR W/OPEN CO	393959	1
U58	IC, CMOS, PROG LOGIC, 35NS, 5700A-	845263	1
U59, U63	IC, CMOS, 14 STAGE BINARY COUNTE	807701	2
U60	IC, VOLT SUPERVISORS, 10V SENSE	780577	1
U62	IC, CMOS, 8K X 8 STAT RAM, 120 NS	783332	1
VR1, VR3	ZENER, UNCOMP, 43V, 5%, 30MA, 0.5W	851584	2
VR2, VR4	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	698696	2
VR5, VR6	ZENER, UNCOMP, 5.6V, 5%, 220.0MA, 5	454553	2
X1	SOCKET, IC, 24 PIN	812198	1
X2	SOCKET, IC, 0.070 CTR, 64 PIN	783688	1
X3	SOCKET, IC, 28 PIN	448217	1
Y51	CRYSTAL, 4.9152 MHZ, +/- 0.005%,	800367	1
Y52	CRYSTAL, 8.00MHZ QUARTZ HC-18U	707133	1
Z1, Z3	RES, NET, SIP, 8 PIN, 4 RES, 10K, +-	513309	2
Z2	RES, NET, SIP, 10 PIN, 5 RES, 10K, +	529990	1
Z51	RES, NET, DIP, 16 PIN, 15 RES, 10K,	355305	1
Z52	RES, NET, SIP, 8 PIN, 4 RES, 4.7K, +	573881	1
Z53, Z54	RES, NET, SIP, 10PIN, 5RES, 33	622761	2

Table 6-23. A18 Filter/PA Supply PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C10, C17	CAP, POLYES, 0.22UF, +-5%, 50V	747519	3
C2, C3	CAP, AL, 6800UF, +30-20%, 25V, SOLV	782466	2
C4, C6	CAP, AL, 1000UF, +-20%, 50V, SOLV P	782391	2
C5, C19	CAP, AL, 2200UF, +-20%, 25V, SOLV P	782383	2
C7-9, C18	CAP, AL, 330UF, +-20%, 100V, SOLV P	816785	4
C11	CAP, AL, 220UF, +-20%, 25V, SOLV PR	816793	1
C12, C22	CAP, AL, 22UF, +-20%, 35V, SOLV PRO	817056	2
C13-16	CAP, AL, 3300UF, +30-20%, 50V, SOLV	782458	4
C20	CAP, AL, 10UF, +-20%, 63V, SOLV PRO	816843	1
C21	CAP, AL, 470UF, +-20%, 50V, SOLV PR	747493	1
C23, C209, C210	CAP, POLYES, 1.0UF, +-10%, 50V	733089	3
C201, C203, C204, C206	CAP, AL, 47UF, +-20%, 400V, SOLV PR	782532	4
C202, C205	CAP, AL, 3.3UF, +30-20%, 450V, SOLV	782524	2
C207, C208	CAP, AL, 100UF, +-20%, 16V, SOLV PR	816850	2
C211, C212	CAP, CER, 100PF, +-5%, 50V, CG	831495	2
CR1, CR2, CR4, CR5	DIODE, SI, 50 PIV, 3.0 AMP	403055	4
CR3, CR14	DIODE, SI, RECT, BRIDGE, BV=100V, I	392910	2
CR6, CR7	DIODE, SI, RECT, BRIDGE, BV=200V, I	296509	2
CR8, CR10, CR12, CR13	DIODE, SI, 100 PIV, 3.0 AMPS	816363	4
CR9, CR16, CR18	DIODE, SI, 100 PIV, 1.0 AMP	742874	3
CR11, CR15, CR17	DIODE, SI, RECT, BRIDGE, BV= 50V, I	586115	3
CR19	THYRISTOR, SI, TRIAC, VBO=200V, 8.	413013	1
CR201, CR203, CR208, CR210, CR234, CR235, CR239, CR243	DIODE, SI, 400 PIV, 1 AMP	831586	8
CR205, CR217, CR218, CR220, CR221, CR223, CR224, CR227, CR228, CR240, CR247, CR248	DIODE, SI, 1K PIV, 1.0 AMP	707075	12
CR209, CR236	DIODE, SI, N-JFET, CURRENT REG, IF	334839	2
CR222	DIODE, SI, RECT, BRIDGE, BV=800V, I	341016	1
CR244, CR251	DIODE, SI, BV= 75.0V, RADIAL INSE	659516	2
F1, F2, F8	FUSE, SUB-MIN, SLOW, 1.6A, 250V, PI	816488	3
F3-5, F7, F9	FUSE, SUB-MIN, SLOW, 0.5A, 250V, PI	831990	5
F6, F201-204	FUSE, SUB MIN, SLOW, 0.315A, 250V,	832337	5
H6-9	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
H13-16	WASHER, LOCK, INTRNL, STEEL, #4	110403	4
J201, J202	JUMPER, REC, 2 POS, .100CTR, .025	757294	2
K201	RELAY, ARMATURE, 2 FORM C, 5V	733063	1
MP3	HEAT DIS, RADIAL FIN, 0.255 ID, 0	104646	1
MP4, MP5	EJECTOR, PWB, NYLON	494724	2
MP10-13	SPACER, TRANSISTOR MOUNT, DAP	152207	4
MP201, MP202	HEADER, 1 ROW, 0.100CTR, 2 PIN	643916	2
MP203-206	HEAT DIS, VERT, 1.00X1.50X.375,	816546	4
MP207-210	INSUL PART, TRANS, SILICONE, POWE	534453	4
MP211-214	WASHER, SHOULDER, TEF, .115, .200	844824	4
MP215-218	SCREW, MACH, PH, P, STL, 4-40X.250	129890	4
MP219-222	NUT, MACH, HEX, STL, 4-40	110635	5
P901, P902	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
Q201, Q202	TRANSISTOR, SI, N-MOS, 30W, 500V, T	782540	2

Table 6-23. A18 Filter/PA Supply PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
Q203, Q206	TRANSISTOR, SI, PNP, SM SIG, SELEC	650846	2
Q204, Q209, Q210 Q212	TRANSISTOR, SI, P-MOS, 500V, TO-92	782508	4
Q205, Q207, Q208 Q213	TRANSISTOR, SI, N-DMOS, 500V, TO-9	782490	4
Q211, Q214	TRANSISTOR, SI, NPN, SMALL SIGNAL	335067	2
Q215, Q216	TRANSISTOR, SI, P-MOS, POWER, 500V	782482	2
Q217, Q218	TRANSISTOR, SI, NPN, SMALL SIGNAL	698225	2
Q219	TRANSISTOR, SI, PNP, T92	698233	1
R1	RES, CC, 560, +-5%, 1W	266361	1
R2-5	RES, CC, 20K, +-5%, 0.5W	109041	4
R201, R244	RES, CF, 8.2, +-5%, 0.25W	442269	2
R202, R243	RES, CF, 5.6, +-5%, 0.25W	572917	2
R203, R241	RES, CF, 9.1K, +-5%, 0.25W	706663	2
R204, R253	RES, CF, 1.5, +-5%, 0.25W	732800	2
R205, R216, R229, R240	RES, CC, 560K, +-10%, 0.5W	108795	4
R206, R239	RES, CF, 1M, +-5%, 0.25W	649970	2
R207, R209, R237, R238	RES, CF, 3K, +-5%, 0.25W	810366	4
R208, R210, R235, R236	RES, CC, 100K, +-5%, 1W	641282	4
R211	RES, CF, 47, +-5%, 0.25W	822189	1
R212, R220, R222, R231, R242	RES, CF, 33K, +-5%, 0.25W	733667	5
R213, R217, R218, R230, R232, R245, R249	RES, CF, 10K, +-5%, 0.25W	697102	7
R214, R233	RES, CF, 200K, +-5%, 0.25W	681841	2
R215, R234	RES, CC, 330, +-10%, 0.5W	108589	2
R221, R250	RES, CF, 82K, +-5%, 0.25W	655027	2
R225	RES, CF, 100K, +-5%, 0.25W	573584	1
R226, R248	RES, MF, 3.16K, +-1%, 0.125W, 100PP	235291	2
R228, R247	RES, CF, 100K, +-5%, 0.25W	658963	2
R246, R251	RES, CF, 4.7K, +-5%, 0.25W	721571	2
R252	RES, CF, 300K, +-5%, 0.25W	732818	1
R254, R255	RES, CC, 27, +-5%, 0.5W	260984	2
RT1, RT2	THERMISTOR, DISC, POSITIVE, 50, +-	816140	2
S201	SWITCH, SLIDE, DPDT	436691	1
TP1-22, TP203 TP205-212	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	31
TP201	SOCKET, SINGLE, PWB, FOR 0.080 PI	170480	1
TP204	SOCKET, SINGLE, PWB, FOR 0.080 PI	149120	1
U1	IC, VOLT REG, FIXED, -5 VOLTS, 0.	816322	1
U2	IC, VOLT REG, FIXED, +5 VOLTS, 0.1	816355	1

Table 6-23. A18 Filter/PA Supply PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U3	IC, VOLT REG, FIXED, -18 VOLTS, 1.	845474	1
U201	IC, COMPARATOR, QUAD, 14 PIN DIP	387233	1
VR20, VR21	ZENER, UNCOMP, 82.0V, 5%, 1.5MA, 0.	853481	2
VR202, VR213, VR233, VR242	ZENER, UNCOMP, 10.0V, 5%, 12.5MA, 0	810267	4
VR206, VR207, VR218, VR228, VR237, VR238	ZENER, UNCOMP, 10.0V, 5%, 20.0MA, 0	820480	6
VR211, VR217, VR227, VR231	ZENER, UNCOMP, 140.0V, 5%, 1.8MA, 1	340703	4
VR212, VR232	ZENER, UNCOMP, 190V, 2%, 0.66MA, 0.	853424	2
VR214, VR230, VR246, VR247	ZENER, UNCOMP, 56.OV, 5%, 2.2MA, 0.	832568	4
VR215, VR219, VR225, VR229	ZENER, UNCOMP, 200.0V, 5%, 5.0MA, 5	386839	4
VR216, VR226	ZENER, UNCOMP, 180V, 2%, 0.68MA, 0.	816348	2
VR245	ZENER, UNCOMP, 3.3V, 5%, 20.0MA, 0.	820423	1
Z1-3	RES, NET, SIP, 10 PIN, 5 RES, 10K, +	529990	3
Z201	RES, NET, SIP, 6 PIN, 5 RES, 100K, +	412726	1

Table 6-24. A19 Digital Power Supply PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1	CAP, AL, 470UF, +-20%, 160V, SOLV P	816835	1
C2	CAP, AL, 10UF, +-20%, 160V, SOLV PR	817064	1
C3	CAP, AL, 330UF, +-20%, 100V, SOLV P	816785	1
C4, C9	CAP, AL, 10UF, +-20%, 63V, SOLV PRO	816843	2
C5, C11	CAP, CER, 0.10UF, +-20%, 50V, X7R	853650	2
C6	CAP, AL, 10000UF, +-20%, 25V, SOLV	816819	1
C7	CAP, AL, 6800UF, +30-20%, 25V, SOLV	782466	1
C8	CAP, AL, 2.2UF, +-20%, 50V, SOLV PR	816868	1
C10	CAP, AL, 22UF, +-20%, 35V, SOLV PRO	817056	1
C12, C13	CAP, AL, 22000UF, +-20%, 16V, SOLV	822379	2
C14, C16, C19-23	CAP, CER, 0.22UF, +-20%, 50V, X7R	853648	7
C15	CAP, AL, 100UF, +-20%, 16V, SOLV PR	816850	1
C17	CAP, POLYPR, 0.047UF, +-10%, 630V	500827	1
C18	CAP, POLYPR, 0.047UF, +-10%, 160V	446773	1
C24, C25	CAP, CER, 0.022UF, +80-20%, 500V, Z	740340	2
CR1-4, CR9-12	DIODE, SI, 200 PIV, 1.0 AMP	851964	8
CR8, CR16, CR21-24, CR29-34	DIODE, SI, 100 PIV, 1.0 AMP	742874	12
CR13	DIODE, N-JFET, CURRENT REG, IF=3.	852137	1
CR17-20	DIODE, SI, 50 PIV, 1.0 AMP	851951	4
CR25-28	DIODE, SI, 50 PIV, 3.0 AMP	403055	4
CR35	DIODE, GER, BV=66 V, IO=50MA	180505	1
F1	FUSE, SUB MIN, SLOW, 0.315A, 250V,	832337	1
F2	FUSE, SUB MIN, SLOW, 0.125A, 250V,	832261	1
F3, F4	FUSE, SUB-MIN, SLOW, 2A, 250V, PIGT	806331	2
F5	FUSE, SUB MIN, SLOW, 3.15A, 250V, P	832253	1
H2, H11	SCREW, MACH, PH, P, STL, 4-40X.375	152124	2
H3, H4	HEAT DIS, CLIP, 1.00X1.18X.50, T	643353	2
H5	HEAT DIS, VERTICAL FINS, TO-3	342675	1
H6, H7	RIVET, S-TUB, OVAL, STL, .087, .343	838458	2
H9, H10	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	2
L1-6	CHOKE, 6TURN	320911	6
L7	INDUCTOR, 33UH	813485	1
L8	TRANSFORMER, PULSE	660589	1
M1, M2	FOOT, ADHESIVE, RUBBER, GREY, .44X	358341	2
MP8, MP27	NUT, MACH, HEX, STL, 4-40	110635	2
MP9, MP10	NUT, CAP EXT LW, STL, 6-32X7/64	152819	2
MP11, MP12	GROMMET, SLOT, RUBBER, .250, .437	853291	2
MP13, MP14	EJECTOR, PWB, NYLON	494724	2
MP15, MP26	HEAT DIS, VERT, 1.00X1.375X.50,	831099	2
MP16	HEAT, DIS, ACC, NYL, TO-3	851907	1
MP21-23	INSUL PART, TRANS, SILICONE, POWE	534453	3
MP24	INSUL PART, TRANS, SILICONE, TO-3	473165	1
MP25	SPACER, TRANSISTOR MOUNT, DAP	152207	1
MP28, MP29	SCREW, MACH, MAG, PH, P, SS, 6-32, .2	772236	2
MP30, MP31	SPACER, SWAGED, RND, BRASS, 6-32X	435578	2
P41	CONN, DIN41612, TYPE C, RT ANG, 64	807800	1
Q1	TRANSISTOR, SI, BV=200V, 80W, TO-3	261347	1
Q2, Q6	TRANSISTOR, SI, NPN, HI-VOLTAGE	370684	2
Q3, Q7-10	TRANSISTOR, SI, BV=300V, 10W, TO-	381731	5
Q4	TRANSISTOR, SI, VB=200V, 10W, TO-5	276899	1
Q5	TRANSISTOR, SI, BV= 60V, 65W, TO-	386128	1
R1	RES, CF, 5.1, +-5%, 0.25W	640995	1
R2	RES, CF, 2K, +-5%, 0.25W	573238	1
R3, R12	RES, CF, 100K, +-5%, 0.25W	573584	2
R4	RES, CC, 4.7K, +-5%, 0.25W	148072	1
R5	RES, CF, 12, +-5%, 0.25W	442178	1

Table 6-24. A19 Digital Power Supply PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
R6	RES, CC, 10K, +-10%, 2W	110106	1
R7	RES, CC, 2, +-5%, 0.5W	218735	1
R8	RES, CF, 120K, +-5%, 0.25W	573592	1
R9, R11	RES, CF, 33K, +-5%, 0.25W	573485	2
R10	RES, CF, 51K, +-5%, 0.25W	573535	1
R13	RES, CC, 10K, +-5%, 0.25W	148106	1
TP1-5, TP8, TP10, TP12, TP13	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	9
U1	IC, VOLT REG, FIXED, +12 VOLTS, 1.	413195	1
U2	IC, VOLT REG, FIXED, -12 VOLTS, 1.	381665	1
U3	IC, VOLT REG, FIXED, 5 VOLTS, 2 AM	816918	1
VR5	ZENER, UNCOMP, 6.2V, 5%, 20.0MA, 0.	698662	1
VR6	ZENER, UNCOMP, 36.0V, 5%, 3.4MA, 0.	186163	1
VR7	ZENER, UNCOMP, 39.0V, 5%, 3.2MA, 0.	831248	1
VR14, VR15	ZENER, UNCOMP, 18.0V, 5%, 7.0MA, 0,	327973	2

Table 6-25. A20 CPU PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
BT1	BATTERY, LITHIUM, 3.0V, 0.500AH	821439	1
C1	CAP, TA, 220UF, +-20%, 10V	474288	1
C2-4, C6, C101-106, C108-111, C113, C115-120, C122-133, C143-145, C152	CAP, POLYES, 0.1UF, +-10%, 50V	649913	37
C5	CAP, TA, 22UF, +-20%, 10V	658971	1
C8-11	CAP, CER, 22PF, +-2%, 50V, COG	714832	4
C12, C13	CAP, POLYES, 0.22UF, +-10%, 50V	706028	2
C17	CAP, AL, 47UF, +-20%, 35V, SOLV PRO	643312	1
C80	CAP, CER, 0.22UF, +80-20%, 50V, Z5U	649939	1
C81, C82	CAP, CER, 120PF, +-5%, 50V, COG	721142	2
C100	CAP, TA, 2.2UF, +-20%, 16V	706804	1
CR1	LED, RED, T1/T1-3/4	723486	1
CR2, CR3, CR7	DIODE, SI, 100 PIV, 1.0 AMP	742874	3
CR4-6, CR8	DIODE, SI, SCHOTTKY BARRIER, SMAL	313247	4
H3-6	RIVET, S-TUB, OVAL, STL, .087, .343	838458	4
L80, L81	CHOKE, 3 TURN	452888	2
M3, M4	FOOT, ADHESIVE, RUBBER, GREY, .44X	358341	2
MP1, MP2	EJECTOR, PWB, NYLON	494724	2
MP7	PAD, ADHESIVE	735365	1
MP8	PAD, ADHESIVE	735365	1
P61, P62	CONN, DIN41612, TYPE C, RT ANG, 64	807800	2
R1, R3	RES, CF, 360, +-5%, 0.25W	573097	2
R4	RES, CF, 10M, +-5%, 0.25W	696971	1
R5	RES, CF, 1.8K, +-5%, 0.25W	573220	1
R6	RES, CF, 6.2K, +-5%, 0.25W	573345	1
R51-54	RES, MF, 5.11K, +-1%, 0.125W, 100PP	720342	4
R55	RES, MF, 10K, +-1%, 0.125W, 100PPM	719476	1
R56, R57	RES, MF, 1K, +-1%, 0.125W, 50PPM	320333	2
R58, R59	RES, MF, 39.2K, +-1%, 0.125W, 25PPM	312207	2
R60, R61	RES, MF, 1M, +-1%, 0.125W, 100PPM	719492	2
R80, R81	RES, CF, 100, +-5%, 0.25W	573014	2
R82	RES, CF, 150, +-5%, 0.25W	573030	1
SW1	SWITCH, PUSHBUTTON, SPST, MOMENTA	782656	1
T51	RF TRANSFORMER, 8 MHZ	813477	1
TP1, TP3-12	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	11
U1	IC, VOLT SUPERVISORS, 10V SENSE	780577	1
U2	IC, LSTTL, HEX INVERTER W/OPEN C	394536	1
U3	IC, CMOS, HEX INVERTER, UNBUFFERE	741199	1
U4, U11	IC, CMOS, 14 STAGE BINARY COUNTE	807701	2
U5	IC, CMOS, PROG LOG, 35NS, 5700A-90	845271	1
U6	IC, CMOS, PROG LOGIC, 25NS, 5700A-	845250	1
U8	IC, CMOS, 16 BIT MPU, 8 MHZ, DIP	816926	1
U9	IC, CMOS, QUAD 2 INPUT OR GATE	817312	1
U10	IC, CMOS, PROG LOGIC, 35NS, 5700A-	845268	1
U13	IC, NMOS, 32K X 8 EEPROM, 200N	817270	1
U15	EPROM, PROGRAMMED 27010, U15	761262	1
U16	EPROM, PROGRAMMED 27010, U16	761361	1
U17	EPROM, PROGRAMMED 27010, U17	761379	1
U18	EPROM, PROGRAMMED 27010, U18	775247	1
U19-22	IC, CMOS, 32K X 8 STATIC RAM, 120	800250	4
U25, U27-29	IC, CMOS, OCTL LINE DRVR W/3-ST	741892	4
U26, U30	IC, CMOS, OCTAL BUS TRANSCEIVER	722017	2
U31	IC, CMOS, DUAL CHANNEL UART (DUA	799494	1
U32	IC, TTL, DUAL AND DRVR W/OPEN CO	393959	1
U33	IC, CMOS, CLOCK CALNDR, SEL TRD, T	845193	1

Table 6-25. A20 CPU PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U52	IC, OP AMP, QUAD, 14 PIN DIP	402669	1
X5, X6, X10	SOCKET, IC, 24 PIN	812198	3
X8	SOCKET, IC, 64 PIN	483842	1
X13	SOCKET, IC, 28 PIN	448217	1
X15-22	SOCKET, IC, 32 PIN	807156	8
Y1	CRYSTAL, 7.3728MHZ, +-1, %, HC-18U	742049	1
Y3	CRYSTAL, 32.768KHZ, +-5PPM	811943	1
Z1	RES, NET, DIP, 16PIN, 15RES, 3.3K, +	837666	1
Z2, Z3	RES, NET, DIP, 16 PIN, 15 RES, 4.7K	416834	2
Z4	RES, NET, SIP, 10 PIN, 5 RES, 10K, +	529990	1
Z5	RES, NET, DIP, 14 PIN, 13 RES, 100K	404624	1

Table 6-26. A21 Rear Panel PCA

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
C1, C3, C5	CAP, CER, 330PF, +-5%, 50V, COG	697441	3
C4, C21, C22 C24-32, C34, C36, C37, C40-45, C48, C49	CAP, POLYES, 0.1UF, +-10%, 50V	649913	23
C6, C7	CAP, CER, 0.22UF, +80-20%, 50V, Z5U	649939	2
C8	CAP, CER, 4700PF, +-20%, 100V, X7R	362871	1
C9	CAP, CER, 470PF, +-10%, 50V, COG	733071	1
C10, C70	CAP, TA, 68UF, +-20%, 15V	193615	2
C11-15	CAP, TA, 10UF, +-20%, 25V	714774	5
C33	CAP, TA, 39UF, +-20%, 20V	358234	1
C46, C50	CAP, TA, 1UF, +-20%, 35V	697417	2
C47	CAP, CER, 33PF, +-2%, 50V, COG	715292	1
CR1, CR2	DIODE, SI, BV= 75.0V, IO=150MA, 50	698720	2
CR3, CR4	DIODE, SI, BV=75V, IO=150MA, 500MW	203323	2
J1	CONN, MICRO-RIBBON, REC, PWB, 24 P	851675	1
J2	CONN, D-SUB, PWB, 25 PIN	845214	1
J3	CONN, D-SUB, PWB, 15 SCKT	837336	1
J4	CONN, D-SUB, PWB, 15 PIN	837328	1
J5, J6	CONN, COAX, BNC(F), PWB	479162	2
J7	CONN, D-SUB, PWB, 4 CAVITY, 32 SCK	810846	1
J8	HEADER, 2 ROW, 0.100CTR, 40 PIN	807453	1
J9	HEADER, 2 ROW, 0.100CTR, 34 PIN	807446	1
J10	HEADER, 1 ROW, 0.100CTR, 4 PIN	631184	1
J11, J12	HEADER, 1 ROW, .100CTR, 3 PIN	837351	2
K1, K4, K5, K7-12	RELAY, ARMATURE, 2 FORM C, 5V	733063	9
K2, K3, K6	RELAY, ARMATURE, 4 FORM C, 5V, LAT	715078	3
L1	CHOKE, 6TURN	320911	1
MP1, MP2	SPACER, SWAGED, RND, BRASS, 6-32X	261727	2
MP3-10	SPACER, SWAGED, RND, BRASS, 4-40X	385310	8
MP21, MP22	SPACER, SWAGED, RND, BRASS, 6-32X	423806	2
Q1, Q2	TRANSISTOR, SI, N-CHAN, TO-92, SWI	832139	2
R1	RES, MF, 1K, +-1%, 0.125W, 100PPM	719468	1
R2	RES, MF, 332, +-1%, 0.125W, 100PPM	192898	1
R3, R7, R10, R14	RES, CF, 1K, +-5%, 0.25W	573170	4
R4, R5, R12, R13, R16, R17	RES, CF, 10K, +-5%, 0.25W	573394	6
R6	RES, CF, 15K, +-5%, 0.25W	573428	1
R8, R9, R18, R19	RES, CF, 200, +-5%, 0.25W	573055	4
R11	RES, CC, 1K, +-10%, 1W	109371	1
S1	SWITCH, SLIDE, SPDT, LOW PROFILE	810887	1
TP1-15	JUMPER, WIRE, NONINSUL, 0.200CTR	816090	15
U1	IC, CMOS, OCTAL BUS TRANSCEIVER	722017	1
U2	IC, NMOS, GPIB ADAPTER	585240	1
U3	IC, LSTTL, OCTAL GPIB XCVR W/OPE	585224	1
U4	IC, LSTTL, OCTAL IEEE-488 BUS TR	686022	1
U5	IC, CMOS, DUAL CHANNEL UART (DUA	799494	1
U6	IC, TTL, QUAD RS232C LINE DRIVER	414052	1
U7	IC, TTL, QUAD RS232C LINE RECEIV	524850	1
U8	IC, CMOS, PROG LOGIC, 35NS, 5700A-	845255	1
U9, U10	IC, CMOS, OCTL D F/F W/3-STATE, +	585364	2
U11, U12	IC, CMOS, OCTL LINE DRVR W/3-ST	741892	2
U13	IC, OP AMP, JFET INPUT, 22V SUPPL	832584	1
U14	IC, CMOS, PROGRMBL PERIPHERAL IN	780650	1
U16, U17	IC, BIMOS, 8 CHNL HI-VOLT DRVR W	782912	2

Table 6-26. A21 Rear Panel PCA (cont.)

REF DESIGNATOR	DESCRIPTION	FLUKE PART NO.	QTY.
U18	IC, COMPARATOR, HI-SPEED, 14 PIN	647115	1
VR1, VR2	ZENER, UNCOMP, 3.3V, 10%, 20.0MA, 0	698647	2
VR3	ZENER, UNCOMP, 4.7V, 10%, 20.0MA, 0	387084	1
W1	CABLE, BOOST, B-OUT HI	802827	1
W2	CABLE, BOOST B-SENSE HI	802850	1
W3	CABLE, BOOST HIGH VOLTAGE	802843	1
X2, X5	SOCKET, IC, 40 PIN	429282	2
X4, X16, X17	SOCKET, IC, 22 PIN	453126	3
X8	SOCKET, IC, 24 PIN	812198	1
Z1, Z2	RES, NET, SIP, 10 PIN, 9 RES, 4.7K,	484063	2
Z4	RES, NET, SIP, 6 PIN, 5 RES, 4.7K, +	494690	1
Z5	RES, NET, SIP, 6 PIN, 5 RES, 10K, +-	500876	1

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CH-8027 Zurich, Switzerland
Tel 488221

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(For Philips products)
Rue Fardoss 79
B P 2442 Damascus
Tel 221650

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(For Fluke products)
5th Floor, Cathay Min-Sheng
Commercial Building
344 Min-Sheng East Road
Taipei, Taiwan, R O C
Tel 5013468

Yung Kang Trading Co Ltd
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11th Floor CTS Building
102 Kuang Fu South Road
P O Box 1467
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Dar es Salaam
Tel 29571

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(For Fluke products)
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Bangkok, 10240 Thailand
Tel 3742516

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of Thailand Ltd
(For Philips products)
Electronic and Communication
Systems Dept
283 Silom Road
P O Box 961
Bangkok 10
Tel 233-63330/9

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Necatiby Cad 92/3
Karakoy, Istanbul, Turkey
Tel 441546

Turk Philips Ticaret A S
(For Philips products)
Posta Kutusu 504
Beykoglu Istanbul
Tel 1435910

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Philips Middle East b v
(For Philips products)
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Level 11
P O Box 6269
Dubai
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Libertad 2529
Montevideo, Uruguay
Tel 789015

Industrias Philips del Uruguay
(For Philips products)
Avda Uruguay 1287
Casilla de Correo 294
Montevideo
Tel 915641

Venezuela
Coasin C A
(For Fluke products)
Calle 9 Con Calle 4
Edif Edinurbi
Apartado de Correos Nr-70-136
Los Ruices
Caracas 1070-A Venezuela
Tel 241-0309

Industias Venezolanas
Philips S A
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Apartado Postal 1167
Caracas
Tel 239-3811

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Kinshasa
Tel 31693

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Philips Electrica Zambia Ltd
(For Philips products)
Mwembeshi Road
P O Box 31878
Lusaka
Tel 218511

Zimbabwe
Philips Electric (Pvt) Ltd
(For Philips products)
P O Box 994
62 Umtali Road
Beverley Harare
Tel 47211

Section 7
Schematic Diagrams

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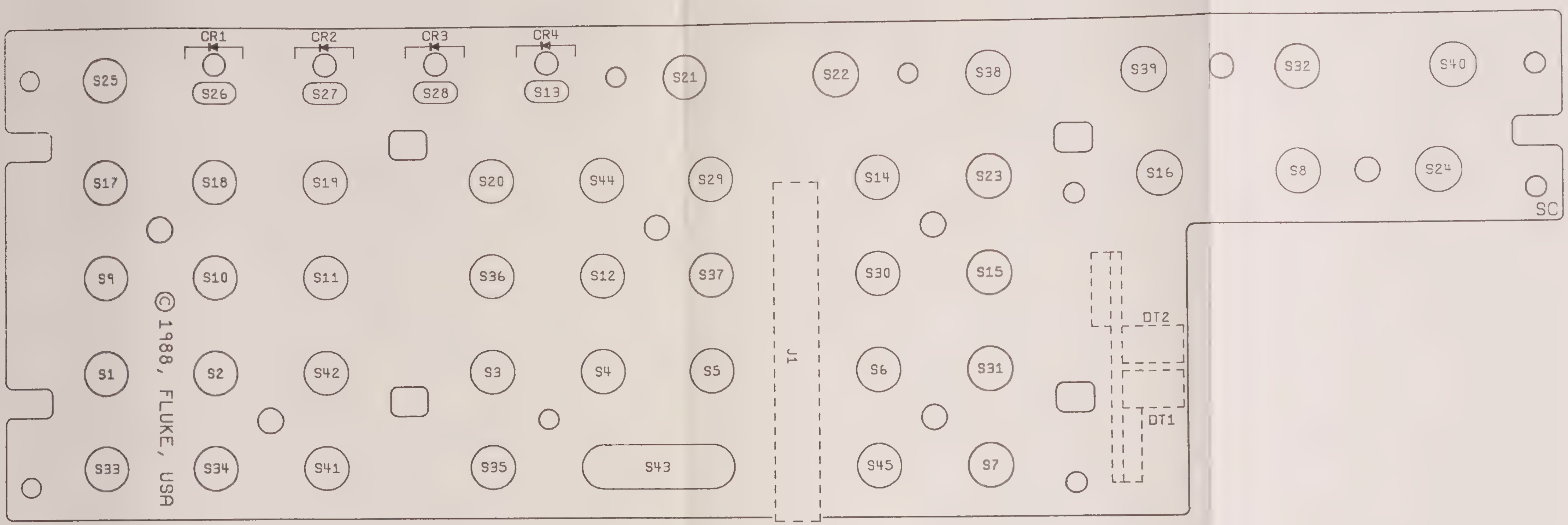

CR1
CR2
CR3
CR4
S25
S26
S27
S28
S13
S21
S22
S38
S39
S32
S40
S17
S18
S19
S20
S44
S29
S14
S23
S16
S8
S24
SC
S9
S10
S11
S36
S12
S37
S30
S15
DT2
S1
S2
S42
S3
S4
S5
J1
S6
S31
DT1
S33
S34
S41
S35
S43
S45
S7
© 1988, FLUKE, USA

Figure 7-1. A1 Keyboard Assembly

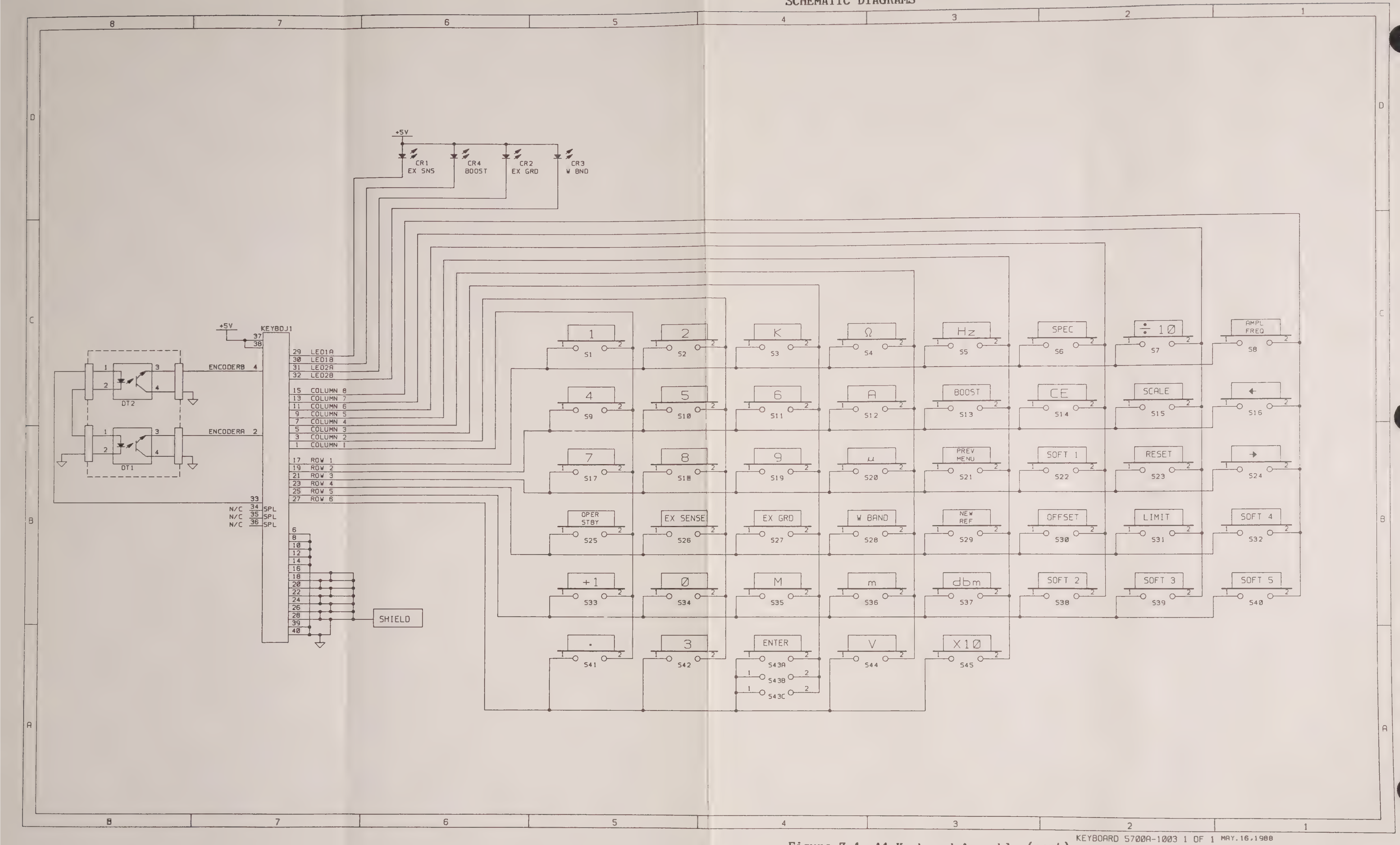

+5V
CR1
EX SNS
CR4
BOOST
CR2
EX GRD
CR3
W BND
+5V
KEYBDJ1
37
38
ENCODERB 4
ENCODERA 2
DT2
DT1
29 LED1A
30 LED1B
31 LED2A
32 LED2B
15 COLUMN 8
13 COLUMN 7
11 COLUMN 6
9 COLUMN 5
7 COLUMN 4
5 COLUMN 3
3 COLUMN 2
1 COLUMN 1
17 ROW 1
19 ROW 2
21 ROW 3
23 ROW 4
25 ROW 5
27 ROW 6
33
N/C 34 SPL
N/C 35 SPL
N/C 36 SPL
6
8
10
12
14
16
18
20
22
24
26
28
39
40
SHIELD
1 S1
2 S2
K S3
Ω S4
Hz S5
SPEC S6
÷ 10 S7
AMPL FREQ S8
4 S9
5 S10
6 S11
A S12
BOOST S13
CE S14
SCALE S15
← S16
7 S17
8 S18
9 S19
μ S20
PREV MENU S21
SOFT 1 S22
RESET S23
→ S24
OPER STBY S25
EX SENSE S26
EX GRD S27
W BAND S28
NEW REF S29
OFFSET S30
LIMIT S31
SOFT 4 S32
+1 S33
0 S34
M S35
m S36
dbm S37
SOFT 2 S38
SOFT 3 S39
SOFT 5 S40
. S41
3 S42
ENTER S43A
S43B
S43C
V S44
X10 S45
A
B
C
D
1
2
3
4
5
6
7
8
KEYBOARD 5700A-1003 1 OF 1 MAY.16,1988

Figure 7-1. A1 Keyboard Assembly (cont)

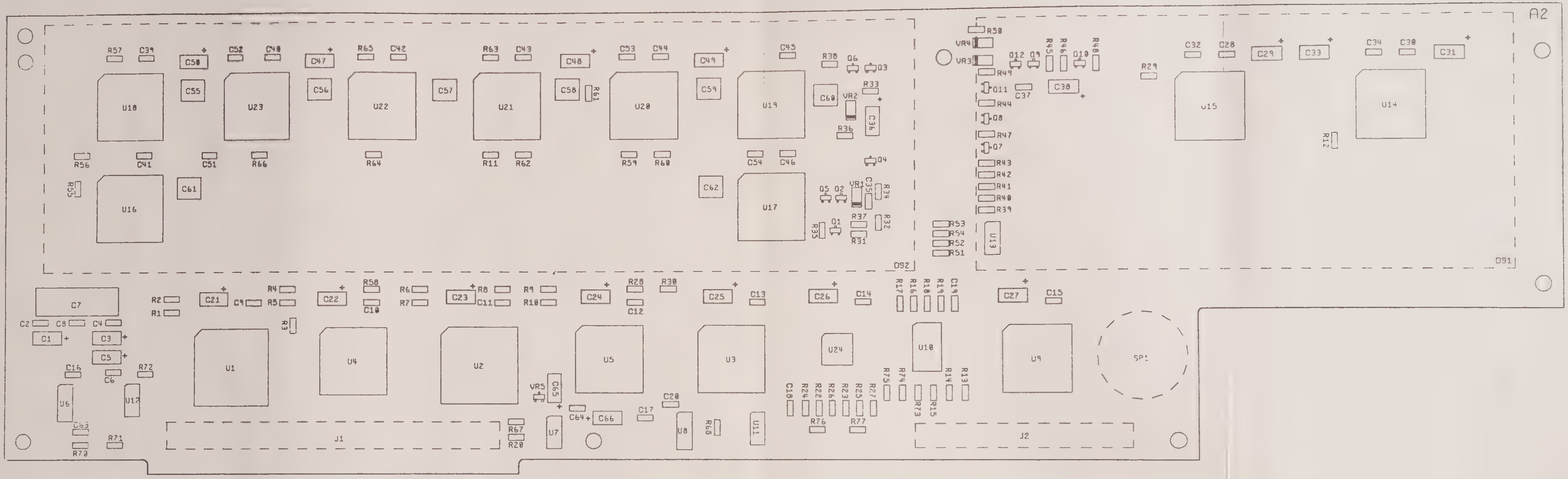
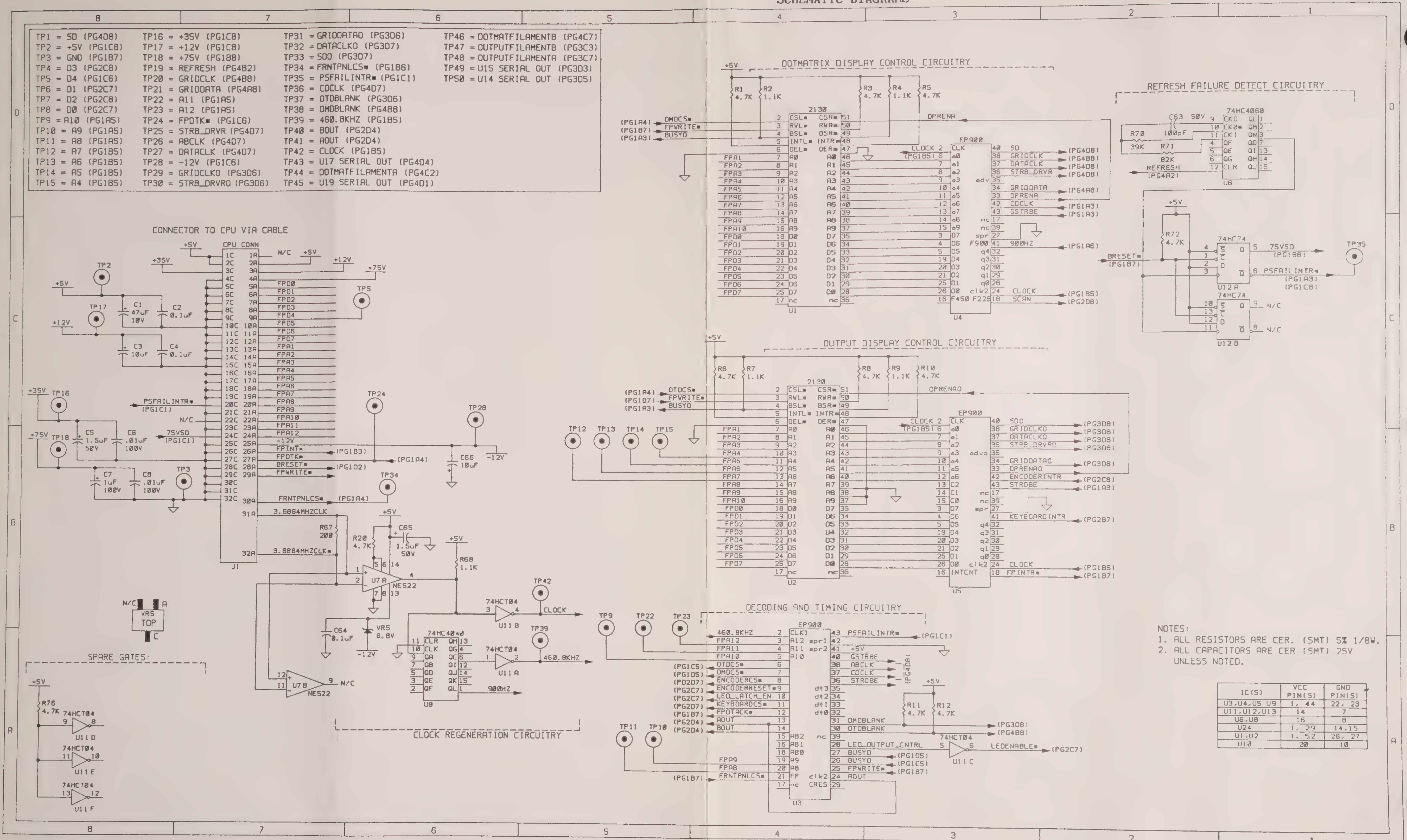

A2
R57
C39
C50
C52
C40
C47
R65
C42
R63
C43
C48
C53
C44
C49
C45
R38
Q6
Q3
R58
VR4
VR3
Q12
Q9
R45
R46
Q10
R48
R29
C32
C28
C29
C33
C34
C30
C31
C55
C56
C57
C58
R61
C59
R33
C60
VR2
C36
R36
R49
Q11
C37
C38
R44
Q8
R47
Q7
U18
U23
U22
U21
U20
U19
U15
U14
R12
R56
C41
C51
R66
R64
R11
R62
R59
R60
C54
C46
Q4
R55
C61
C62
Q5
Q2
VR1
C35
R34
R43
R42
R41
R40
R39
U16
U17
R37
R32
R35
Q1
R31
R53
R54
R52
R51
U13
D92
D91
C7
R2
R1
C21
C9
R4
R5
C22
R58
C10
R6
R7
C23
R8
C11
R9
R10
C24
R28
C12
R30
C25
C13
C26
C14
R17
R16
R18
R19
C19
C27
C15
C2
C8
C4
C1
C3
R3
C5
C16
C6
R72
U1
U4
U2
U5
U3
U24
U10
U9
SP1
U6
U12
C63
R70
R71
J1
VR5
C65
C64
C66
C17
C20
R67
R20
U7
U8
R68
U11
C18
R24
R22
R26
R23
R25
R27
R75
R74
R73
R14
R15
R13
R76
R77
J2

Figure 7-2. A2 Front Panel PCA


DOTMATRIX DISPLAY CONTROL CIRCUITRY
REFRESH FAILURE DETECT CIRCUITRY
OUTPUT DISPLAY CONTROL CIRCUITRY
DECODING AND TIMING CIRCUITRY
CLOCK REGENERATION CIRCUITRY
CONNECTOR TO CPU VIA CABLE
SPARE GATES:
CPU CONN
J1
2130
U1
U2
EP900
U3
U4
U5
74HC4060
U6
74HC74
U12 A
U12 B
74HC4040
U8
74HCT04
U11 A
U11 B
U11 C
U11 D
U11 E
U11 F
NE522
U7 A
U7 B
VR5
TOP
N/C
R1 4.7K
R2 1.1K
R3 4.7K
R4 1.1K
R5 4.7K
R6 4.7K
R7 1.1K
R8 4.7K
R9 1.1K
R10 4.7K
R11 4.7K
R12 4.7K
R20 4.7K
R67 200
R68 1.1K
R70 39K
R71 82K
R72 4.7K
R76 4.7K
C1 47uF 10V
C2 0.1uF
C3 10uF
C4 0.1uF
C5 1.5uF 50V
C6 .01uF 100V
C7 1uF 100V
C8 .01uF 100V
C63 50V 100pF
C64 0.1uF
C65 1.5uF 50V
C66 10uF
VR5 6.8V
DMDCS*
FPWRITE*
BUSYO
OTDCS*
DPRENA
DPRENAO
CLOCK 2
SDD
GRIDCLK
DATACLK
STRB_DRVR
GRIDDATA
CDCLK
GSTROBE
900HZ
CLOCK
SCAN
SDO
GRIDCLKO
DATACLKO
STRB_DRVRO
GRIDDATAO
ENCODERINTR
STROBE
KEYBOARDINTR
FPINTR*
REFRESH
BRESET*
75VSD
PSFAILINTR*
3.6864MHZCLK
3.6864MHZCLK*
460.8KHZ
FRNTPNLCS*
FPDTK*
FPINT*
-12V
+5V
+12V
+35V
+75V
PSFAILINTR*
OTDCS*
DMDCS*
ENCODERCS*
ENCODERRESET*
LED_LATCH_EN
KEYBOARDCS*
FPDTACK*
AOUT
BOUT
GSTROBE
ABCLK
CDCLK
STROBE
DMDBLANK
OTDBLANK
LED_OUTPUT_CNTRL
BUSYO
BUSYO
FPWRITE*
AOUT
LEDENABLE*
TP1
TP2
TP3
TP5
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP22
TP23
TP24
TP28
TP34
TP35
TP39
TP42

TP1 = SD (PG4D8)
TP2 = +5V (PG1C8)
TP3 = GND (PG1B7)
TP4 = D3 (PG2C8)
TP5 = D4 (PG1C6)
TP6 = D1 (PG2C7)
TP7 = D2 (PG2C8)
TP8 = D0 (PG2C7)
TP9 = A10 (PG1A5)
TP10 = A9 (PG1A5)
TP11 = A8 (PG1A5)
TP12 = A7 (PG1B5)
TP13 = A6 (PG1B5)
TP14 = A5 (PG1B5)
TP15 = A4 (PG1B5)
TP16 = +35V (PG1C8)
TP17 = +12V (PG1C8)
TP18 = +75V (PG1B8)
TP19 = REFRESH (PG4B2)
TP20 = GRIDCLK (PG4B8)
TP21 = GRIDDATA (PG4A8)
TP22 = A11 (PG1A5)
TP23 = A12 (PG1A5)
TP24 = FPDTK* (PG1C6)
TP25 = STRB_DRVR (PG4D7)
TP26 = ABCLK (PG4D7)
TP27 = DATACLK (PG4D7)
TP28 = -12V (PG1C6)
TP29 = GRIDCLKO (PG3D6)
TP30 = STRB_DRVRO (PG3D6)
TP31 = GRIDDATAO (PG3D6)
TP32 = DATACLKO (PG3D7)
TP33 = SDO (PG3D7)
TP34 = FRNTPNLCS* (PG1B6)
TP35 = PSFAILINTR* (PG1C1)
TP36 = CDCLK (PG4D7)
TP37 = OTDBLANK (PG3D6)
TP38 = DMDBLANK (PG4B8)
TP39 = 460.8KHZ (PG1B5)
TP40 = BOUT (PG2D4)
TP41 = AOUT (PG2D4)
TP42 = CLOCK (PG1B5)
TP43 = U17 SERIAL OUT (PG4D4)
TP44 = DOTMATFILAMENTA (PG4C2)
TP45 = U19 SERIAL OUT (PG4D1)
TP46 = DOTMATFILAMENTB (PG4C7)
TP47 = OUTPUTFILAMENTB (PG3C3)
TP48 = OUTPUTFILAMENTA (PG3C7)
TP49 = U15 SERIAL OUT (PG3D3)
TP50 = U14 SERIAL OUT (PG3D5)

NOTES:
1. ALL RESISTORS ARE CER. (SMT) 5% 1/8W.
2. ALL CAPACITORS ARE CER (SMT) 25V UNLESS NOTED.

IC(S)	VCC PIN(S)	GND PIN(S)
U3,U4,U5 U9	1, 44	22, 23
U11,U12,U13	14	7
U6,U8	16	8
U24	1, 29	14,15
U1,U2	1, 52	26, 27
U10	20	10

FRONT PANEL 5700A-1002 1 OF 4 AUG.8,1988

Figure 7-2. A2 Front Panel PCA (cont)

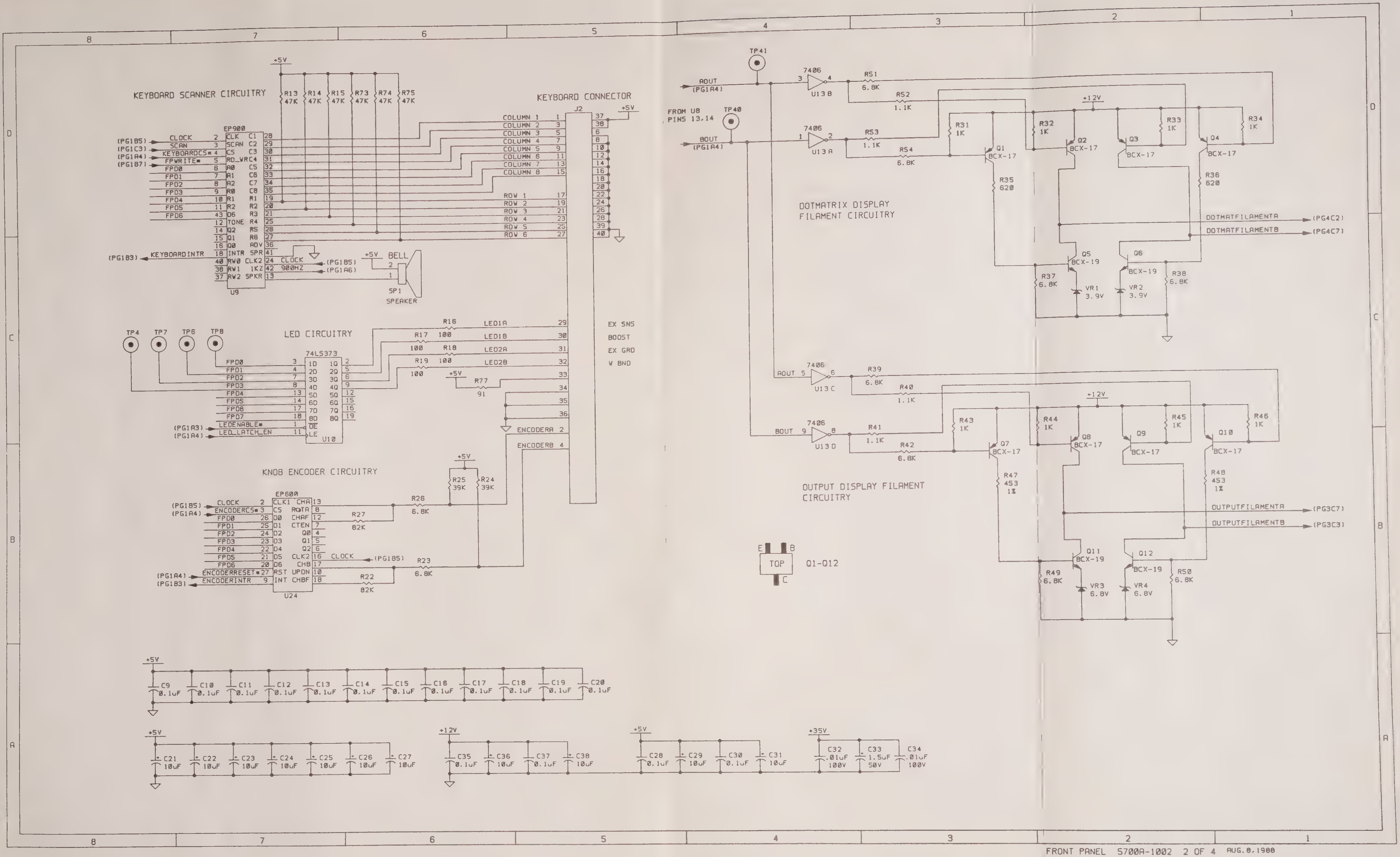

KEYBOARD SCANNER CIRCUITRY
KEYBOARD CONNECTOR
LED CIRCUITRY
KNOB ENCODER CIRCUITRY
DOTMATRIX DISPLAY FILAMENT CIRCUITRY
OUTPUT DISPLAY FILAMENT CIRCUITRY
EP900
U9
74LS373
U10
EP600
U24
J2
7406
U13 A
U13 B
U13 C
U13 D
BELL
SP1
SPEAKER
TP4
TP7
TP6
TP8
TP40
TP41
FROM U8 PINS 13,14
AOUT (PG1A4)
BOUT (PG1A4)
(PG1B5) CLOCK
(PG1C3) SCAN
(PG1A4) KEYBOARDCS*
(PG1B7) FPWRITE*
(PG1B3) KEYBOARDINTR
(PG1A3) LEDENABLE*
(PG1A4) LED_LATCH_EN
(PG1B5) ENCODERCS*
(PG1A4) ENCODERRESET*
(PG1B3) ENCODERINTR
DOTMATFILAMENTA (PG4C2)
DOTMATFILAMENTB (PG4C7)
OUTPUTFILAMENTA (PG3C7)
OUTPUTFILAMENTB (PG3C3)
EX SNS
BOOST
EX GRD
W BND
ENCODERA
ENCODERB
Q1-Q12
TOP
E B C
+5V
+12V
+35V
FRONT PANEL 5700A-1002 2 OF 4 AUG.8.1988

Figure 7-2. A2 Front Panel PCA (cont)

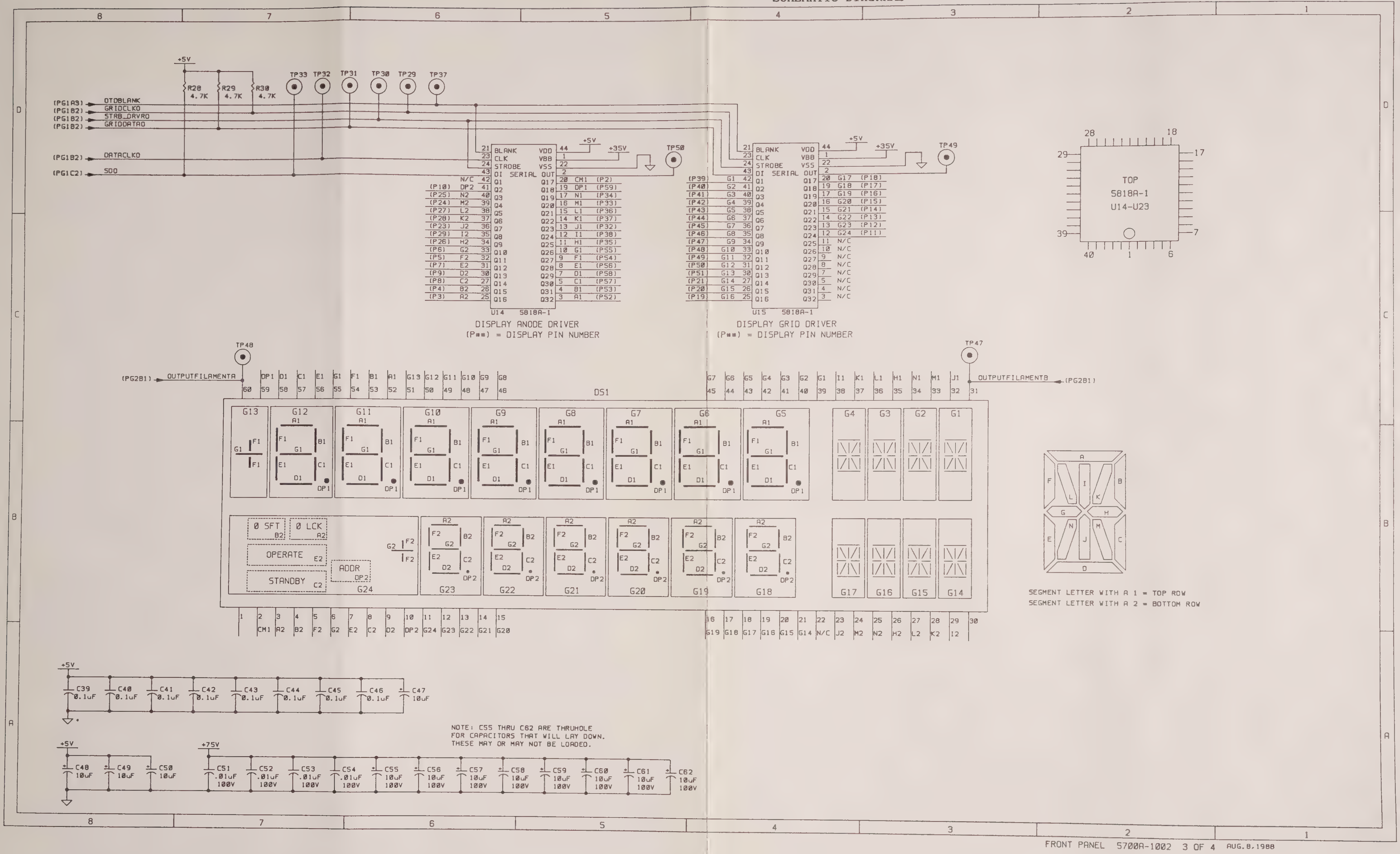

+5V
R28 4.7K
R29 4.7K
R30 4.7K
TP33
TP32
TP31
TP30
TP29
TP37
(PG1A3) OTDBLANK
(PG1B2) GRIDCLKO
(PG1B2) STRB_DRVRO
(PG1B2) GRIDDATAO
(PG1B2) DATACLKO
(PG1C2) SDO
BLANK
CLK
STROBE
DI SERIAL OUT
VDD
VBB
VSS
+35V
TP50
TP49
U14 5818A-1
DISPLAY ANODE DRIVER
(P##) = DISPLAY PIN NUMBER
U15 5818A-1
DISPLAY GRID DRIVER
(P##) = DISPLAY PIN NUMBER
TOP
5818A-1
U14-U23
TP48
TP47
(PG2B1) OUTPUTFILAMENTA
OUTPUTFILAMENTB (PG2B1)
DS1
Ø SFT
Ø LCK
OPERATE
STANDBY
ADDR
SEGMENT LETTER WITH A 1 = TOP ROW
SEGMENT LETTER WITH A 2 = BOTTOM ROW
C39 0.1uF
C40 0.1uF
C41 0.1uF
C42 0.1uF
C43 0.1uF
C44 0.1uF
C45 0.1uF
C46 0.1uF
C47 10uF
+75V
C48 10uF
C49 10uF
C50 10uF
C51 .01uF 100V
C52 .01uF 100V
C53 .01uF 100V
C54 .01uF 100V
C55 10uF 100V
C56 10uF 100V
C57 10uF 100V
C58 10uF 100V
C59 10uF 100V
C60 10uF 100V
C61 10uF 100V
C62 10uF 100V
NOTE: C55 THRU C62 ARE THRUHOLE
FOR CAPACITORS THAT WILL LAY DOWN.
THESE MAY OR MAY NOT BE LOADED.
FRONT PANEL 5700A-1002 3 OF 4 AUG.8.1988

Figure 7-2. A2 Front Panel PCA (cont)

]

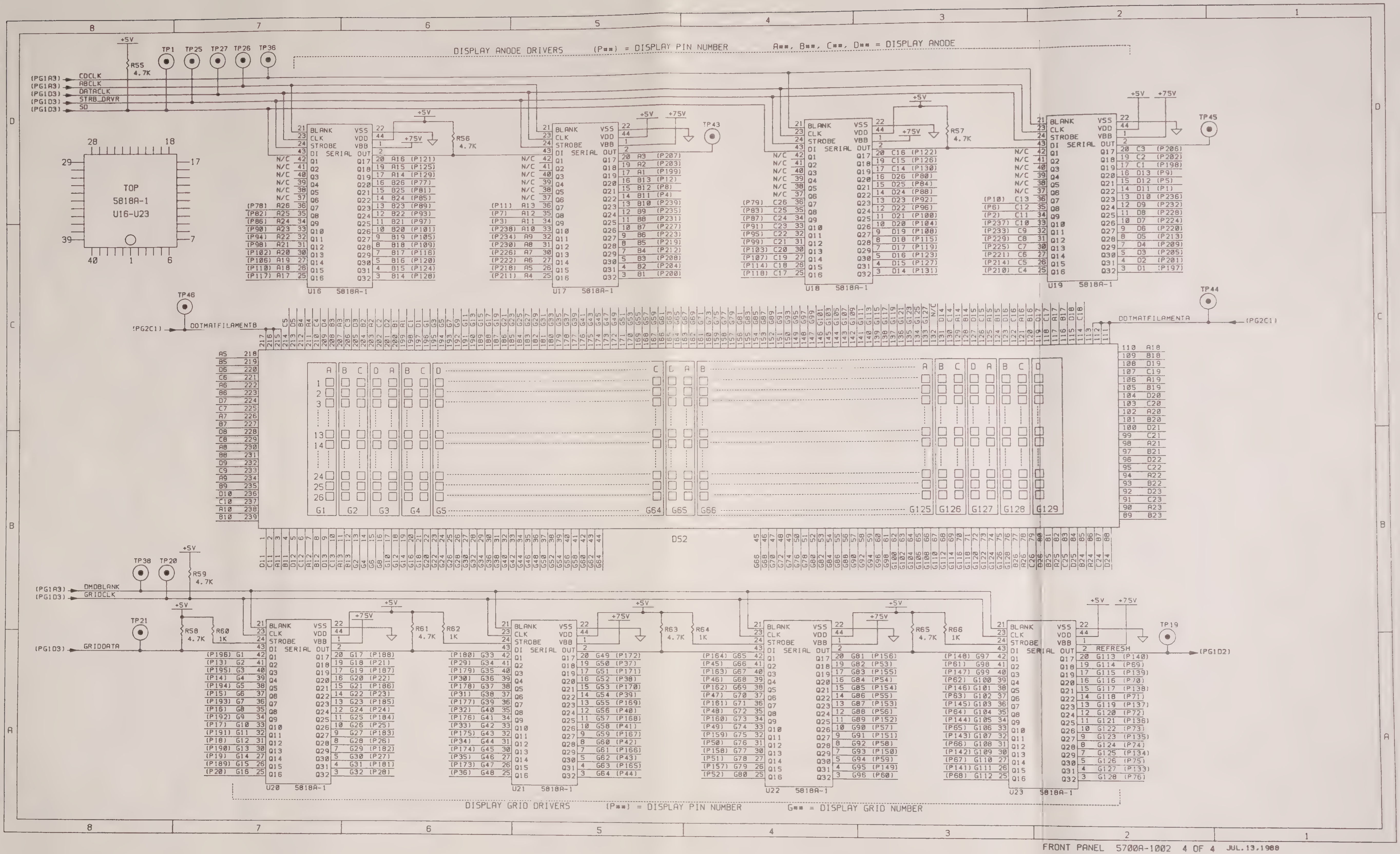

DISPLAY ANODE DRIVERS
(P**) = DISPLAY PIN NUMBER
A**, B**, C**, D** = DISPLAY ANODE
(PG1A3) CDCLK
(PG1A3) ABCLK
(PG1D3) DATACLK
(PG1D3) STRB_DRVR
(PG1D3) SD
+5V
R55 4.7K
TP1
TP25
TP27
TP26
TP36
TP43
TP45
TP44
TP46
TOP
5818A-1
U16-U23
R56 4.7K
R57 4.7K
+75V
BLANK
CLK
STROBE
DI SERIAL OUT
VSS
VDD
VBB
N/C
U16 5818A-1
U17 5818A-1
U18 5818A-1
U19 5818A-1
(PG2C1) DOTMATFILAMENTB
DOTMATFILAMENTA (PG2C1)
DS2
G1
G2
G3
G4
G5
G64
G65
G66
G125
G126
G127
G128
G129
TP38
TP20
TP21
TP19
R59 4.7K
(PG1A3) DMDBLANK
(PG1D3) GRIDCLK
(PG1D3) GRIDDATA
R58 4.7K
R60 1K
R61 4.7K
R62 1K
R63 4.7K
R64 1K
R65 4.7K
R66 1K
REFRESH
(PG1D2)
U20 5818A-1
U21 5818A-1
U22 5818A-1
U23 5818A-1
DISPLAY GRID DRIVERS
(P**) = DISPLAY PIN NUMBER
G** = DISPLAY GRID NUMBER
FRONT PANEL 5700A-1002 4 OF 4 JUL.13.1988

Figure 7-2. A2 Front Panel PCA (cont)

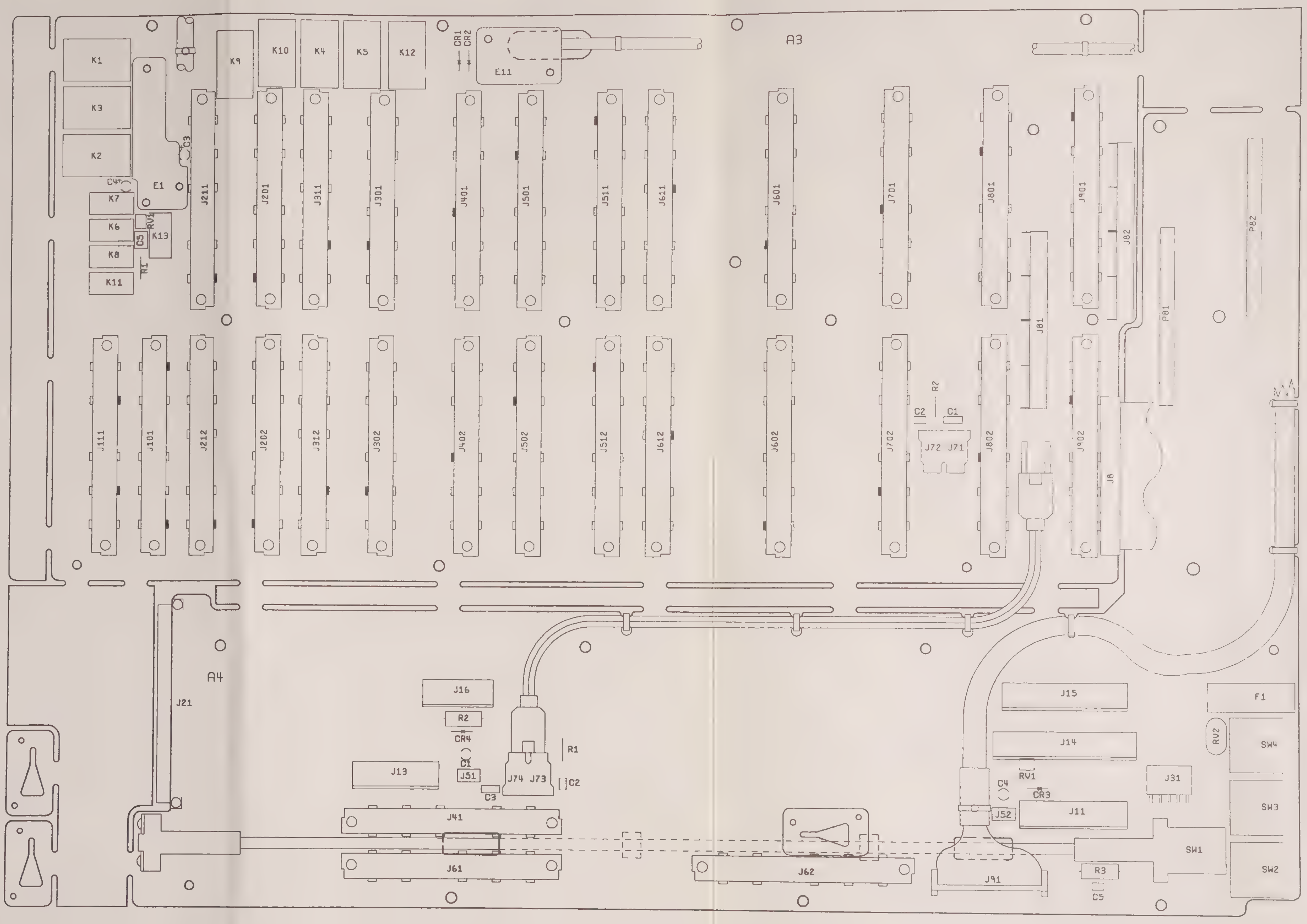

A3
K1
K3
K2
C4+
E1
C3
K7
K6
K8
K11
RV1
C5
K13
R1
K9
K10
K4
K5
K12
CR1
CR2
E11
J211
J201
J311
J301
J401
J501
J511
J611
J601
J701
J801
J901
J82
PB2
J81
PB1
J111
J101
J212
J202
J312
J302
J402
J502
J512
J612
J602
J702
R2
C2
C1
J72
J71
J802
J902
J8
A4
J21
J16
R2
CR4
C1
J51
J74
J73
R1
C2
C3
J13
J41
J61
J62
J91
J15
F1
J14
RV2
SW4
RV1
C4
CR3
J52
J11
J31
SW3
SW1
R3
C5
SW2

Figure 7-3. A3 Analog Motherboard PCA

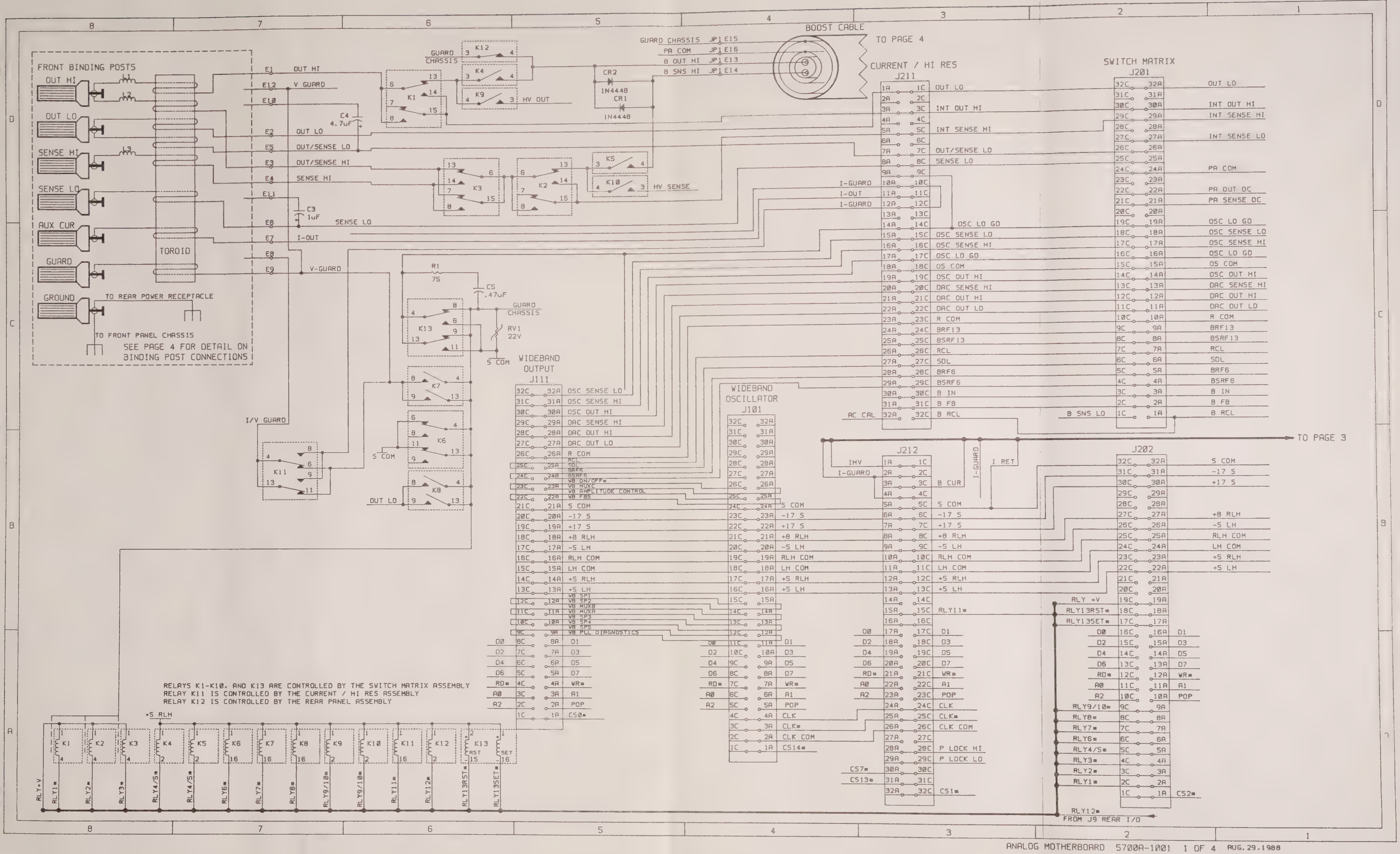

FRONT BINDING POSTS
OUT HI
OUT LO
SENSE HI
SENSE LO
AUX CUR
GUARD
GROUND
TOROID
TO REAR POWER RECEPTACLE
TO FRONT PANEL CHASSIS
SEE PAGE 4 FOR DETAIL ON BINDING POST CONNECTIONS
OUT HI
V GUARD
OUT LO
OUT/SENSE LO
OUT/SENSE HI
SENSE HI
SENSE LO
I-OUT
V-GUARD
I/V GUARD
C4 4.7uF
C3 1uF
R1 75
C5 .47uF
RV1 22V
GUARD CHASSIS
S COM
HV OUT
HV SENSE
CR2 1N4448
CR1 1N4448
BOOST CABLE
TO PAGE 4
GUARD CHASSIS
PA COM
B OUT HI
B SNS HI
CURRENT / HI RES
J211
SWITCH MATRIX
J201
WIDEBAND OUTPUT
J111
WIDEBAND OSCILLATOR
J101
J212
J202
TO PAGE 3
OUT LO
INT OUT HI
INT SENSE HI
INT SENSE LO
PA COM
PA OUT DC
PA SENSE DC
I-GUARD
I-OUT
OSC LO GD
OSC SENSE LO
OSC SENSE HI
OS COM
OSC OUT HI
DAC SENSE HI
DAC OUT HI
DAC OUT LO
R COM
BRF13
BSRF13
RCL
SDL
BRF6
BSRF6
B IN
B FB
B RCL
AC CAL
B SNS LO
IHV
I RET
B CUR
S COM
-17 S
+17 S
+8 RLH
-5 LH
RLH COM
LH COM
+5 RLH
+5 LH
WB ON/OFF
WB HUXC
WB AMPLITUDE CONTROL
WB FBS
WB SP1
WB SP2
WB HUXB
WB HUXA
WB SP3
WB SP4
WB SP5
WB PLL DIAGNOSTICS
D0 D1 D2 D3 D4 D5 D6 D7
RD WR
A0 A1 A2
POP
CS0
CLK
CLK COM
CS14
RLY11
P LOCK HI
P LOCK LO
CS7
CS13
CS1
RLY +V
RLY13RST
RLY13SET
RLY9/10
RLY8
RLY7
RLY6
RLY4/5
RLY3
RLY2
RLY1
CS2
RLY12
FROM J9 REAR I/O
RELAYS K1-K10, AND K13 ARE CONTROLLED BY THE SWITCH MATRIX ASSEMBLY
RELAY K11 IS CONTROLLED BY THE CURRENT / HI RES ASSEMBLY
RELAY K12 IS CONTROLLED BY THE REAR PANEL ASSEMBLY
+5 RLH
K1 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 K12 K13
RLY+V
RLY12
RLY13RST
RLY13SET
ANALOG MOTHERBOARD 5700A-1001 1 OF 4 AUG.29.1988

Figure 7-3. A3 Analog Motherboard PCA (cont)

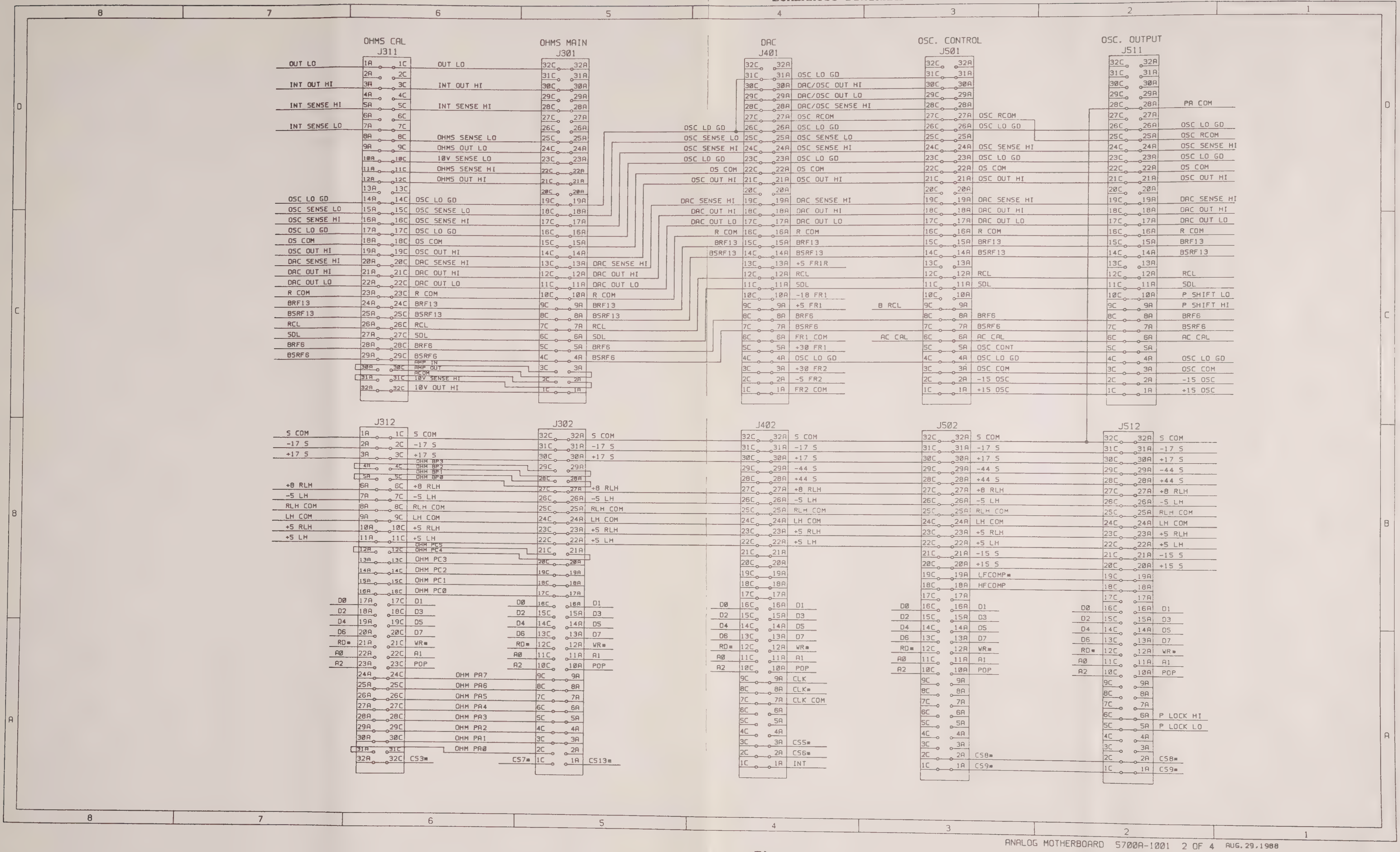

OHMS CAL
J311
OHMS MAIN
J301
DAC
J401
OSC. CONTROL
J501
OSC. OUTPUT
J511
J312
J302
J402
J502
J512
ANALOG MOTHERBOARD 5700A-1001 2 OF 4 AUG.29.1988

Figure 7-3. A3 Analog Motherboard PCA (cont)

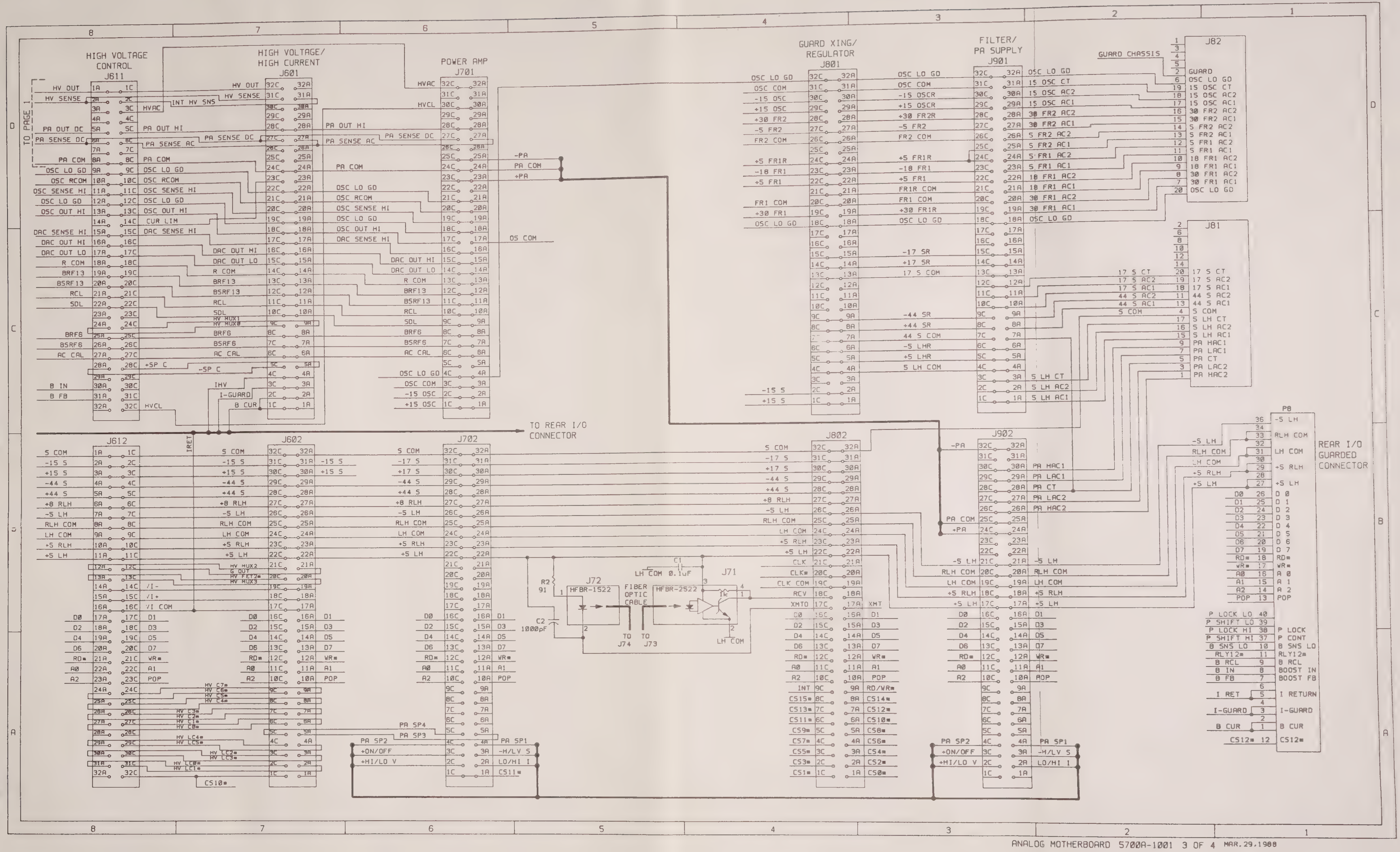

HIGH VOLTAGE CONTROL
J611
HIGH VOLTAGE/ HIGH CURRENT
J601
POWER AMP
J701
GUARD XING/ REGULATOR
J801
FILTER/ PA SUPPLY
J901
J82
J81
TO PAGE 1
TO REAR I/O CONNECTOR
J612
J602
J702
J802
J902
P8
REAR I/O GUARDED CONNECTOR
J72
HFBR-1522
J71
HFBR-2522
FIBER OPTIC CABLE
LH COM
C1 0.1uF
R2 91
C2 1000pF
TO J74
TO J73
IRET
GUARD CHASSIS
ANALOG MOTHERBOARD 5700A-1001 3 OF 4 MAR.29.1988

Figure 7-3. A3 Analog Motherboard PCA (cont)

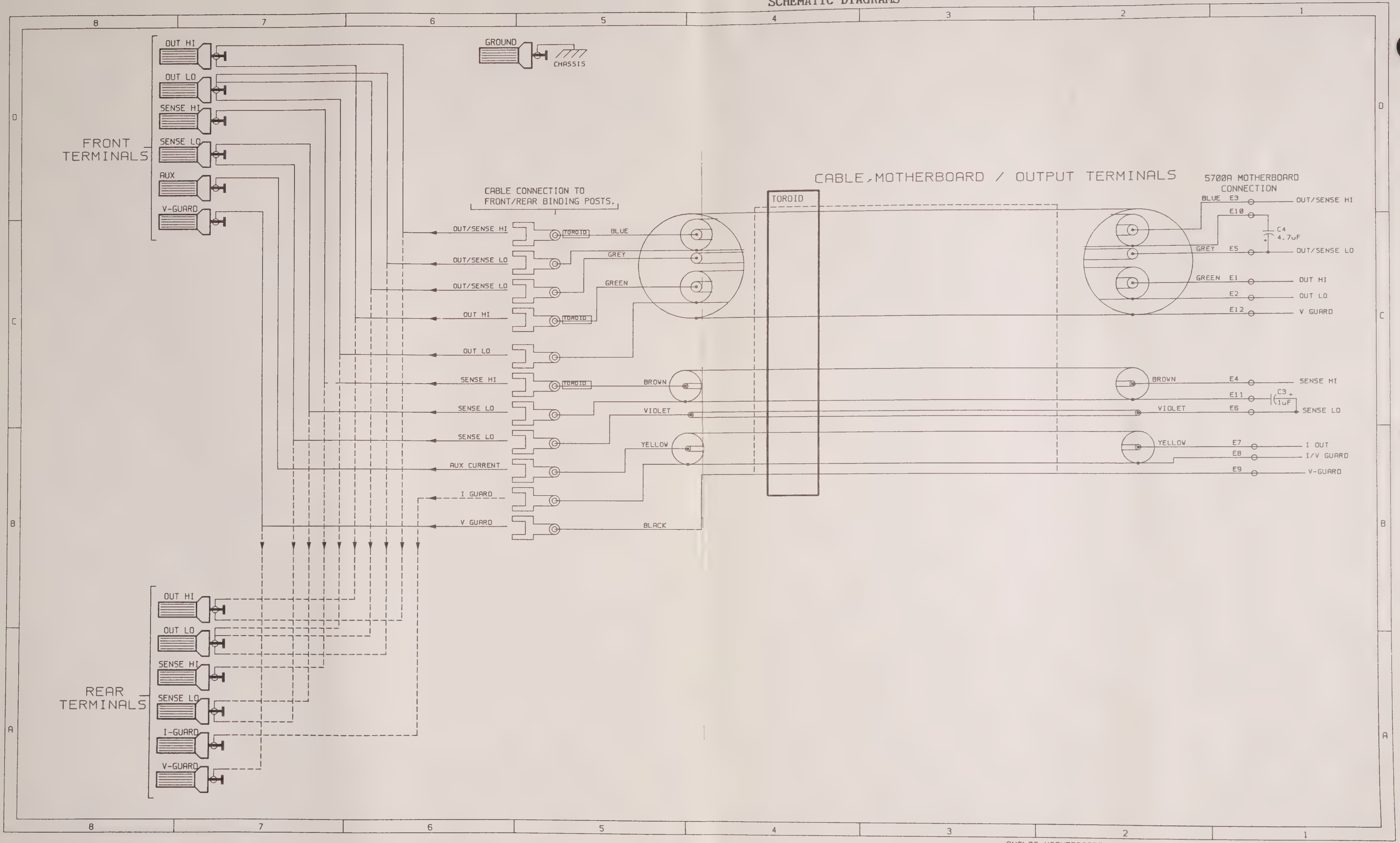

8
7
6
5
4
3
2
1
D
C
B
A
FRONT TERMINALS
OUT HI
OUT LO
SENSE HI
SENSE LO
AUX
V-GUARD
GROUND
CHASSIS
CABLE CONNECTION TO FRONT/REAR BINDING POSTS.
OUT/SENSE HI
OUT/SENSE LO
OUT/SENSE LO
OUT HI
OUT LO
SENSE HI
SENSE LO
SENSE LO
AUX CURRENT
I GUARD
V GUARD
TOROID
BLUE
GREY
GREEN
BROWN
VIOLET
YELLOW
BLACK
CABLE, MOTHERBOARD / OUTPUT TERMINALS
TOROID
5700A MOTHERBOARD CONNECTION
BLUE E3 OUT/SENSE HI
E10
C4 4.7uF
GREY E5 OUT/SENSE LO
GREEN E1 OUT HI
E2 OUT LO
E12 V GUARD
BROWN E4 SENSE HI
E11
C3 1uF
VIOLET E6 SENSE LO
YELLOW E7 I OUT
E8 I/V GUARD
E9 V-GUARD
REAR TERMINALS
OUT HI
OUT LO
SENSE HI
SENSE LO
I-GUARD
V-GUARD
ANALOG MOTHERBOARD 5700A-1001 4 OF 4 MAR.28,1988

Figure 7-3. A3 Analog Motherboard PCA (cont)

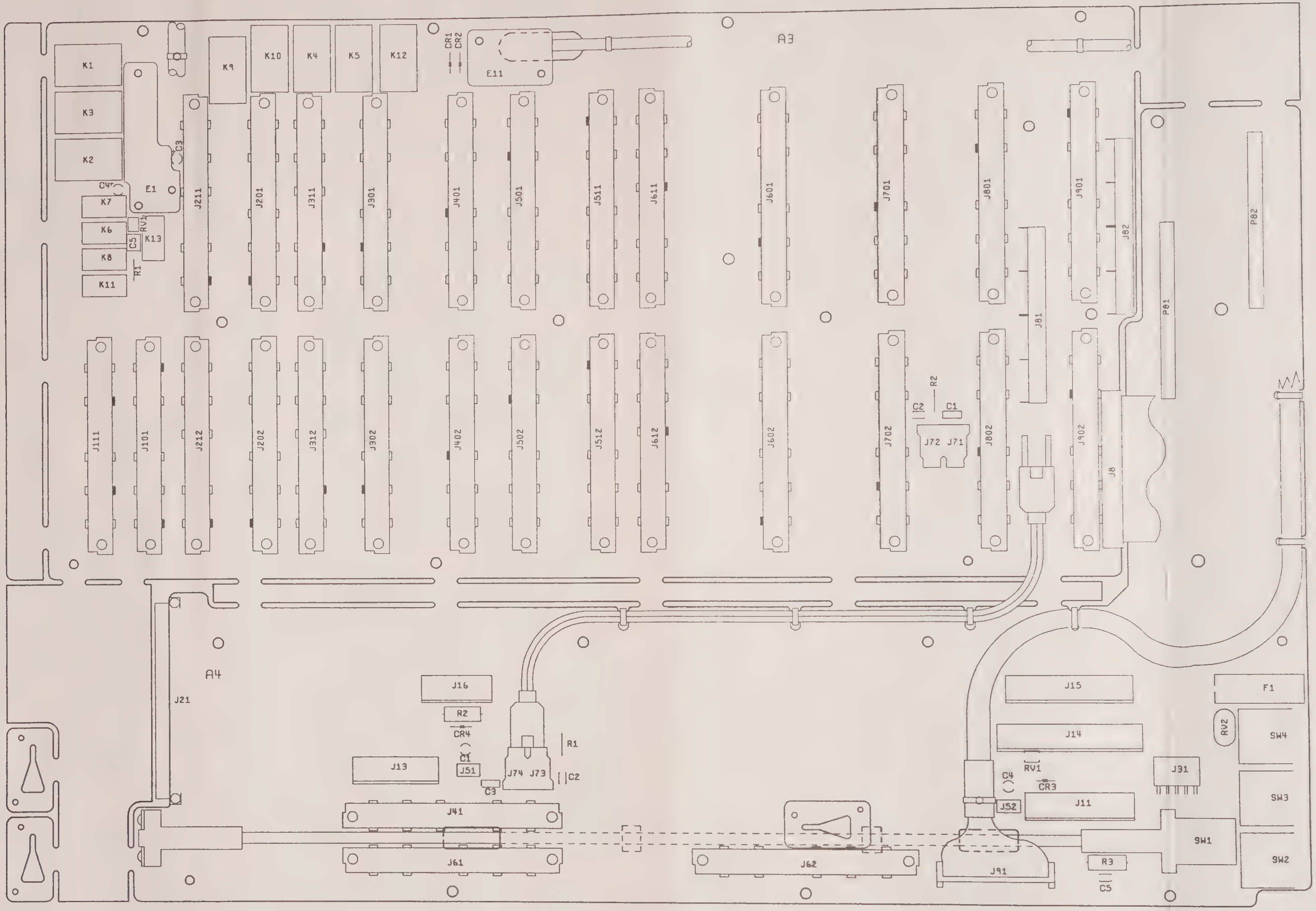
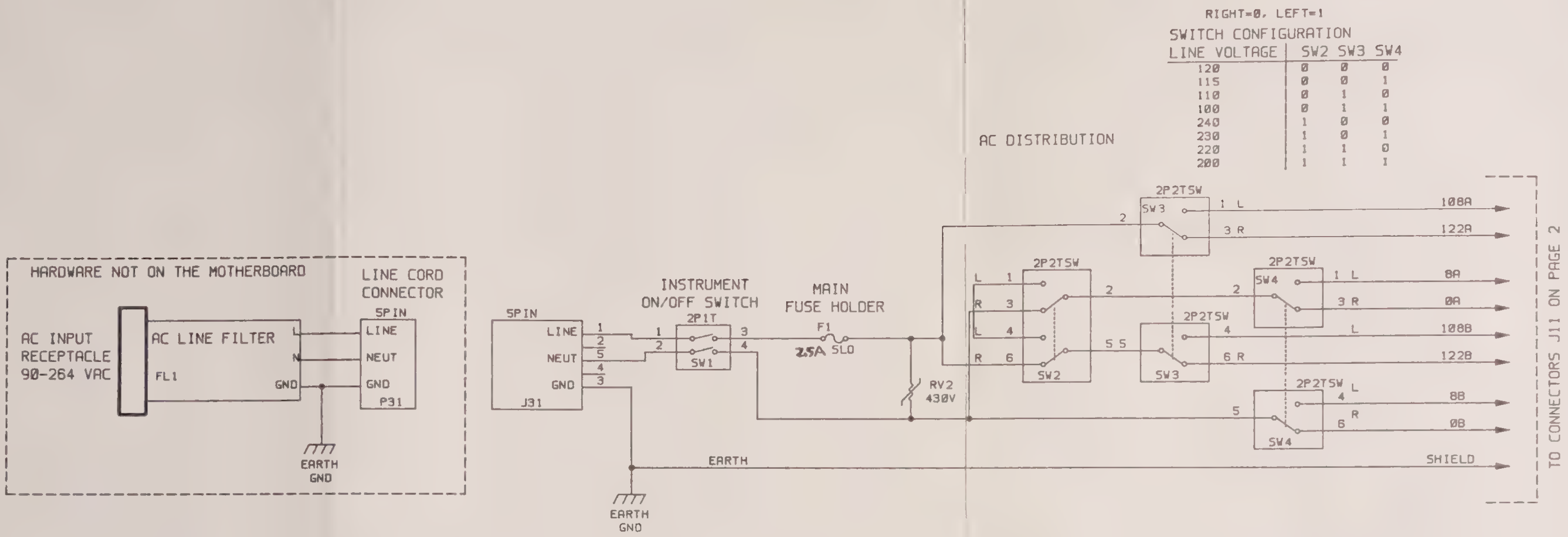

A3
K1
K3
K2
K9
K10
K4
K5
K12
CR1
CR2
E11
C3
C4
E1
K7
K6
K8
K11
RV1
C5
K13
R1
J211
J201
J311
J301
J401
J501
J511
J611
J601
J701
J801
J901
J82
P82
J81
P81
J111
J101
J212
J202
J312
J302
J402
J502
J512
J612
J602
J702
R2
C2
C1
J72
J71
J802
J902
J8
A4
J21
J16
R2
CR4
C1
J51
J74
J73
R1
C2
C3
J13
J41
J61
J62
J91
J15
J14
RV1
C4
CR3
J52
J11
J31
F1
RV2
SW4
SW3
SW1
SW2
R3
C5

Figure 7-4. A4 Digital Motherboard PCA


HARDWARE NOT ON THE MOTHERBOARD
AC INPUT RECEPTACLE 90-264 VAC
AC LINE FILTER
FL1
L
N
GND
LINE CORD CONNECTOR
5PIN
LINE
NEUT
GND
P31
EARTH GND
5PIN
LINE
NEUT
GND
J31
1
2
5
4
3
INSTRUMENT ON/OFF SWITCH
2P1T
SW1
MAIN FUSE HOLDER
F1
2.5A SLO
RV2
430V
EARTH
EARTH GND
AC DISTRIBUTION
2P2TSW
SW2
SW3
SW4
L
R
108A
122A
8A
0A
108B
122B
8B
0B
SHIELD
TO CONNECTORS J11 ON PAGE 2

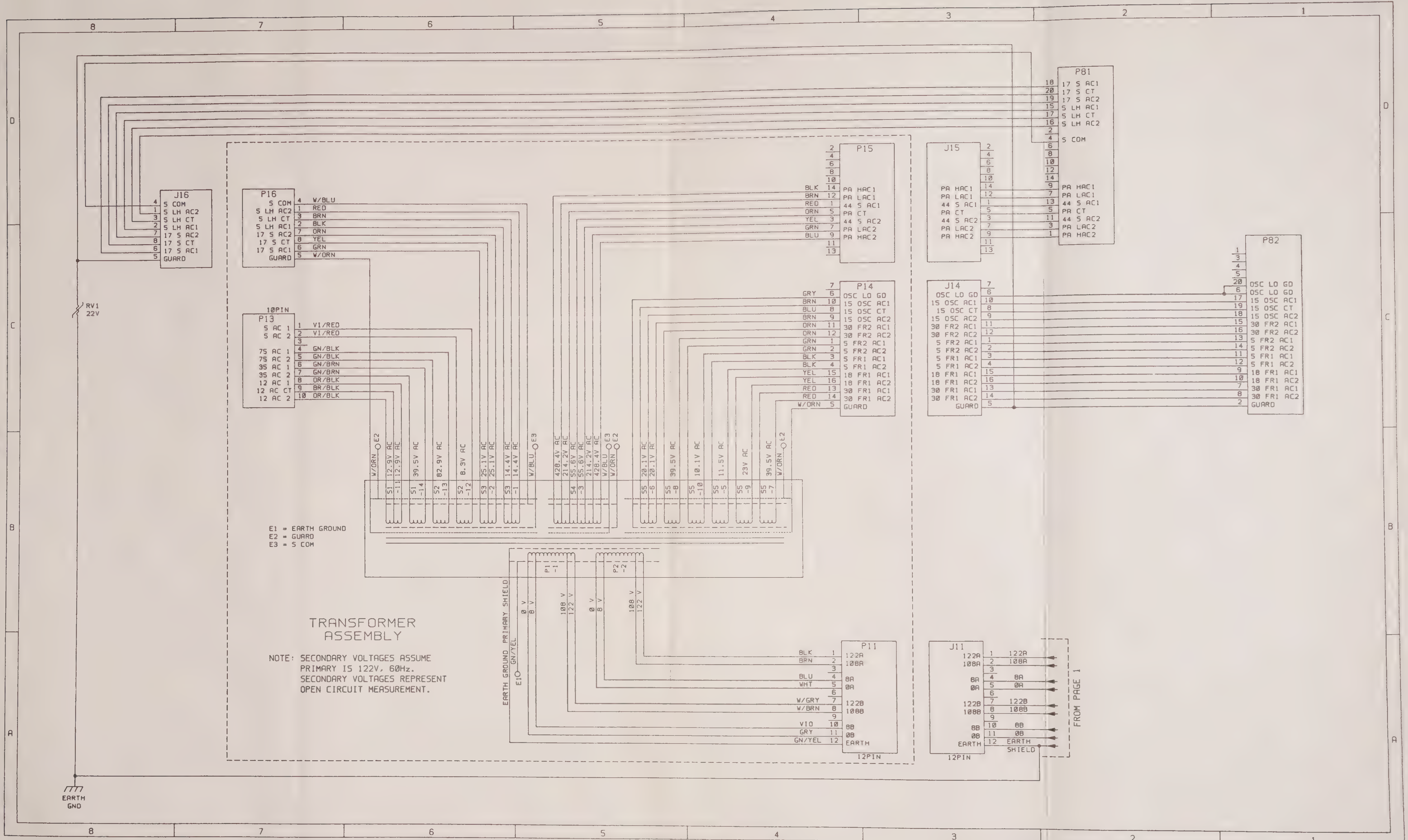
RIGHT=0, LEFT=1

SWITCH CONFIGURATION

LINE VOLTAGE	SW2	SW3	SW4
120	0	0	0
115	0	0	1
110	0	1	0
100	0	1	1
240	1	0	0
230	1	0	1
220	1	1	0
200	1	1	1

DIGITAL MOTHERBOARD 5700A-1005 1 OF 3 AUG.29,1988

Figure 7-4. A4 Digital Motherboard PCA (cont)


P81
17 S AC1
17 S CT
17 S AC2
5 LH AC1
5 LH CT
5 LH AC2
S COM
PA HAC1
PA LAC1
44 S AC1
PA CT
44 S AC2
PA LAC2
PA HAC2
P15
J15
P82
P14
J14
OSC LO GD
15 OSC AC1
15 OSC CT
15 OSC AC2
30 FR2 AC1
30 FR2 AC2
5 FR2 AC1
5 FR2 AC2
5 FR1 AC1
5 FR1 AC2
18 FR1 AC1
18 FR1 AC2
30 FR1 AC1
30 FR1 AC2
GUARD
J16
P16
10PIN
P13
5 AC 1
5 AC 2
75 AC 1
75 AC 2
35 AC 1
35 AC 2
12 AC 1
12 AC CT
12 AC 2
RV1
22V
E1 = EARTH GROUND
E2 = GUARD
E3 = S COM
TRANSFORMER ASSEMBLY
NOTE: SECONDARY VOLTAGES ASSUME PRIMARY IS 122V, 60Hz. SECONDARY VOLTAGES REPRESENT OPEN CIRCUIT MEASUREMENT.
EARTH GROUND PRIMARY SHIELD
P11
122A
108A
8A
0A
122B
108B
8B
0B
EARTH
12PIN
J11
SHIELD
FROM PAGE 1
EARTH GND

DIGITAL MOTHERBOARD 5700A-1005 2 OF 3 AUG.29.1988

Figure 7-4. A4 Digital Motherboard PCA (cont)

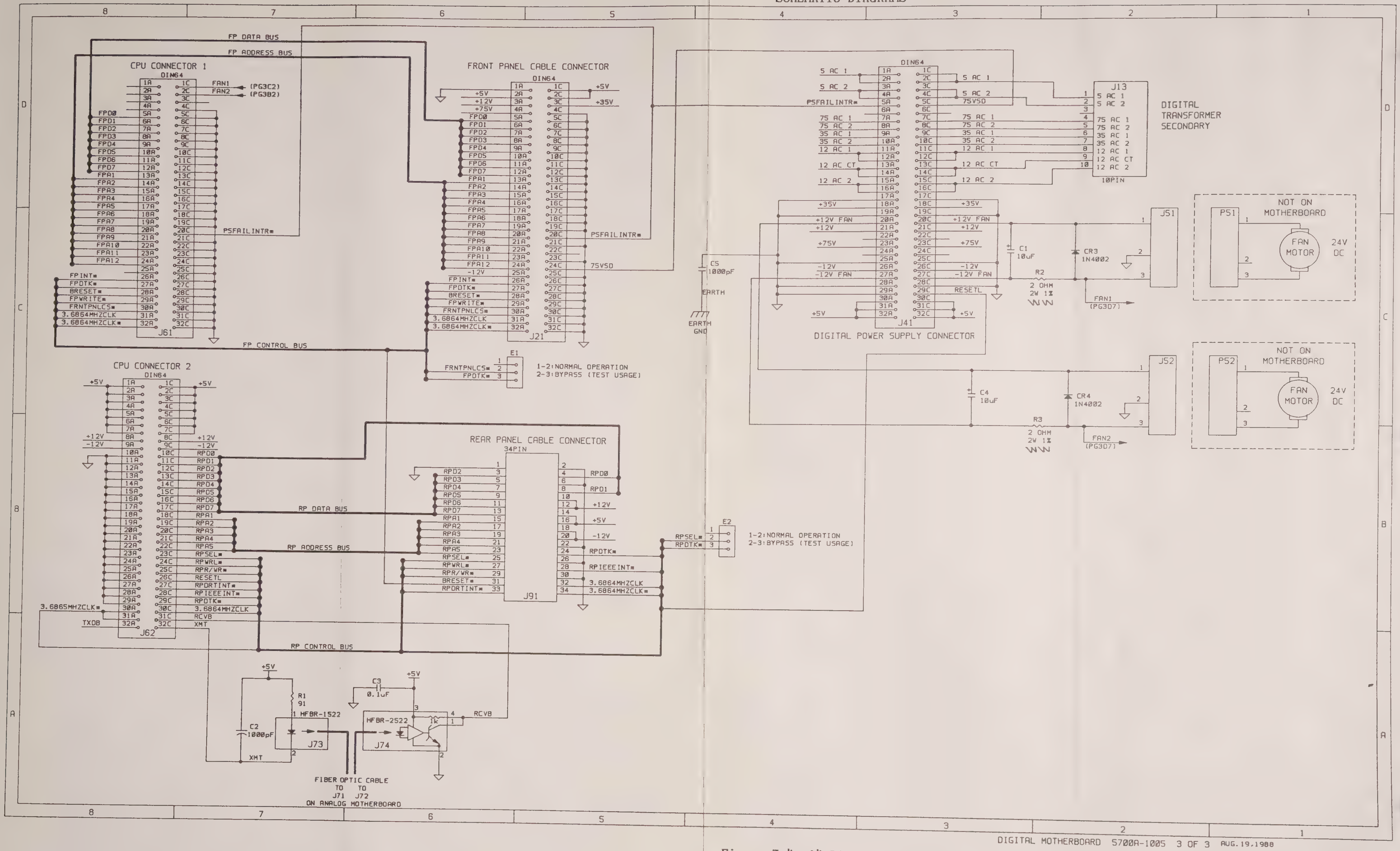

FP DATA BUS
FP ADDRESS BUS
CPU CONNECTOR 1
DIN64
FAN1 (PG3C2)
FAN2 (PG3B2)
FPD0
FPD1
FPD2
FPD3
FPD4
FPD5
FPD6
FPD7
FPA1
FPA2
FPA3
FPA4
FPA5
FPA6
FPA7
FPA8
FPA9
FPA10
FPA11
FPA12
PSFAILINTR*
FPINT*
FPDTK*
BRESET*
FPWRITE*
FRNTPNLCS*
3.6864MHZCLK
3.6864MHZCLK*
J61
FP CONTROL BUS
FRONT PANEL CABLE CONNECTOR
DIN64
+5V
+12V
+75V
+35V
-12V
75VSD
J21
E1
FRNTPNLCS*
FPDTK*
1-2:NORMAL OPERATION
2-3:BYPASS (TEST USAGE)
CPU CONNECTOR 2
DIN64
+5V
+12V
-12V
RPD0
RPD1
RPD2
RPD3
RPD4
RPD5
RPD6
RPD7
RPA1
RPA2
RPA3
RPA4
RPA5
RPSEL*
RPWRL*
RPR/WR*
RESETL
RPORTINT*
RPIEEEINT*
RPDTK*
3.6864MHZCLK
RCVB
XMT
3.6865MHZCLK*
TXDB
J62
RP DATA BUS
RP ADDRESS BUS
RP CONTROL BUS
REAR PANEL CABLE CONNECTOR
34PIN
BRESET*
RPORTINT*
RPDTK*
RPIEEEINT*
3.6864MHZCLK*
J91
E2
RPSEL*
RPDTK*
1-2:NORMAL OPERATION
2-3:BYPASS (TEST USAGE)
+5V
R1
91
HFBR-1522
C2
1000pF
J73
XMT
C3
0.1uF
HFBR-2522
1k
J74
RCVB
FIBER OPTIC CABLE
TO TO
J71 J72
ON ANALOG MOTHERBOARD
C5
1000pF
EARTH
EARTH GND
DIN64
5 AC 1
5 AC 2
PSFAILINTR*
75VSD
75 AC 1
75 AC 2
35 AC 1
35 AC 2
12 AC 1
12 AC CT
12 AC 2
+35V
+12V FAN
+12V
+75V
-12V
-12V FAN
RESETL
+5V
J41
DIGITAL POWER SUPPLY CONNECTOR
J13
10PIN
DIGITAL TRANSFORMER SECONDARY
C1
10uF
CR3
1N4002
R2
2 OHM
2W 1%
FAN1
(PG3D7)
J51
P51
NOT ON MOTHERBOARD
FAN MOTOR
24V DC
C4
10uF
CR4
1N4002
R3
2 OHM
2W 1%
FAN2
(PG3D7)
J52
P52
NOT ON MOTHERBOARD
FAN MOTOR
24V DC
DIGITAL MOTHERBOARD 5700A-1005 3 OF 3 AUG.19.1988

Figure 7-4. A4 Digital Motherboard PCA (cont)

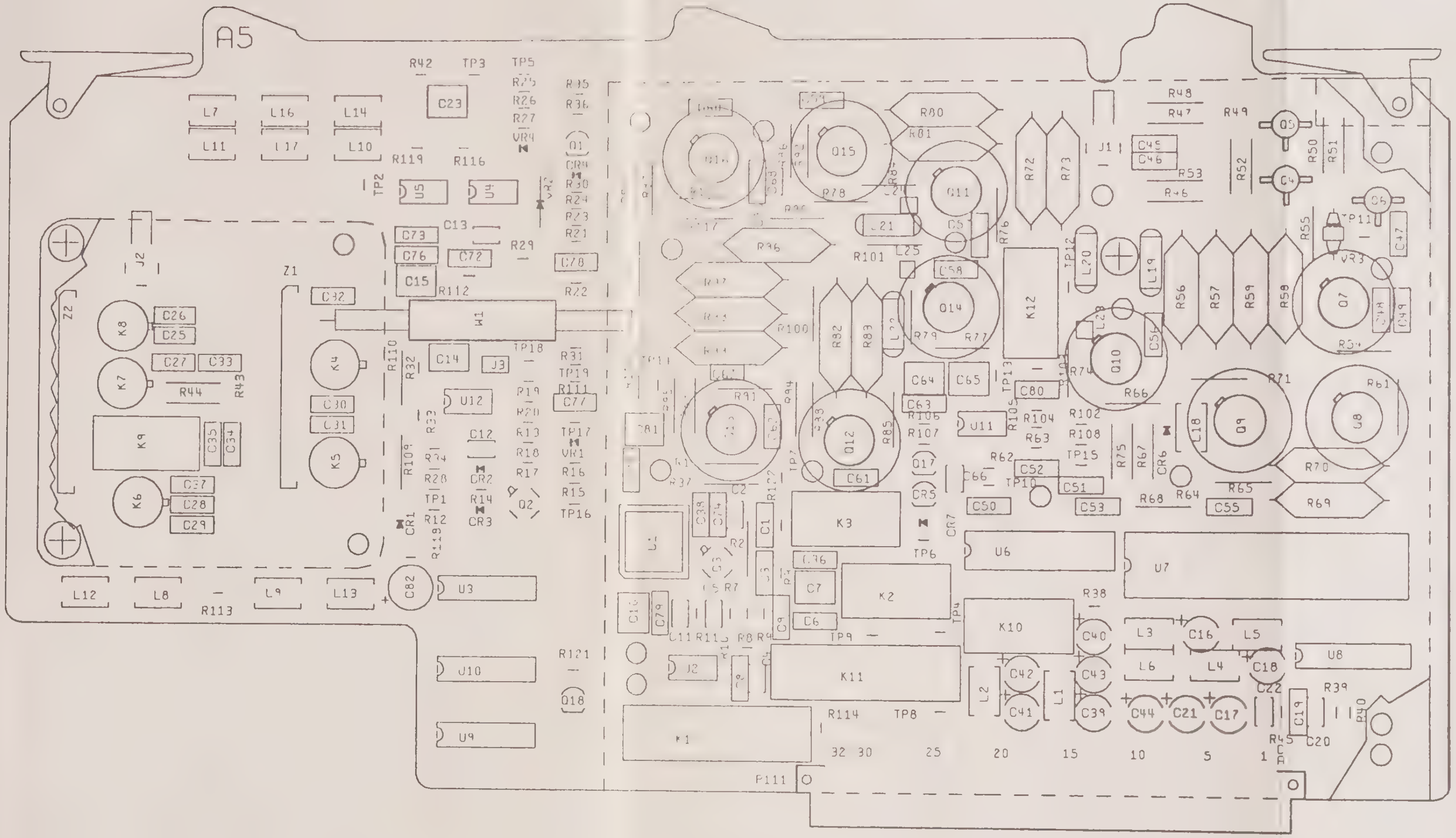
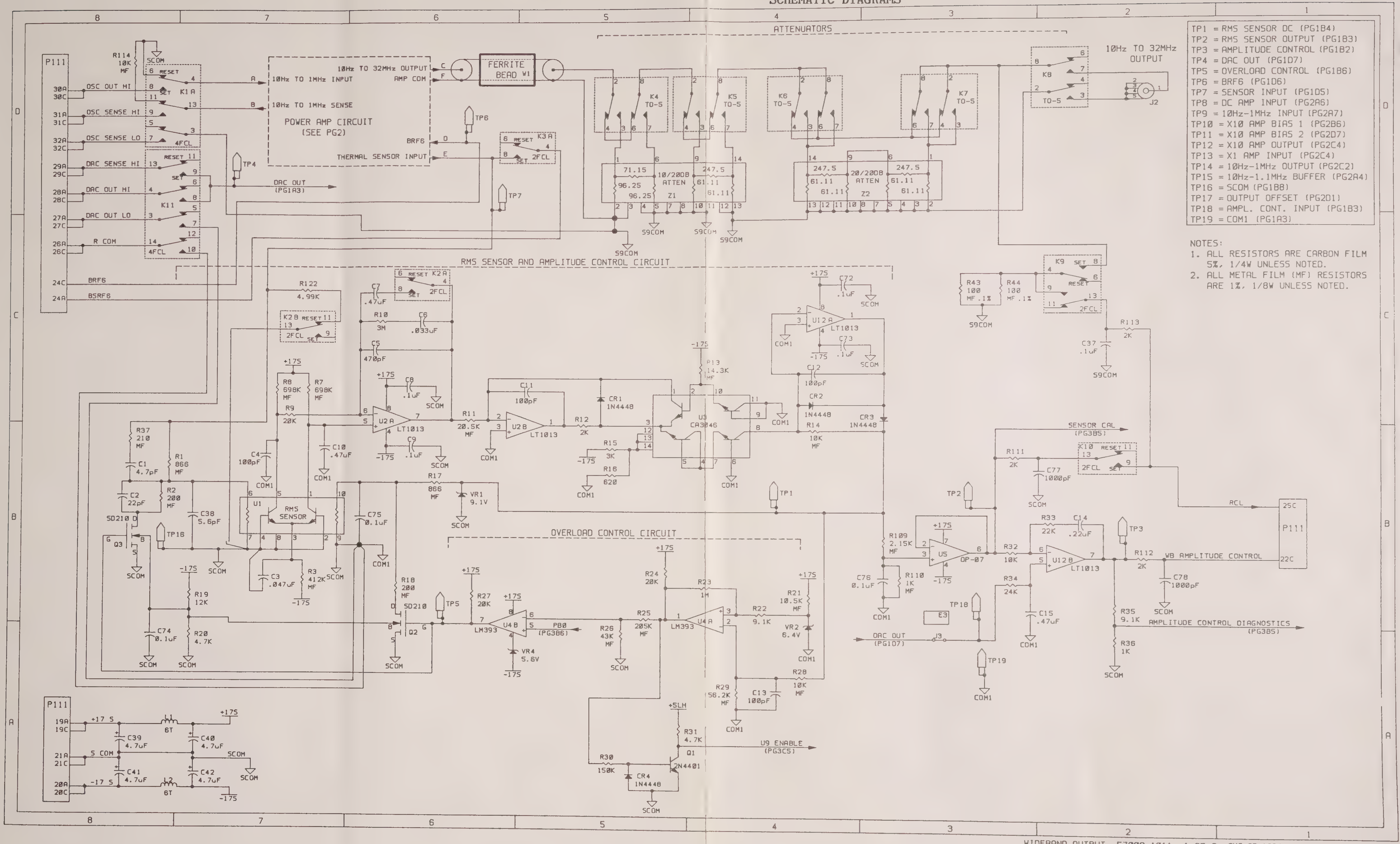

A5
R42
TP3
TP5
R45
R36
C23
L7
L16
L14
L11
L17
L10
R119
R116
TP2
U5
U4
Z1
J2
Z2
K8
K7
K9
K6
K4
K5
C26
C25
C27
C33
R44
R43
C35
C34
C37
C28
C29
C32
C30
C31
C73
C76
C72
C15
C13
R29
R112
W1
C14
J3
U12
C12
CR2
R14
CR3
CR1
TP1
R12
R110
R32
R33
R109
R20
R28
R19
R111
C77
R13
R10
R17
R15
TP16
TP17
VR1
TP18
TP19
R31
R22
C78
Q1
Q2
CR4
VR4
VR2
L12
L8
L9
L13
R113
C82
U3
U10
U9
R121
Q18
Q16
Q15
Q11
Q13
Q12
Q14
Q10
Q9
Q8
Q7
Q5
Q4
Q6
R80
R81
R78
R96
R101
L21
L25
C58
R100
R92
R83
R79
R77
R91
R85
R106
R107
C61
C63
C64
C65
C80
U11
R104
R63
R102
R108
TP15
R105
R62
C52
C51
C53
C50
C55
R68
R64
R65
R69
R70
R71
R61
R66
R74
R75
R67
CR6
CR5
CR7
C18
Q17
TP6
TP7
TP10
TP12
TP13
TP4
TP9
TP8
TP11
R72
R73
J1
C45
C46
R48
R47
R49
R53
R46
R52
R50
R51
R55
VR3
C47
C49
C48
R54
R56
R57
R59
R58
L20
L19
C56
K12
K3
K2
K10
K11
K1
C7
C6
C36
C1
R2
R7
R8
L11
R11
J2
U6
U7
U8
R38
L3
C16
L5
L6
L4
C18
C40
C42
C43
C41
C39
C44
C21
C17
C22
C19
R39
R40
R45
C20
L2
L1
R114
32
30
25
20
15
10
5
1
F111

Figure 7-5. A5 Wideband Output PCA (Option -03)

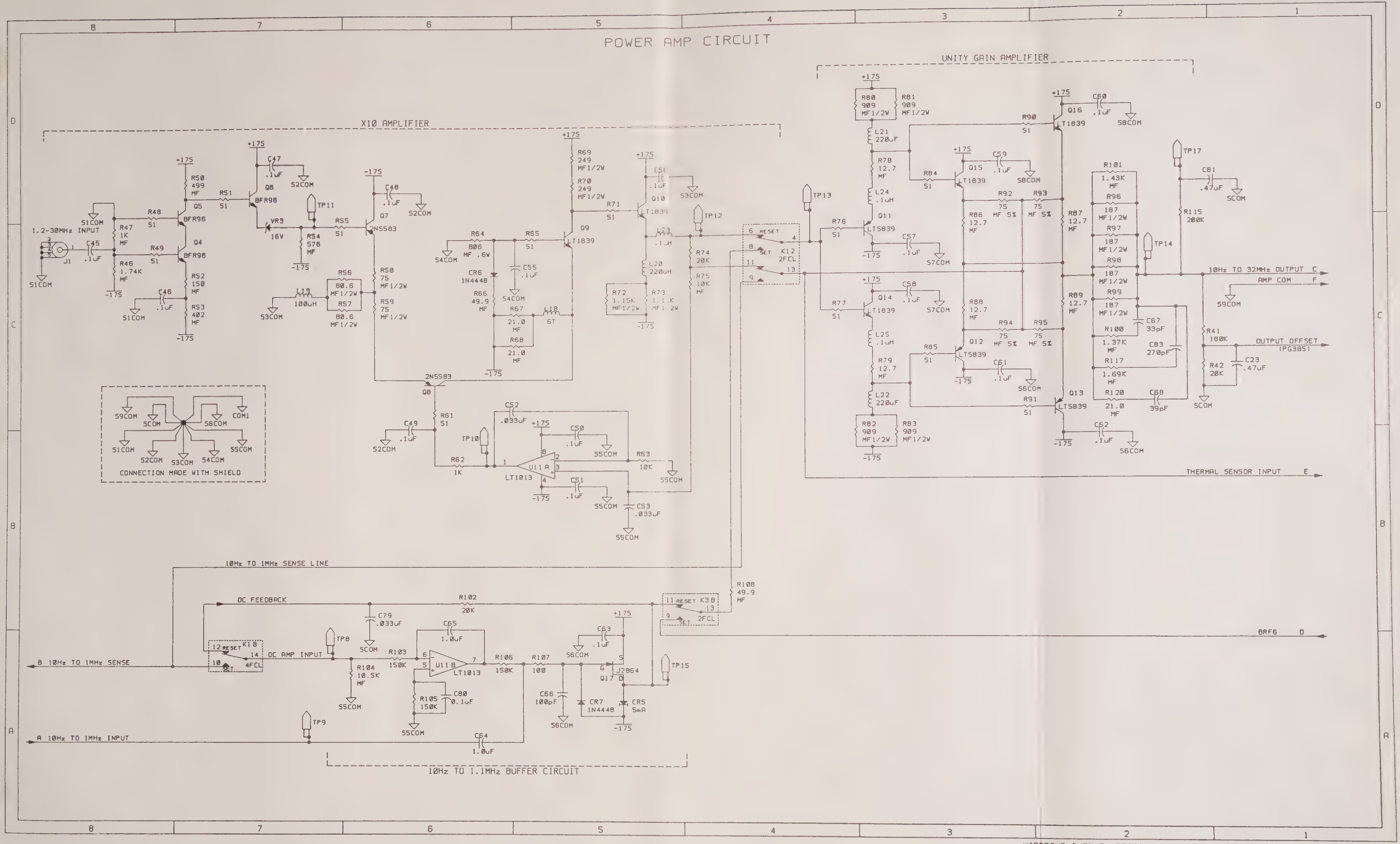

ATTENUATORS
10Hz TO 32MHz OUTPUT
FERRITE BEAD W1
POWER AMP CIRCUIT (SEE PG2)
10Hz TO 32MHz OUTPUT
AMP COM
10Hz TO 1MHz INPUT
10Hz TO 1MHz SENSE
BRF6
THERMAL SENSOR INPUT
P111
OSC OUT HI
OSC SENSE HI
OSC SENSE LO
DAC SENSE HI
DAC OUT HI
DAC OUT LO
R COM
BRF6
BSRF6
DAC OUT (PG1A3)
K1A
K11
K2A
K2B
K3A
K4 TO-5
K5 TO-5
K6 TO-5
K7 TO-5
K8 TO-5
K9
K10
J2
10/20DB ATTEN Z1
20/20DB ATTEN Z2
S9COM
RMS SENSOR AND AMPLITUDE CONTROL CIRCUIT
U2A LT1013
U2B LT1013
U12A LT1013
U12B LT1013
U3 CA3046
U1 RMS SENSOR
U5 OP-07
SENSOR CAL (PG3B5)
RCL
WB AMPLITUDE CONTROL
AMPLITUDE CONTROL DIAGNOSTICS (PG3B5)
DAC OUT (PG1D7)
OVERLOAD CONTROL CIRCUIT
U4A LM393
U4B LM393
PBO (PG3B6)
U9 ENABLE (PG3C5)
Q1 2N4401
Q2 SD210
Q3 SD210
CR1 1N4448
CR2 1N4448
CR3 1N4448
CR4 1N4448
VR1 9.1V
VR2 6.4V
VR4 5.6V
+17S
-17S
+5LH
SCOM
COM1
WIDEBAND OUTPUT 5700A-1011 1 OF 3 AUG.22,1988

TP1 = RMS SENSOR DC (PG1B4)
TP2 = RMS SENSOR OUTPUT (PG1B3)
TP3 = AMPLITUDE CONTROL (PG1B2)
TP4 = DAC OUT (PG1D7)
TP5 = OVERLOAD CONTROL (PG1B6)
TP6 = BRF6 (PG1D6)
TP7 = SENSOR INPUT (PG1D5)
TP8 = DC AMP INPUT (PG2A6)
TP9 = 10Hz-1MHz INPUT (PG2A7)
TP10 = X10 AMP BIAS 1 (PG2B6)
TP11 = X10 AMP BIAS 2 (PG2D7)
TP12 = X10 AMP OUTPUT (PG2C4)
TP13 = X1 AMP INPUT (PG2C4)
TP14 = 10Hz-1MHz OUTPUT (PG2C2)
TP15 = 10Hz-1.1MHz BUFFER (PG2A4)
TP16 = SCOM (PG1B8)
TP17 = OUTPUT OFFSET (PG2D1)
TP18 = AMPL. CONT. INPUT (PG1B3)
TP19 = COM1 (PG1A3)

NOTES:

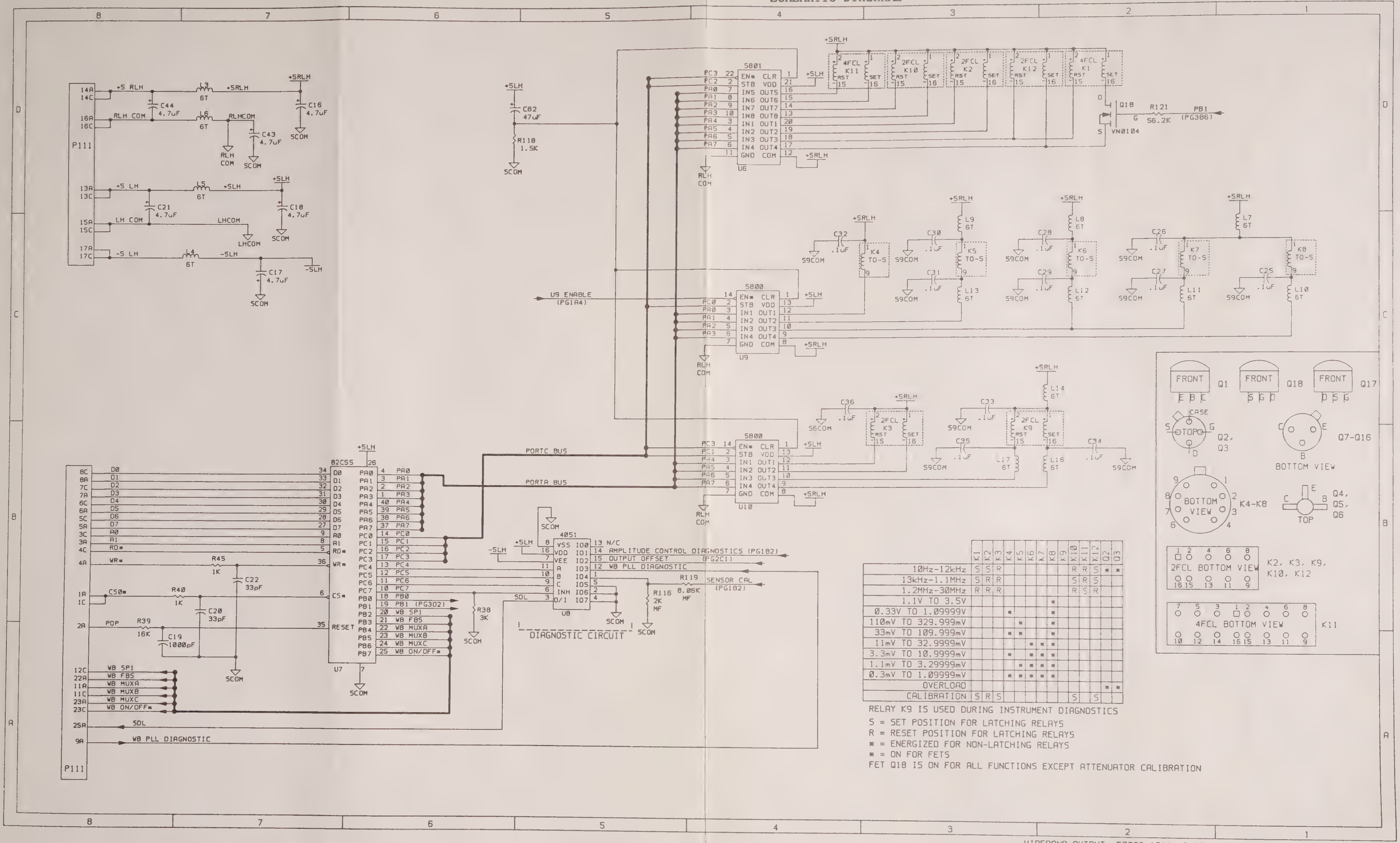
1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

Figure 7-5. A5 Wideband Output PCA (Option -03) (cont)


POWER AMP CIRCUIT
X10 AMPLIFIER
UNITY GAIN AMPLIFIER
1.2-30MHz INPUT
J1
S1COM
Q4 BFR96
Q5 BFR96
Q6 BFR96
VR3 16V
TP11
Q7 2N5583
Q8 2N5583
Q9 LT1839
Q10 LT1839
TP12
TP13
K12 2FCL
RESET
SET
Q11 LT5839
Q12 LT5839
Q13 LT5839
Q14 LT1839
Q15 LT1839
Q16 LT1839
TP14
TP17
10Hz TO 32MHz OUTPUT C
AMP COM F
OUTPUT OFFSET (PG385)
THERMAL SENSOR INPUT E
U11A LT1013
TP10
CONNECTION MADE WITH SHIELD
S9COM
SCOM
S6COM
COM1
S1COM
S2COM
S3COM
S4COM
S5COM
10Hz TO 1MHz SENSE LINE
DC FEEDBACK
K3B 2FCL
BRF6 D
K1B 4FCL
B 10Hz TO 1MHz SENSE
DC AMP INPUT
TP8
U11B LT1013
Q17 J2064
TP15
TP9
A 10Hz TO 1MHz INPUT
10Hz TO 1.1MHz BUFFER CIRCUIT
+175
-175

WIDEBAND OUTPUT 5700A-1011 2 OF 3 AUG.22.1988

Figure 7-5. A5 Wideband Output PCA (Option -03) (cont)


P111
14A
14C
16A
16C
13A
13C
15A
15C
17A
17C
+5 RLH
L3 6T
+SRLH
C44 4.7uF
C16 4.7uF
RLH COM
L6 6T
RLHCOM
C43 4.7uF
SCOM
+5 LH
L5 6T
+SLH
C21 4.7uF
C18 4.7uF
LH COM
LHCOM
-5 LH
L4 6T
-SLH
C17 4.7uF
C82 47uF
R118 1.5K
U6 5801
U9 5800
U10 5800
EN CLR
STB VDD
IN1 OUT1
GND COM
RLH COM
4FCL K11
2FCL K10
2FCL K2
2FCL K12
4FCL K1
RST SET
Q18 VN0104
R121 56.2K
PB1 (PG3B6)
U9 ENABLE (PG1A4)
K4 TO-5
K5 TO-5
K6 TO-5
K7 TO-5
K8 TO-5
L9 6T
L8 6T
L7 6T
L13 6T
L12 6T
L11 6T
L10 6T
C32 .1uF
C30 .1uF
C28 .1uF
C26 .1uF
C31 .1uF
C29 .1uF
C27 .1uF
C25 .1uF
S9COM
2FCL K3
2FCL K9
L14 6T
L17 6T
L16 6T
C36 .1uF
C33 .1uF
C35 .1uF
C34 .1uF
S6COM
PORTC BUS
PORTA BUS
82C55 U7
D0 D1 D2 D3 D4 D5 D6 D7
A0 A1
RD
WR
CS
RESET
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7
PB0 PB1 (PG3D2)
WB SP1
WB FBS
WB MUXA
WB MUXB
WB MUXC
WB ON/OFF
R45 1K
C22 33pF
R40 1K
C20 33pF
R39 16K
C19 1000pF
POP
CS0
R38 3K
4051 U8
VSS VDD VEE A B C INH O/I
N/C
AMPLITUDE CONTROL DIAGNOSTICS (PG1B2)
OUTPUT OFFSET (PG2C1)
WB PLL DIAGNOSTIC
SENSOR CAL (PG1B2)
R119 8.06K MF
R116 2K MF
DIAGNOSTIC CIRCUIT
SDL
WB PLL DIAGNOSTIC
12C 22A 11A 11C 23A 23C 25A 9A
FRONT Q1 E B C
FRONT Q18 S G D
FRONT Q17 D S G
CASE TOP S G D Q2, Q3
BOTTOM VIEW Q7-Q16
BOTTOM VIEW K4-K8
TOP Q4, Q5, Q6
2FCL BOTTOM VIEW K2, K3, K9, K10, K12
4FCL BOTTOM VIEW K11
8 7 6 5 4 3 2 1
D C B A

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	Q2	Q3
10Hz-12kHz	S	S	R							R	R	S	■	■
13kHz-1.1MHz	S	R	R							S	R	S		
1.2MHz-30MHz	R	R	R							R	S	R		
1.1V TO 3.5V								✱						
0.33V TO 1.09999V				✱				✱						
110mV TO 329.999mV					✱			✱						
33mV TO 109.999mV				✱	✱			✱						
11mV TO 32.9999mV						✱	✱	✱						
3.3mV TO 10.9999mV				✱		✱	✱	✱						
1.1mV TO 3.29999mV					✱	✱	✱	✱						
0.3mV TO 1.09999mV				✱	✱	✱	✱	✱						
OVERLOAD													■	■
CALIBRATION	S	R	S							S		S		

RELAY K9 IS USED DURING INSTRUMENT DIAGNOSTICS

S = SET POSITION FOR LATCHING RELAYS
R = RESET POSITION FOR LATCHING RELAYS
✱ = ENERGIZED FOR NON-LATCHING RELAYS
■ = ON FOR FETS
FET Q18 IS ON FOR ALL FUNCTIONS EXCEPT ATTENUATOR CALIBRATION

WIDEBAND OUTPUT 5700A-1011 3 OF 3 AUG.22,1988

Figure 7-5. A5 Wideband Output PCA
(Option -03) (cont)

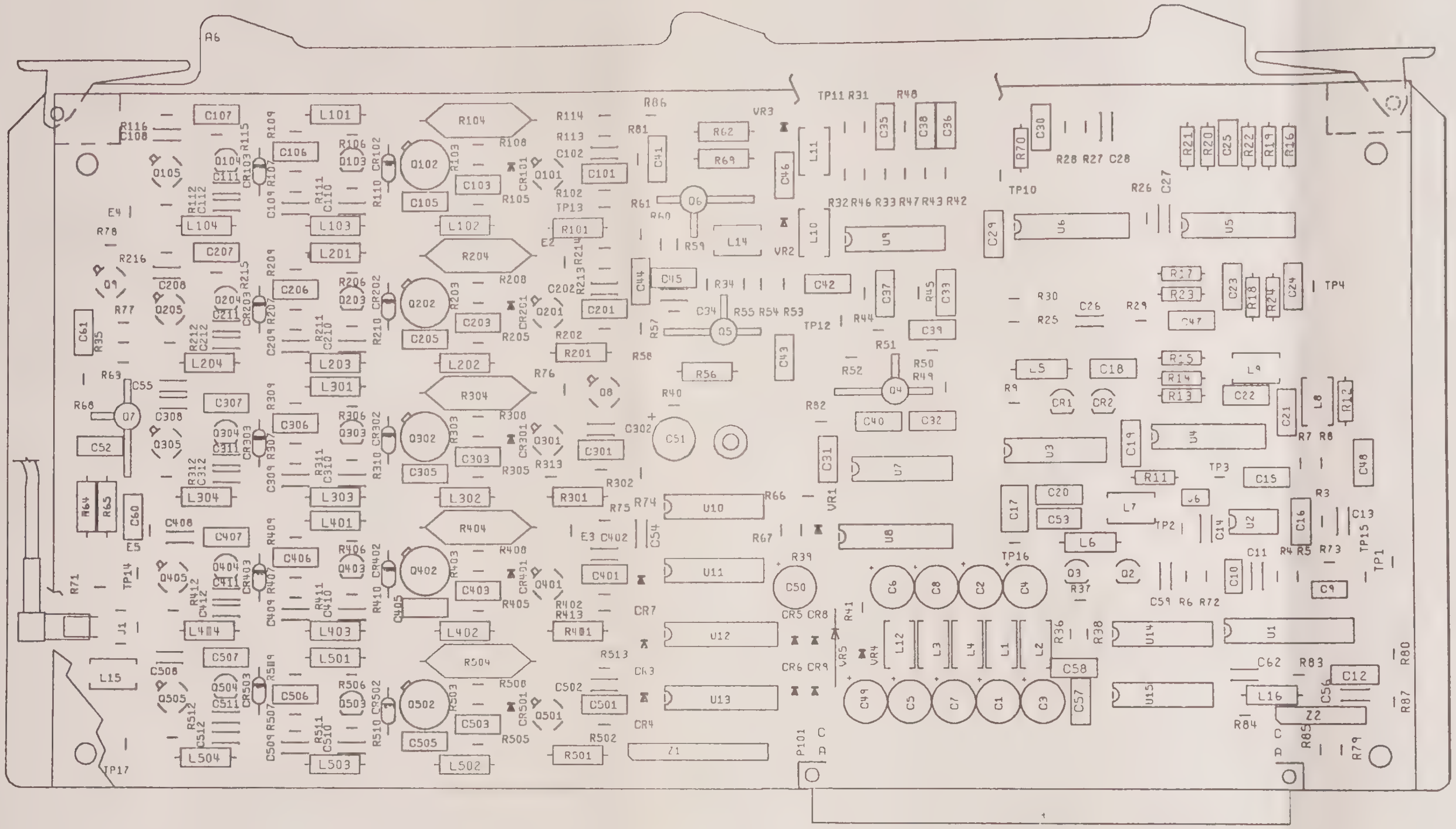
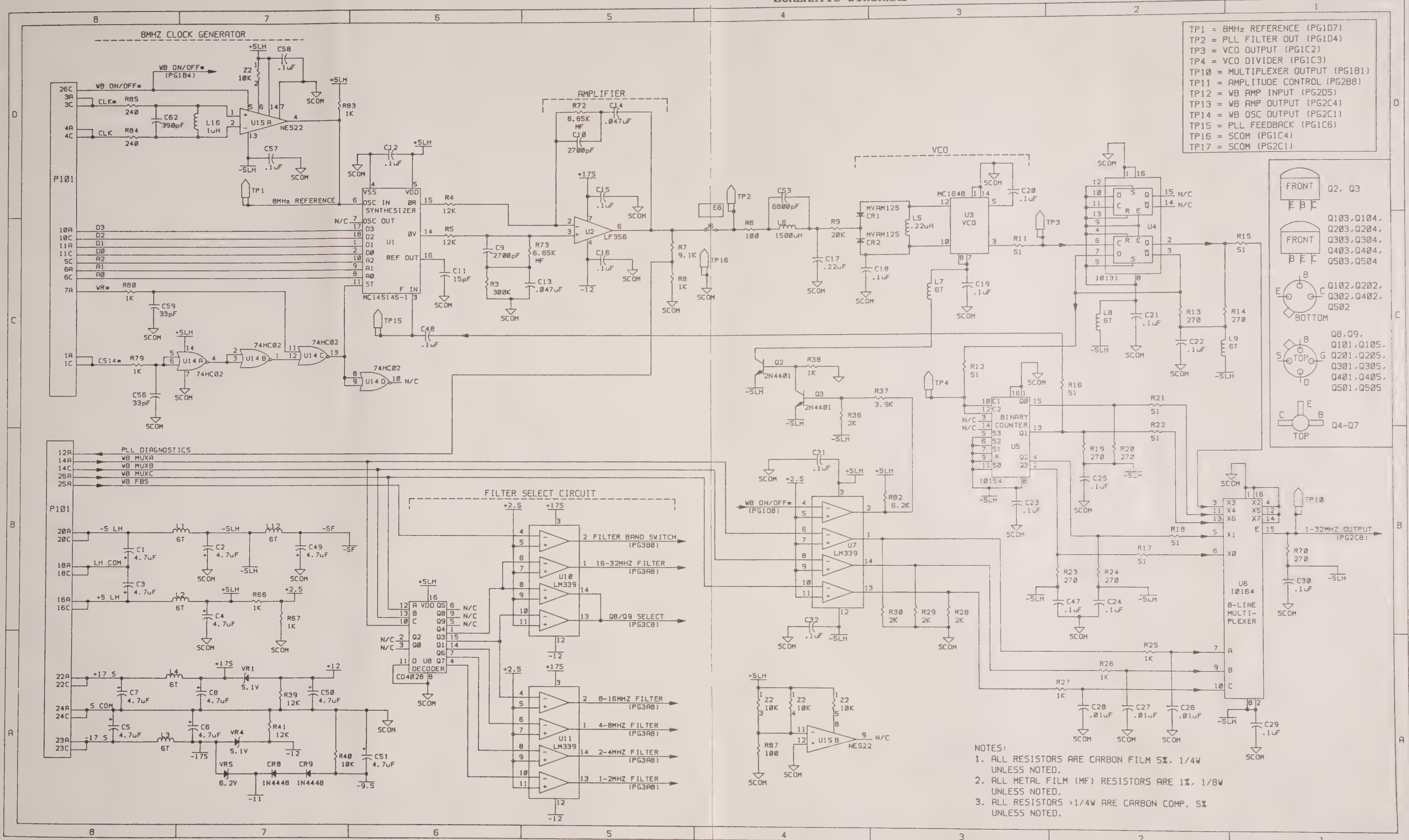

A6
R116
C108
C107
R109
L101
R104
R114
R86
TP11 R31
R48
C35
C38
C36
R70
C30
R28 R27 C28
R21
R20
C25
R22
R19
R16
Q105
Q104
C106
R106
Q103
Q102
R108
R113
R81
R62
VR3
C102
C41
R69
L11
C101
Q101
C103
R105
C105
R102
TP13
R61
Q6
C46
R32 R46 R33 R47 R43 R42
TP10
R26
C27
E4
R78
L104
L103
L102
R101
R40
L14
U9
C29
U6
U5
R216
C207
L201
R204
R213
R214
R59
L10
VR2
Q4
C208
Q205
C206
R206
Q203
Q202
R208
C202
C44
C15
R34
C42
C37
R45
C33
R17
R23
C23
R18
R24
C24
TP4
R77
C211
Q201
C201
C34
Q5
R55 R54 R53
R30
C26
R29
C47
R25
C61
R35
L204
C203
C205
R205
R202
R57
TP12
R44
C39
R63
C55
L203
L202
R201
R58
R56
R51
R50
R49
R52
C43
L5
C18
R15
R14
R13
L9
C22
R9
CR1
CR2
L8
R12
R68
Q7
C308
C307
L301
R304
R76
Q8
R40
Q4
R82
C40
C32
C21
C52
Q305
C306
R306
Q303
Q302
R300
Q301
C302
C301
C51
C31
U7
U3
U4
C19
R7 R8
C48
C311
C303
R305
R313
R11
TP3
C15
R64
R65
C60
L304
L303
L302
R302
R301
R74
U10
R66
VR1
C17
C20
L7
L6
U2
R3
C16
C13
C408
L401
R404
R75
C54
C53
TP2
C14
TP15
C407
C406
R406
Q403
Q402
R408
E3
C402
R67
U8
L6
E5
R71
TP14
Q405
C411
C403
R405
Q401
C401
U11
R39
C50
C6
C8
C2
C4
TP16
Q3
R37
Q2
C11
R4
R5
R73
C10
C9
TP1
R402
R413
CR7
CR5
CR8
C59
R6
R72
J1
L404
L403
L402
R401
R41
U12
L12
L3
L4
L1
L2
R36
R38
U14
U1
C507
L501
R504
R513
C63
VR5
VR4
CR6
CR9
C58
C62
R83
C12
R80
L15
C508
C506
R506
Q503
Q502
R508
C502
C501
U13
C49
C5
C7
C1
C3
C57
U15
L16
C56
R87
Q505
Q504
C511
C503
R505
Q501
CR4
R84
Z2
R502
P101
R85
R79
L504
L503
C505
L502
R501
Z1
TP17

Figure 7-6. A6 Wideband Oscillator PCA (Option -03)


TP1 = 8MHz REFERENCE (PG1D7)
TP2 = PLL FILTER OUT (PG1D4)
TP3 = VCO OUTPUT (PG1C2)
TP4 = VCO DIVIDER (PG1C3)
TP10 = MULTIPLEXER OUTPUT (PG1B1)
TP11 = AMPLITUDE CONTROL (PG2B8)
TP12 = WB AMP INPUT (PG2D5)
TP13 = WB AMP OUTPUT (PG2C4)
TP14 = WB OSC OUTPUT (PG2C1)
TP15 = PLL FEEDBACK (PG1C6)
TP16 = SCOM (PG1C4)
TP17 = SCOM (PG2C1)
8MHZ CLOCK GENERATOR
AMPLIFIER
VCO
FILTER SELECT CIRCUIT
P101
WB ON/OFF* (PG1B4)
8MHz REFERENCE
U15A NE522
U1 MC145145-1 SYNTHESIZER
U2 LF356
U3 MC1648 VCO
U4 10131
U5 10154 BINARY COUNTER
U6 10164 8-LINE MULTI-PLEXER
U7 LM339
U8 CD4028 DECODER
U10 LM339
U11 LM339
U14 74HC02
U15B NE522
PLL DIAGNOSTICS
WB MUXA
WB MUXB
WB MUXC
WB FBS
2 FILTER BAND SWITCH (PG3B8)
1 16-32MHZ FILTER (PG3A8)
Q8/Q9 SELECT (PG3C8)
8-16MHZ FILTER (PG3A8)
4-8MHZ FILTER (PG3A8)
2-4MHZ FILTER (PG3A8)
1-2MHZ FILTER (PG3A8)
1-32MHZ OUTPUT (PG2C8)
WB ON/OFF* (PG1D8)
FRONT Q2, Q3
FRONT Q103, Q104, Q203, Q204, Q303, Q304, Q403, Q404, Q503, Q504
BOTTOM Q102, Q202, Q302, Q402, Q502
TOP Q8, Q9, Q101, Q105, Q201, Q205, Q301, Q305, Q401, Q405, Q501, Q505
TOP Q4-Q7

NOTES:

1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.
3. ALL RESISTORS >1/4W ARE CARBON COMP. 5% UNLESS NOTED.

WIDEBAND OSCILLATOR 5700A-1010 1 OF 3 AUG.19.1988

Figure 7-6. A6 Wideband Oscillator PCA (Option -03) (cont)

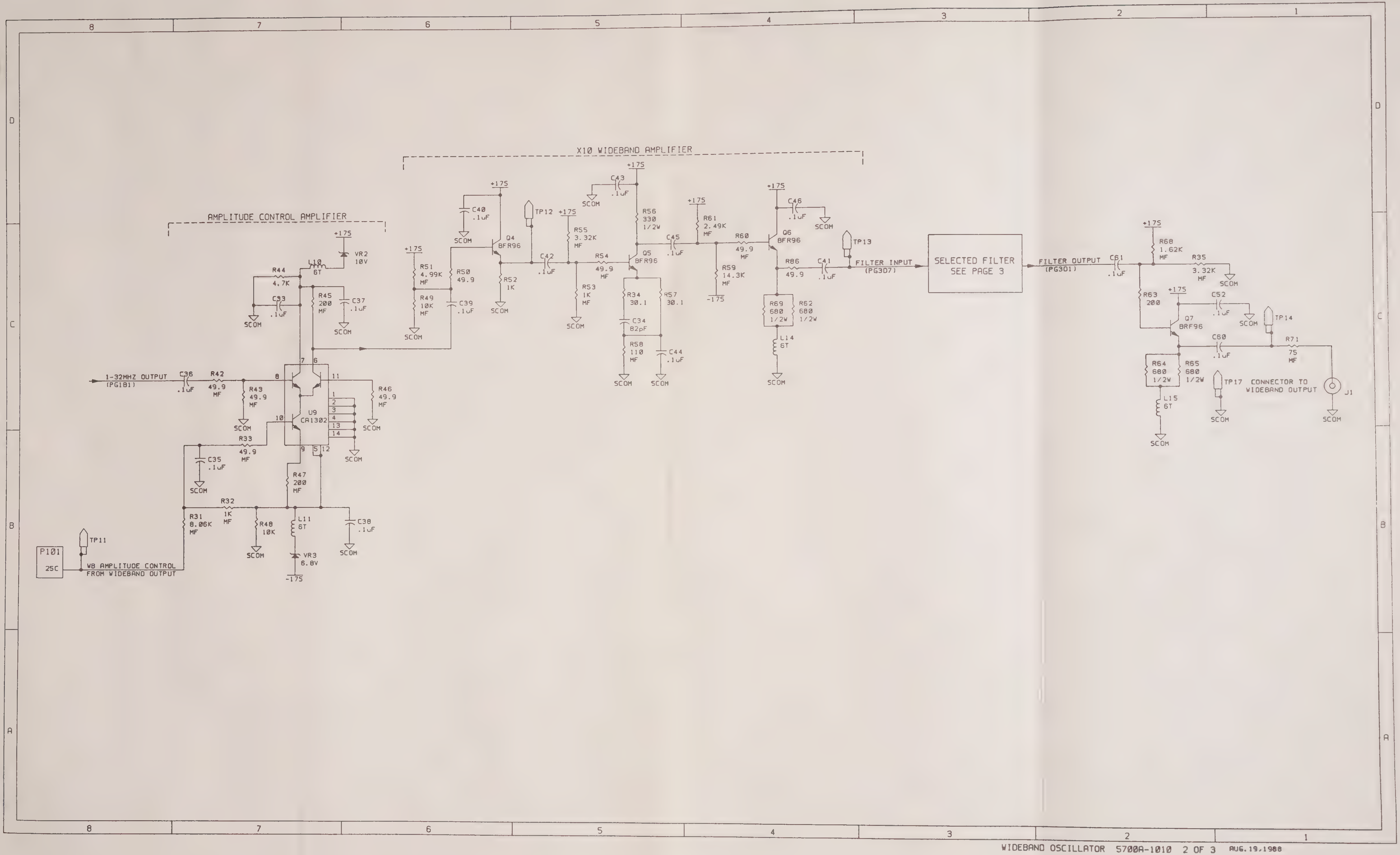

X10 WIDEBAND AMPLIFIER
AMPLITUDE CONTROL AMPLIFIER
+17S
SCOM
-17S
1-32MHZ OUTPUT
(PG181)
C36 .1uF
R42 49.9 MF
R43 49.9 MF
R44 4.7K
L10 6T
VR2 10V
C33 .1uF
R45 200 MF
C37 .1uF
U9 CA1302
R46 49.9 MF
R33 49.9 MF
C35 .1uF
R47 200 MF
R31 8.06K MF
R32 1K MF
R48 10K
L11 6T
VR3 6.8V
C38 .1uF
TP11
P101
25C
WB AMPLITUDE CONTROL
FROM WIDEBAND OUTPUT
R51 4.99K MF
R49 10K MF
R50 49.9
C39 .1uF
C40 .1uF
Q4 BFR96
R52 1K
TP12
C42 .1uF
R55 3.32K MF
R53 1K MF
R54 49.9 MF
C43 .1uF
R56 330 1/2W
Q5 BFR96
R34 30.1
R57 30.1
C34 82pF
R58 110 MF
C44 .1uF
C45 .1uF
R61 2.49K MF
R59 14.3K MF
R60 49.9 MF
Q6 BFR96
C46 .1uF
TP13
R86 49.9
C41 .1uF
R69 680 1/2W
R62 680 1/2W
L14 6T
FILTER INPUT
(PG307)
SELECTED FILTER
SEE PAGE 3
FILTER OUTPUT
(PG301)
C61 .1uF
R68 1.62K MF
R35 3.32K MF
R63 200
C52 .1uF
Q7 BFR96
TP14
C60 .1uF
R71 75 MF
R64 680 1/2W
R65 680 1/2W
L15 6T
TP17
CONNECTOR TO
WIDEBAND OUTPUT
J1
WIDEBAND OSCILLATOR 5700A-1010 2 OF 3 AUG.19.1988

Figure 7-6. A6 Wideband Oscillator PCA (Option -03) (cont)

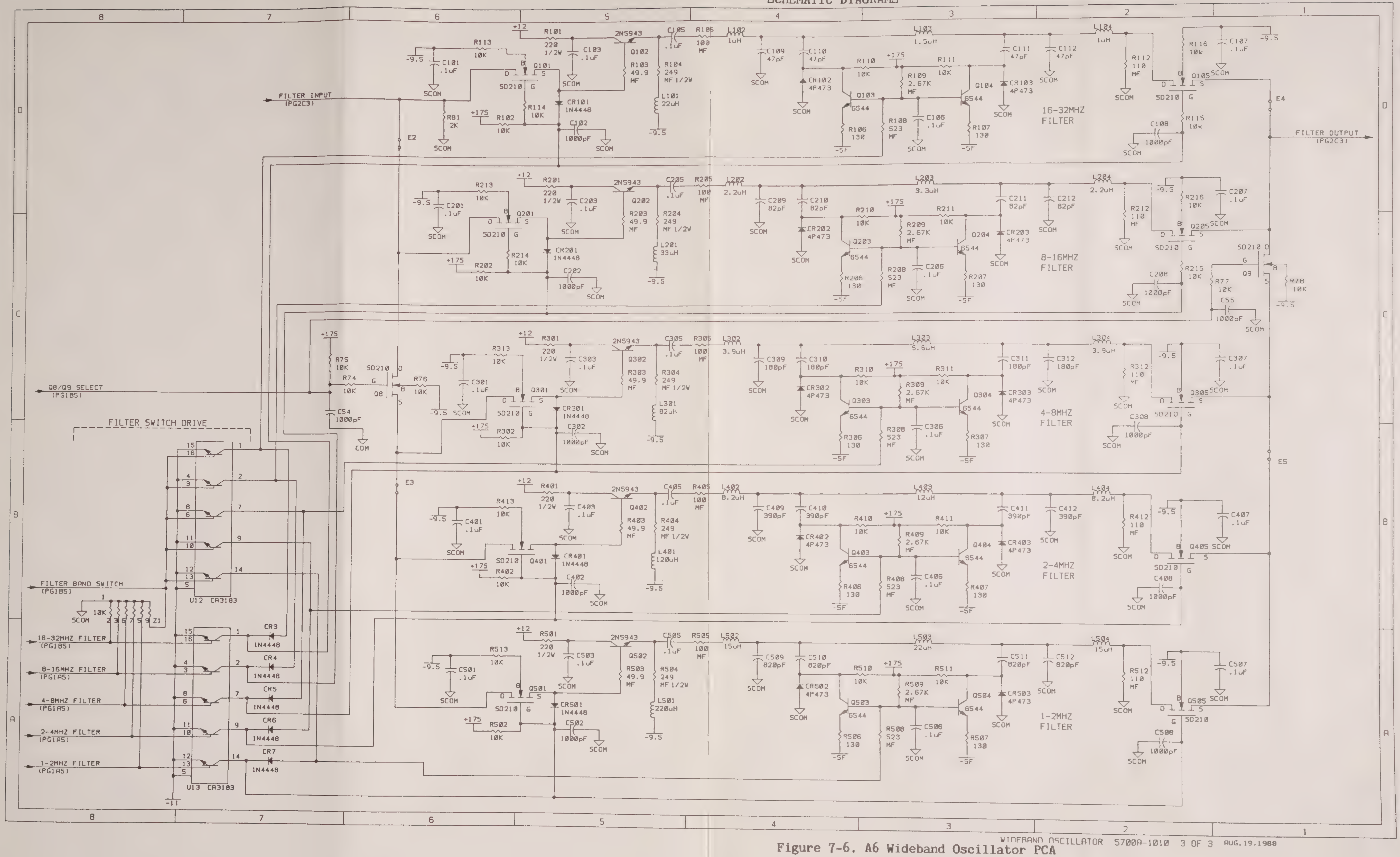

8
7
6
5
4
3
2
1
D
C
B
A
FILTER INPUT
(PG2C3)
FILTER OUTPUT
(PG2C3)
Q8/Q9 SELECT
(PG1B5)
FILTER SWITCH DRIVE
FILTER BAND SWITCH
(PG1B5)
16-32MHZ FILTER
(PG1B5)
8-16MHZ FILTER
(PG1A5)
4-8MHZ FILTER
(PG1A5)
2-4MHZ FILTER
(PG1A5)
1-2MHZ FILTER
(PG1A5)
U12 CA3183
U13 CA3183
CR3
CR4
CR5
CR6
CR7
1N4448
Z1
10K
SCOM
-11
E2
E3
E4
E5
R75
10K
R74
10K
R76
10K
SD210
Q8
C54
1000pF
COM
SD210
Q9
R77
10K
R78
10K
C55
1000pF
R81
2K
+12
+175
-9.5
-5F
R101
220
1/2W
2N5943
Q101
Q102
R103
49.9
MF
R104
249
MF 1/2W
L101
22uH
C105
.1uF
R105
100
MF
L102
1uH
L103
1.5uH
L104
1uH
C109
47pF
C110
47pF
C111
47pF
C112
47pF
CR102
4P473
CR103
4P473
Q103
Q104
6544
R106
130
R107
130
R108
523
MF
R109
2.67K
MF
R110
10K
R111
10K
C106
.1uF
R112
110
MF
R116
10k
C107
.1uF
Q105
R115
10k
C108
1000pF
R113
10K
C101
.1uF
C103
.1uF
R114
10K
R102
10K
CR101
1N4448
C102
1000pF
16-32MHZ
FILTER
R201
220
1/2W
Q201
Q202
R213
10K
C201
.1uF
C203
.1uF
R203
49.9
MF
R204
249
MF 1/2W
L201
33uH
C205
.1uF
R205
100
MF
L202
2.2uH
L203
3.3uH
L204
2.2uH
C209
82pF
C210
82pF
C211
82pF
C212
82pF
CR202
4P473
CR203
4P473
Q203
Q204
R206
130
R207
130
R208
523
MF
R209
2.67K
MF
R210
10K
R211
10K
C206
.1uF
R212
110
MF
R216
10K
C207
.1uF
Q205
R215
10K
C208
1000pF
R214
10K
R202
10K
CR201
1N4448
C202
1000pF
8-16MHZ
FILTER
R301
220
1/2W
Q301
Q302
R313
10K
C301
.1uF
C303
.1uF
R303
49.9
MF
R304
249
MF 1/2W
L301
82uH
C305
.1uF
R305
100
MF
L302
3.9uH
L303
5.6uH
L304
3.9uH
C309
180pF
C310
180pF
C311
180pF
C312
180pF
CR302
4P473
CR303
4P473
Q303
Q304
R306
130
R307
130
R308
523
MF
R309
2.67K
MF
R310
10K
R311
10K
C306
.1uF
R312
110
MF
C307
.1uF
Q305
C308
1000pF
R302
10K
CR301
1N4448
C302
1000pF
4-8MHZ
FILTER
R401
220
1/2W
Q401
Q402
R413
10K
C401
.1uF
C403
.1uF
R403
49.9
MF
R404
249
MF 1/2W
L401
120uH
C405
.1uF
R405
100
MF
L402
8.2uH
L403
12uH
L404
8.2uH
C409
390pF
C410
390pF
C411
390pF
C412
390pF
CR402
4P473
CR403
4P473
Q403
Q404
R406
130
R407
130
R408
523
MF
R409
2.67K
MF
R410
10K
R411
10K
C406
.1uF
R412
110
MF
C407
.1uF
Q405
C408
1000pF
R402
10K
CR401
1N4448
C402
1000pF
2-4MHZ
FILTER
R501
220
1/2W
Q501
Q502
R513
10K
C501
.1uF
C503
.1uF
R503
49.9
MF
R504
249
MF 1/2W
L501
220uH
C505
.1uF
R505
100
MF
L502
15uH
L503
22uH
L504
15uH
C509
820pF
C510
820pF
C511
820pF
C512
820pF
CR502
4P473
CR503
4P473
Q503
Q504
R506
130
R507
130
R508
523
MF
R509
2.67K
MF
R510
10K
R511
10K
C506
.1uF
R512
110
MF
C507
.1uF
Q505
C508
1000pF
R502
10K
CR501
1N4448
C502
1000pF
1-2MHZ
FILTER
WIDEBAND OSCILLATOR 5700A-1010 3 OF 3 AUG.19.1988

Figure 7-6. A6 Wideband Oscillator PCA
(Option -03) (cont)

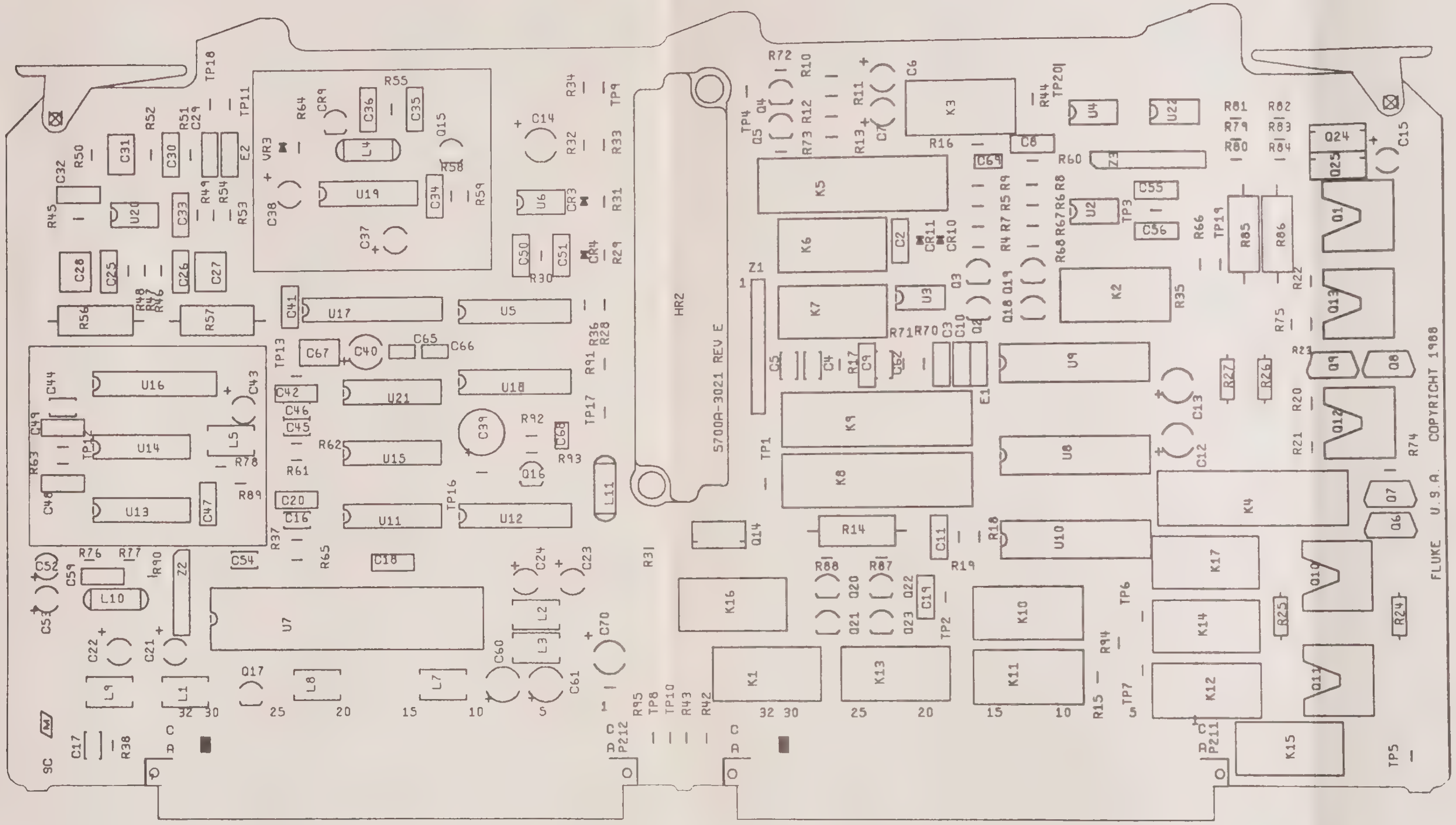
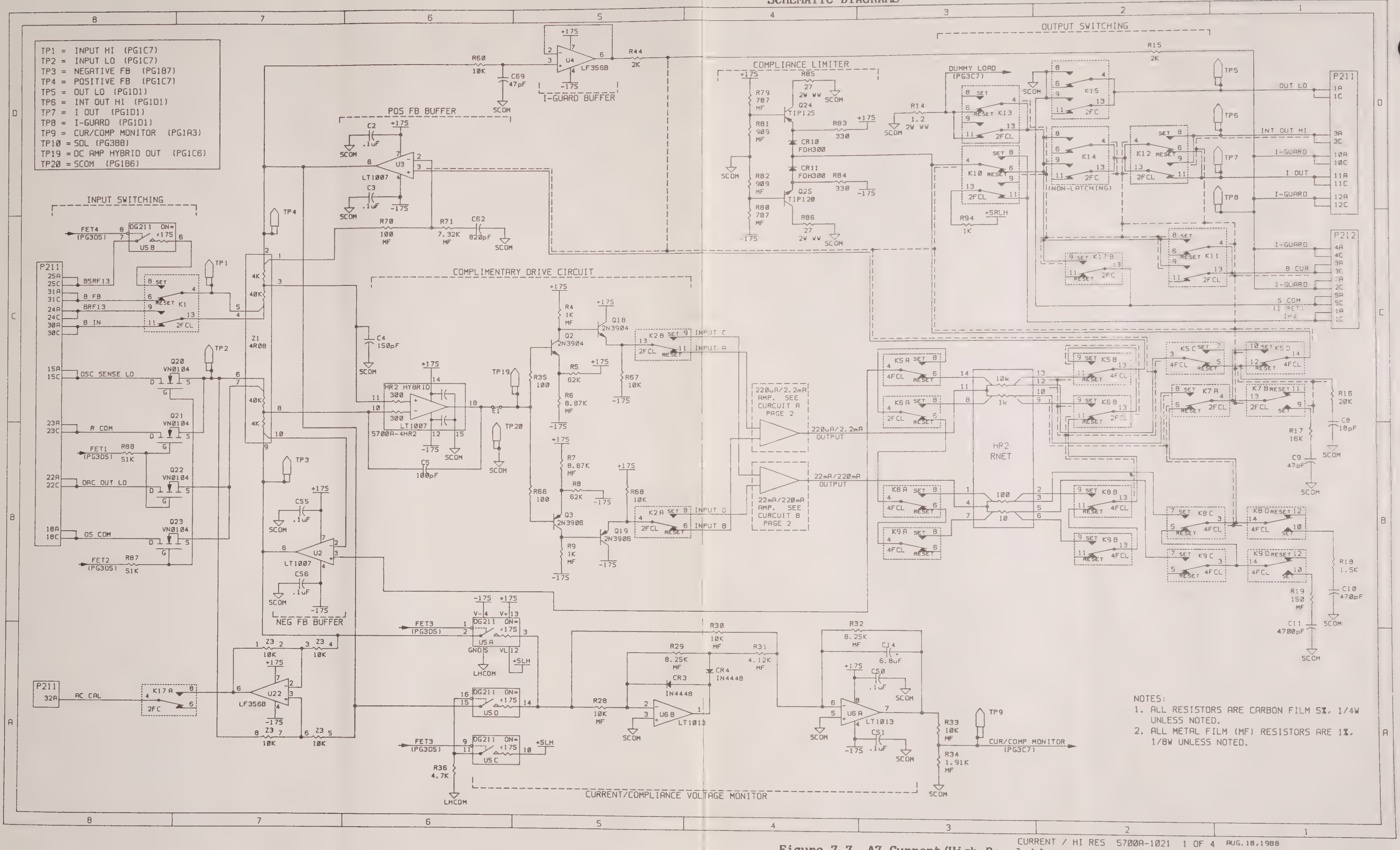

TP18
TP11
R55
R64
CR9
C36
C35
R34
TP9
R72
R10
C6
TP20
R44
R81
R82
R79
R83
R80
R84
Q24
Q25
C15
R52
R51
C29
C31
C30
E2
VR3
L4
Q15
C14
R32
R33
Q5
Q4
TP4
R12
R11
R13
C7
K3
U4
U22
R16
C8
R73
R60
Z3
C69
C32
R50
R45
U20
C33
R49
R54
R53
C38
U19
R58
C34
R59
U6
CR3
R31
K5
R4
R7
R5
R9
R68
R67
R6
R8
U2
TP3
C55
C56
R66
TP19
R85
R86
Q1
C37
C28
C25
C26
C27
R48
R47
R46
C50
C51
C44
R29
R30
HR2
5700A-3021 REV E
Z1
K6
C2
CR11
CR10
Q3
Q19
Q18
K2
R35
R22
Q13
R56
R57
C41
U17
U5
R36
R28
K7
U3
R71
R70
C3
C10
Q2
R75
TP13
C67
C40
C65
C66
R91
C5
C4
R17
C9
C52
E1
U9
R27
R26
R23
Q9
Q8
C44
U16
C43
C42
U21
U18
TP17
R20
COPYRIGHT 1988
C49
C46
C45
C39
R92
C13
TP12
U14
L5
R62
U15
C68
K9
U8
C12
Q12
R63
R78
R61
R93
Q16
TP1
R21
R74
C48
U13
C47
R89
C20
C16
TP16
U11
U12
L11
K8
K4
U.S.A.
Q7
Q6
R76
R77
R90
Z2
R37
R65
C54
C18
C24
C23
R31
Q14
R14
C11
R18
U10
C52
C59
L10
R88
R87
R19
K17
FLUKE
Q10
C53
C22
C21
U7
L2
K16
Q20
Q21
Q22
Q23
C19
TP2
K10
TP6
K14
R25
R24
L9
L1
Q17
L8
L7
C60
L3
C70
C61
K1
K13
K11
R94
K12
Q11
32 30
25
20
15
10
5
1
R95
TP8
TP10
R43
R42
R15
TP7
C17
R38
P212
P211
K15
TP5

Figure 7-7. A7 Current/High-Resolution
Oscillator PCA (cont)

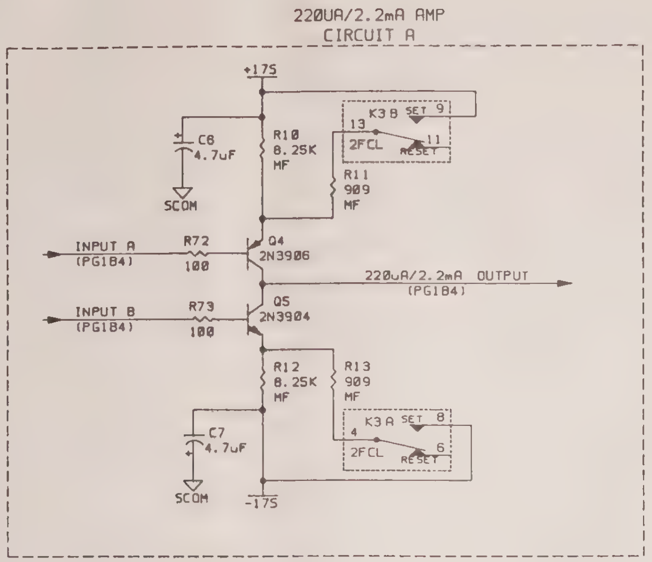


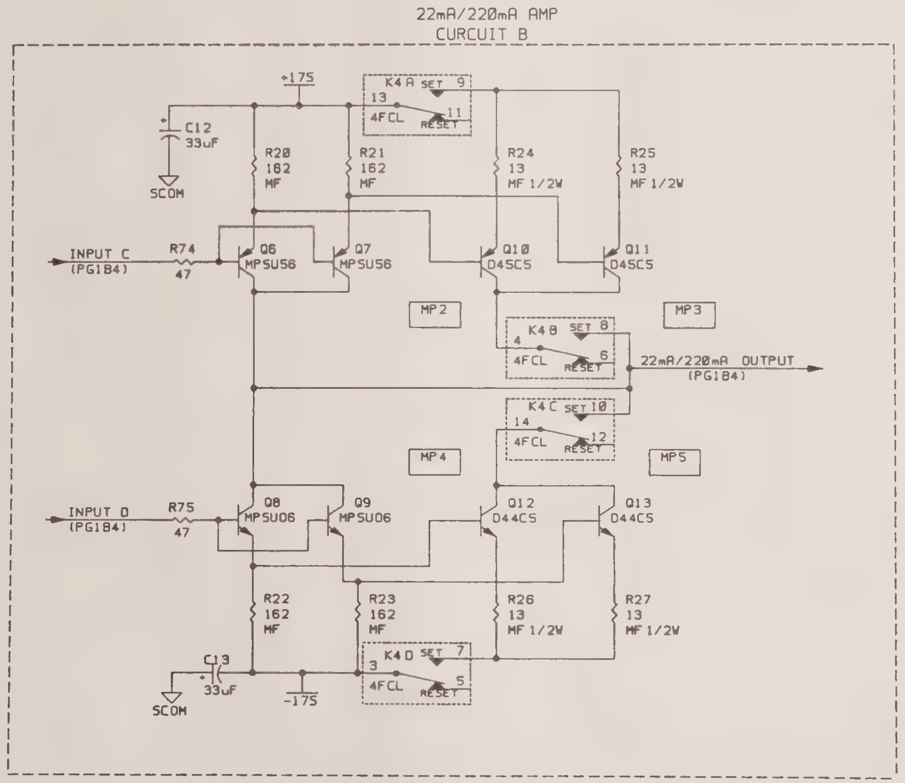
TP1 = INPUT HI (PG1C7)
TP2 = INPUT LO (PG1C7)
TP3 = NEGATIVE FB (PG1B7)
TP4 = POSITIVE FB (PG1C7)
TP5 = OUT LO (PG1D1)
TP6 = INT OUT HI (PG1D1)
TP7 = I OUT (PG1D1)
TP8 = I-GUARD (PG1D1)
TP9 = CUR/COMP MONITOR (PG1A3)
TP10 = SDL (PG3B8)
TP19 = DC AMP HYBRID OUT (PG1C6)
TP20 = SCOM (PG1B6)

NOTES:
1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

8
7
6
5
4
3
2
1
D
C
B
A
INPUT SWITCHING
POS FB BUFFER
I-GUARD BUFFER
COMPLIANCE LIMITER
OUTPUT SWITCHING
COMPLIMENTARY DRIVE CIRCUIT
NEG FB BUFFER
CURRENT/COMPLIANCE VOLTAGE MONITOR
DUMMY LOAD (PG3C7)
(NON-LATCHING)
P211
P212
FET4 (PG3D5)
FET1 (PG3D5)
FET2 (PG3D5)
FET3 (PG3D5)
BSRF13
B FB
BRF13
B IN
OSC SENSE LO
R COM
DAC OUT LO
OS COM
AC CAL
U5 B
U5 A
U5 C
U5 D
DG211
K1
K2 A
K2 B
K5 A
K5 B
K5 C
K5 D
K6 A
K6 B
K7 A
K7 B
K8 A
K8 B
K8 C
K8 D
K9 A
K9 B
K9 C
K9 D
K10
K11
K12
K13
K14
K15
K17 A
K17 B
Q18 2N3904
Q2 2N3904
Q3 2N3906
Q19 2N3906
Q20 VN0104
Q21 VN0104
Q22 VN0104
Q23 VN0104
Q24 TIP125
Q25 TIP120
CR10 FDH300
CR11 FDH300
CR3 IN4448
CR4 IN4448
U2 LT1007
U3 LT1007
U4 LF356B
U22 LF356B
U6 A LT1013
U6 B LT1013
HR2 HYBRID
LT1007
5700A-4HR2
HR2 RNET
Z1 4R08
Z3
220uA/2.2mA AMP. SEE CURCUIT A PAGE 2
220uA/2.2mA OUTPUT
22mA/220mA AMP. SEE CURCUIT B PAGE 2
22mA/220mA OUTPUT
INPUT A
INPUT B
INPUT C
INPUT D
OUT LO
INT OUT HI
I-GUARD
I OUT
B CUR
S COM
CUR/COMP MONITOR (PG3C7)
SCOM
LHCOM
+17S
-17S
+SLH
+SRLH
R14 1.2 2W WW
R15 2K
R44 2K
R60 10K
C69 47pF
R70 100 MF
R71 7.32K MF
C62 820pF
C2 .1uF
C3 .1uF
C4 150pF
C5 100pF
C55 .1uF
C56 .1uF
R79 787 MF
R80 787 MF
R81 909 MF
R82 909 MF
R83 330
R84 330
R85 27 2W WW
R86 27 2W WW
R94 1K
R4 1K MF
R5 62K
R6 8.87K MF
R7 8.87K MF
R8 62K
R9 1K MF
R35 100
R66 100
R67 10K
R68 10K
R87 51K
R88 51K
R16 20K
R17 16K
R18 1.5K
R19 150 MF
C8 10pF
C9 47pF
C10 470pF
C11 4700pF
R28 10K MF
R29 8.25K MF
R30 10K MF
R31 4.12K MF
R32 8.25K MF
R33 10K MF
R34 1.91K MF
R36 4.7K
C14 6.8uF
C50 .1uF
C51 .1uF
CURRENT / HI RES 5700A-1021 1 OF 4 AUG.18,1988

Figure 7-7. A7 Current/High-Resolution Oscillator PCA (cont)

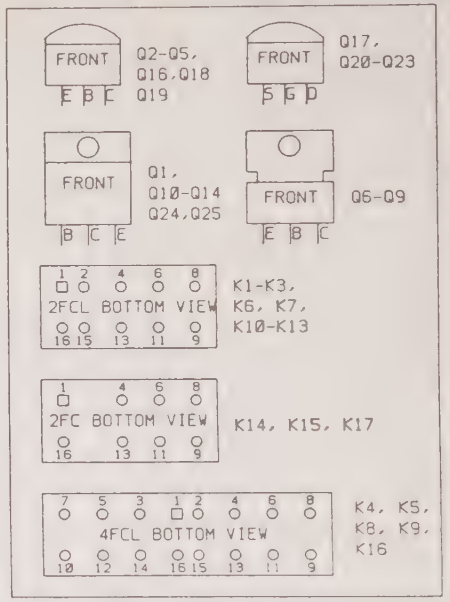

220UA/2.2mA AMP
CIRCUIT A
+17S
C6
4.7uF
SCOM
R10
8.25K
MF
K3 B
SET
9
13
2FCL
11
RESET
R11
909
MF
INPUT A
(PG1B4)
R72
100
Q4
2N3906
220uA/2.2mA OUTPUT
(PG1B4)
INPUT B
(PG1B4)
R73
100
Q5
2N3904
R12
8.25K
MF
R13
909
MF
K3 A
SET
8
4
2FCL
6
RESET
C7
4.7uF
SCOM
-17S

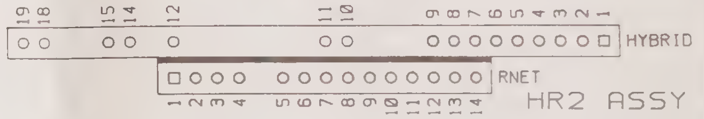

22mA/220mA AMP
CURCUIT B
+17S
K4 A
SET
9
13
4FCL
11
RESET
C12
33uF
SCOM
R20
162
MF
R21
162
MF
R24
13
MF 1/2W
R25
13
MF 1/2W
INPUT C
(PG1B4)
R74
47
Q6
MPSU56
Q7
MPSU56
Q10
D45C5
Q11
D45C5
MP2
MP3
K4 B
SET
8
4
4FCL
6
RESET
22mA/220mA OUTPUT
(PG1B4)
K4 C
SET
10
14
4FCL
12
RESET
MP4
MP5
INPUT D
(PG1B4)
R75
47
Q8
MPSU06
Q9
MPSU06
Q12
D44C5
Q13
D44C5
R22
162
MF
R23
162
MF
R26
13
MF 1/2W
R27
13
MF 1/2W
C13
33uF
SCOM
-17S
K4 D
SET
7
3
4FCL
5
RESET

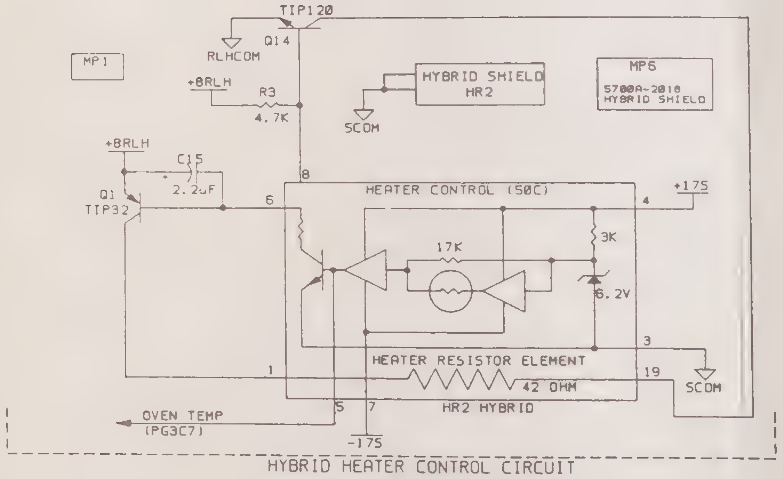
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	Q20/Q23	Q21/Q22	U5A/U5C	U5D
PWR-UP / RESET																					
DC 220uA RANGE														✱	✱				✱		
DC 2.2mA RANGE			S		S	S	S							✱	✱				✱		
DC 22mA RANGE		S			S			S						✱	✱				✱		
DC 220mA RANGE		S		S	S				S					✱	✱				✱		
DC 2.2A RANGE		S			S					S	S			✱	✱				✱		
AC 220uA RANGE														✱	✱			✱			
AC 2.2mA RANGE			S		S	S	S							✱	✱			✱			
AC 22mA RANGE		S			S			S						✱	✱			✱			
AC 220mA RANGE		S		S	S				S					✱	✱			✱			
AC 2.2A RANGE		S			S					S	S			✱	✱			✱			

ALL RELAYS SHOWN IN THE RESET OR NON-LATCHING POSITION
S = SET POSITION OF LATCHING RELAYS
✱ = ENERGIZED FOR NON-LATCHING RELAYS
✱ = ON FOR FETS
K1 IS SET DURING CURRENT GAIN CALIBRATION
K12 IS SET WHEN CURRENT OUTPUT IS AT THE OUT HI BINDING POST OR RESET WHEN CURRENT OUTPUT IS AT THE AUX I OUT BINDING POST
K13 CONNECTS A DUMMY LOAD TO THE OUTPUT CURRENT WHEN RESET. THIS IS DONE DURING DIAGNOSTICS AND CURRENT RANGE SWITCHING

K16 IS SET DURING BOOST AMPLIFIER CALIBRATION
K17 IS ENERGIZED DURING AC CURRENT FLATNESS CHARACTERIZATION


FRONT
E B C
Q2-Q5,
Q16,Q18
Q19
FRONT
S G D
Q17,
Q20-Q23
FRONT
B C E
Q1,
Q10-Q14
Q24,Q25
FRONT
E B C
Q6-Q9
1 2 4 6 8
2FCL BOTTOM VIEW
16 15 13 11 9
K1-K3,
K6, K7,
K10-K13
1 4 6 8
2FC BOTTOM VIEW
16 13 11 9
K14, K15, K17
7 5 3 1 2 4 6 8
4FCL BOTTOM VIEW
10 12 14 16 15 13 11 9
K4, K5,
K8, K9,
K16


19 18 15 14 12 11 10 9 8 7 6 5 4 3 2 1
HYBRID
RNET
1 2 3 4 5 6 7 8 9 10 11 12 13 14
HR2 ASSY


MP1
TIP120
Q14
RLHCOM
+BRLH
R3
4.7K
SCOM
HYBRID SHIELD
HR2
MP6
5700A-2010
HYBRID SHIELD
+BRLH
C15
2.2uF
Q1
TIP32
8
6
HEATER CONTROL (50C)
4
+17S
17K
3K
6.2V
3
HEATER RESISTOR ELEMENT
1
19
42 OHM
SCOM
5
7
HR2 HYBRID
OVEN TEMP
(PG3C7)
-17S
HYBRID HEATER CONTROL CIRCUIT

CURRENT / HI RES 5700A-1021 2 OF 4 AUG.18.1988

Figure 7-7. A7 Current/High-Resolution Oscillator PCA (cont)

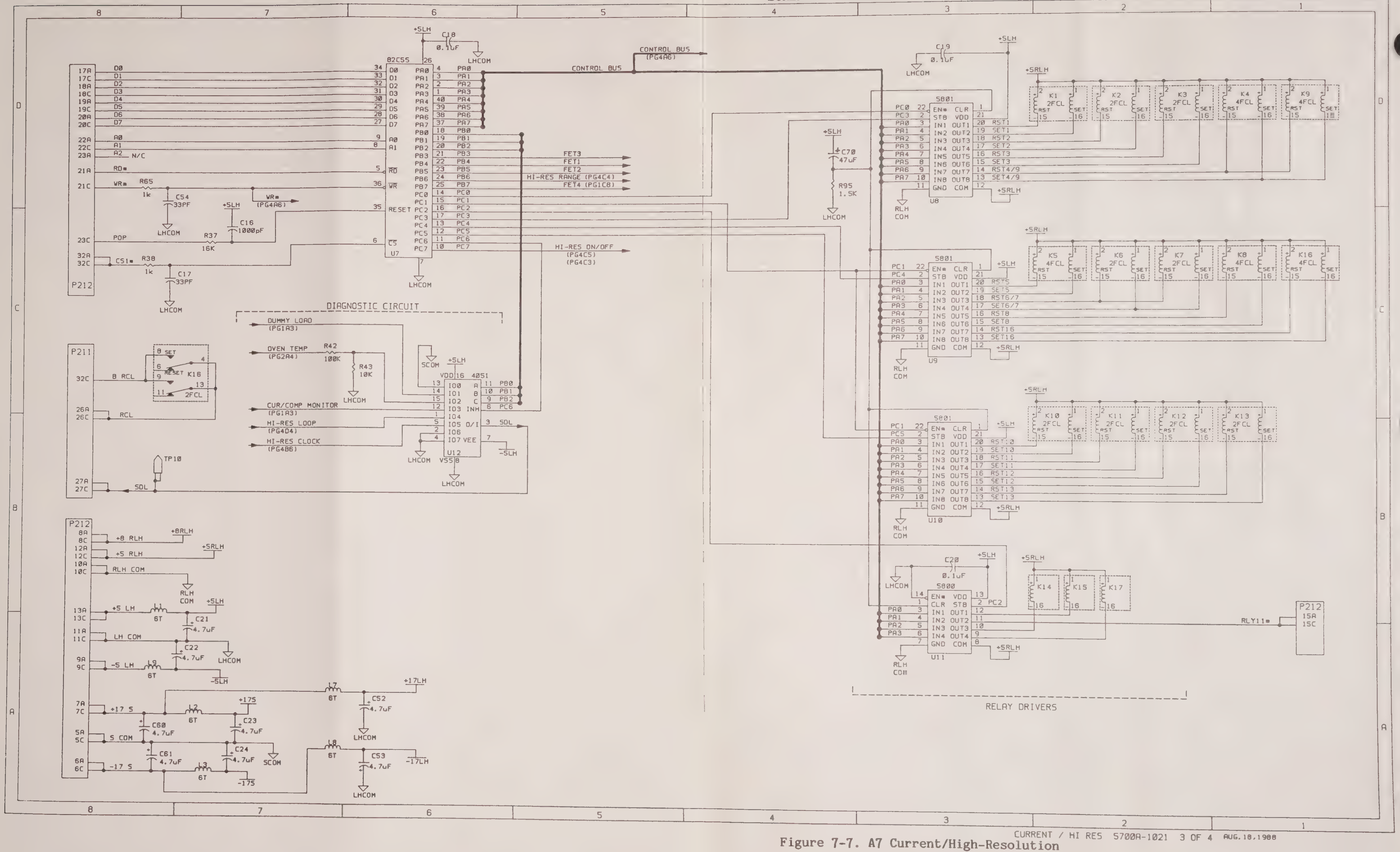
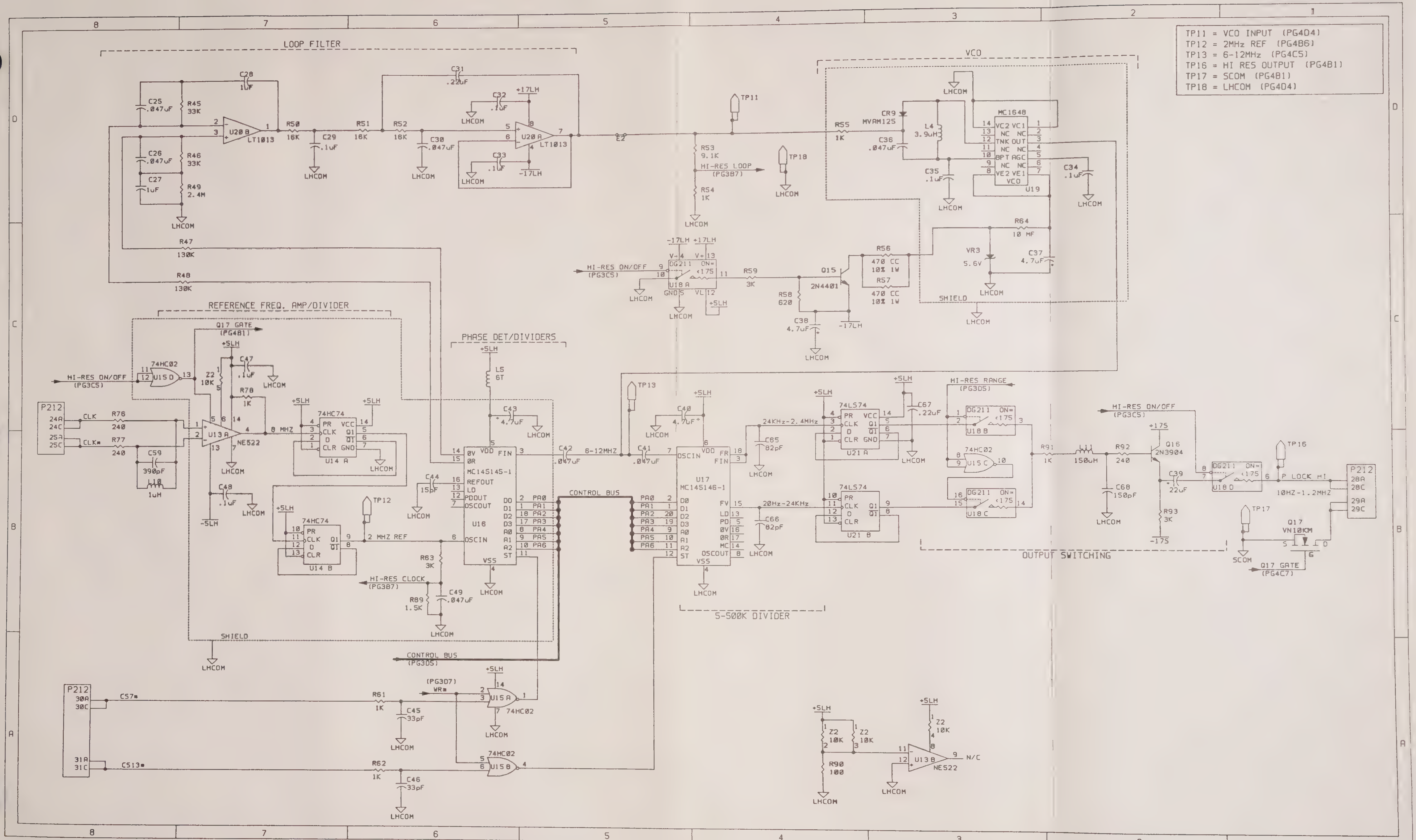

P212
17A
17C
18A
18C
19A
19C
20A
20C
22A
22C
23A
21A
21C
23C
32A
32C
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
N/C
RD*
WR*
R65
1k
C54
33PF
LHCOM
+5LH
C16
1000pF
R37
16K
POP
CS1*
R38
1k
C17
33PF
WR*
(PG4A6)
+5LH
C18
0.1uF
LHCOM
82C55
U7
RESET
CS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
CONTROL BUS
CONTROL BUS
(PG4A6)
FET3
FET1
FET2
HI-RES RANGE (PG4C4)
FET4 (PG1C8)
HI-RES ON/OFF
(PG4C5)
(PG4C3)
DIAGNOSTIC CIRCUIT
DUMMY LOAD
(PG1A3)
OVEN TEMP
(PG2A4)
R42
100K
R43
10K
LHCOM
SCOM
CUR/COMP MONITOR
(PG1A3)
HI-RES LOOP
(PG4D4)
HI-RES CLOCK
(PG4B6)
4051
U12
VDD
VEE
VSS
INH
O/I
SDL
-5LH
P211
32C
B RCL
SET
RESET
K18
2FCL
26A
26C
RCL
TP10
27A
27C
SDL
P212
8A
8C
+8 RLH
+8RLH
12A
12C
+5 RLH
+5RLH
10A
10C
RLH COM
RLH COM
13A
13C
+5 LH
L1
6T
C21
4.7uF
+5LH
11A
11C
LH COM
C22
4.7uF
LHCOM
9A
9C
-5 LH
L9
6T
-5LH
7A
7C
+17 S
L2
6T
+17S
C23
4.7uF
C60
4.7uF
5A
5C
S COM
C24
4.7uF
SCOM
C61
4.7uF
6A
6C
-17 S
L3
6T
-17S
L7
6T
C52
4.7uF
+17LH
LHCOM
L8
6T
C53
4.7uF
-17LH
LHCOM
+5LH
C19
0.1uF
LHCOM
+5LH
C70
47uF
R95
1.5K
LHCOM
5801
U8
EN* CLR
STB VDD
IN1 OUT1
IN2 OUT2
IN3 OUT3
IN4 OUT4
IN5 OUT5
IN6 OUT6
IN7 OUT7
IN8 OUT8
GND COM
RLH COM
+SRLH
RST1
SET1
RST2
SET2
RST3
SET3
RST4/9
SET4/9
K1 2FCL
K2 2FCL
K3 2FCL
K4 4FCL
K9 4FCL
RST
SET
5801
U9
+5LH
RST5
SET5
RST6/7
SET6/7
RST8
SET8
RST16
SET16
K5 4FCL
K6 2FCL
K7 2FCL
K8 4FCL
K16 4FCL
5801
U10
RST10
SET10
RST11
SET11
RST12
SET12
RST13
SET13
K10 2FCL
K11 2FCL
K12 2FCL
K13 2FCL
C20
0.1uF
+5LH
LHCOM
5800
U11
PC2
K14
K15
K17
RLY11*
P212
15A
15C
RELAY DRIVERS
CURRENT / HI RES 5700A-1021 3 OF 4 AUG.10,1988

Figure 7-7. A7 Current/High-Resolution Oscillator PCA (cont)


LOOP FILTER
C28 1uF
C25 .047uF
R45 33K
U20 B LT1013
R50 16K
C29 .1uF
R51 16K
R52 16K
C30 .047uF
C31 .22uF
C32 .1uF
+17LH
U20 A LT1013
C33 .1uF
-17LH
C26 .047uF
R46 33K
C27 1uF
R49 2.4M
LHCOM
R47 130K
R48 130K
TP11
E2
R53 9.1K
HI-RES LOOP (PG3B7)
R54 1K
TP18
VCO
CR9 MVAM125
R55 1K
C36 .047uF
L4 3.9uH
MC1648
VC2 VC1
NC NC
TNK OUT
BPT AGC
VE2 VE1
VCO
U19
C35 .1uF
C34 .1uF
R64 10 MF
VR3 5.6V
C37 4.7uF
R56 470 CC 10% 1W
R57 470 CC 10% 1W
SHIELD
-17LH +17LH
HI-RES ON/OFF (PG3C5)
DG211 ON= <175
U18 A
R59 3K
Q15 2N4401
R58 620
C38 4.7uF
REFERENCE FREQ. AMP/DIVIDER
Q17 GATE (PG4B1)
+5LH
C47 .1uF
Z2 10K
R70 1K
74HC02 U15 D
HI-RES ON/OFF (PG3C5)
P212 24A 24C 25A 25C
CLK
CLK*
R76 240
R77 240
C59 390pF
L10 1uH
U13 A NE522
8 MHZ
-5LH
C48 .1uF
74HC74 PR VCC CLK Q1 D Q1 CLR GND
U14 A
U14 B
TP12
2 MHZ REF
R63 3K
HI-RES CLOCK (PG3B7)
R89 1.5K
C49 .047uF
PHASE DET/DIVIDERS
L5 6T
C43 4.7uF
C44 15pF
MC145145-1
U16
FIN REFOUT LD PDOUT OSCOUT OSCIN
D0 D1 D2 D3 A0 A1 A2 ST
PA0 PA1 PA2 PA3 PA4 PA5 PA6
VSS
C42 .047uF
6-12MHZ
CONTROL BUS
CONTROL BUS (PG3D5)
TP13
C40 4.7uF
C41 .047uF
U17 MC145146-1
OSCIN FIN FR FV LD PD 0V 0R MC OSCOUT VSS
5-500K DIVIDER
24KHz-2.4MHz
C65 82pF
20Hz-24KHz
C66 82pF
74LS74
U21 A
U21 B
C67 .22uF
HI-RES RANGE (PG3D5)
DG211 ON= <175
U18 B
74HC02 U15 C
U18 C
HI-RES ON/OFF (PG3C5)
R91 1K
150uH
R92 240
C68 150pF
Q16 2N3904
+17S
C39 22uF
R93 3K
-17S
U18 D
TP16
P LOCK HI
10HZ-1.2MHZ
P212 28A 28C 29A 29C
TP17
Q17 VN10KM
SCOM
Q17 GATE (PG4C7)
OUTPUT SWITCHING
P212 30A 30C 31A 31C
CS7*
CS13*
R61 1K
R62 1K
C45 33pF
C46 33pF
(PG3D7) WR*
U15 A 74HC02
U15 B
Z2 10K
R90 100
U13 B NE522
N/C

TP11 = VCO INPUT (PG4D4)
TP12 = 2MHz REF (PG4B6)
TP13 = 6-12MHz (PG4C5)
TP16 = HI RES OUTPUT (PG4B1)
TP17 = SCOM (PG4B1)
TP18 = LHCOM (PG4D4)

CURRENT / HI RES 5700A-1021 4 OF 4 AUG.18,1988

Figure 7-7. A7 Current/High-Resolution Oscillator PCA (cont)

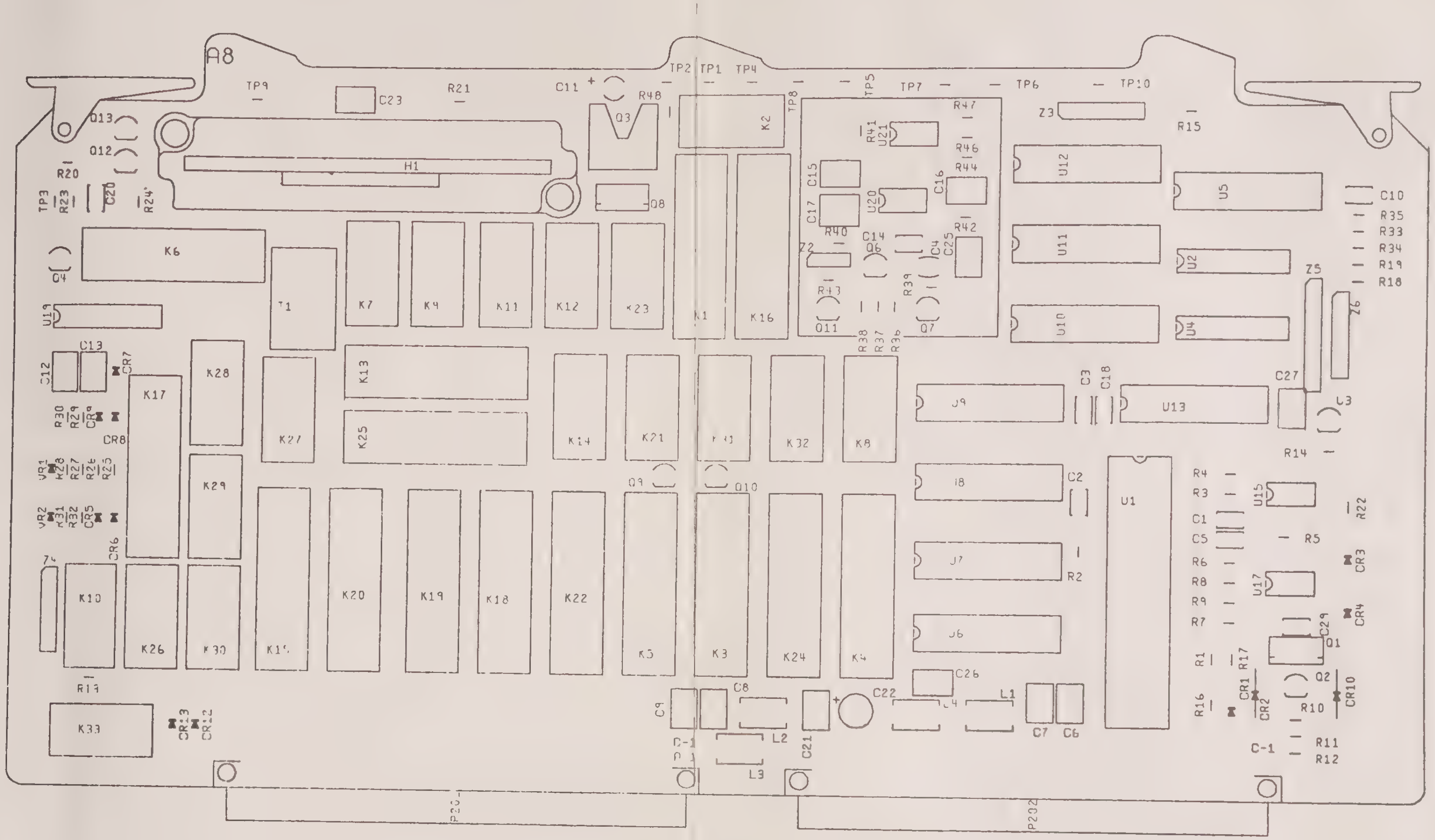
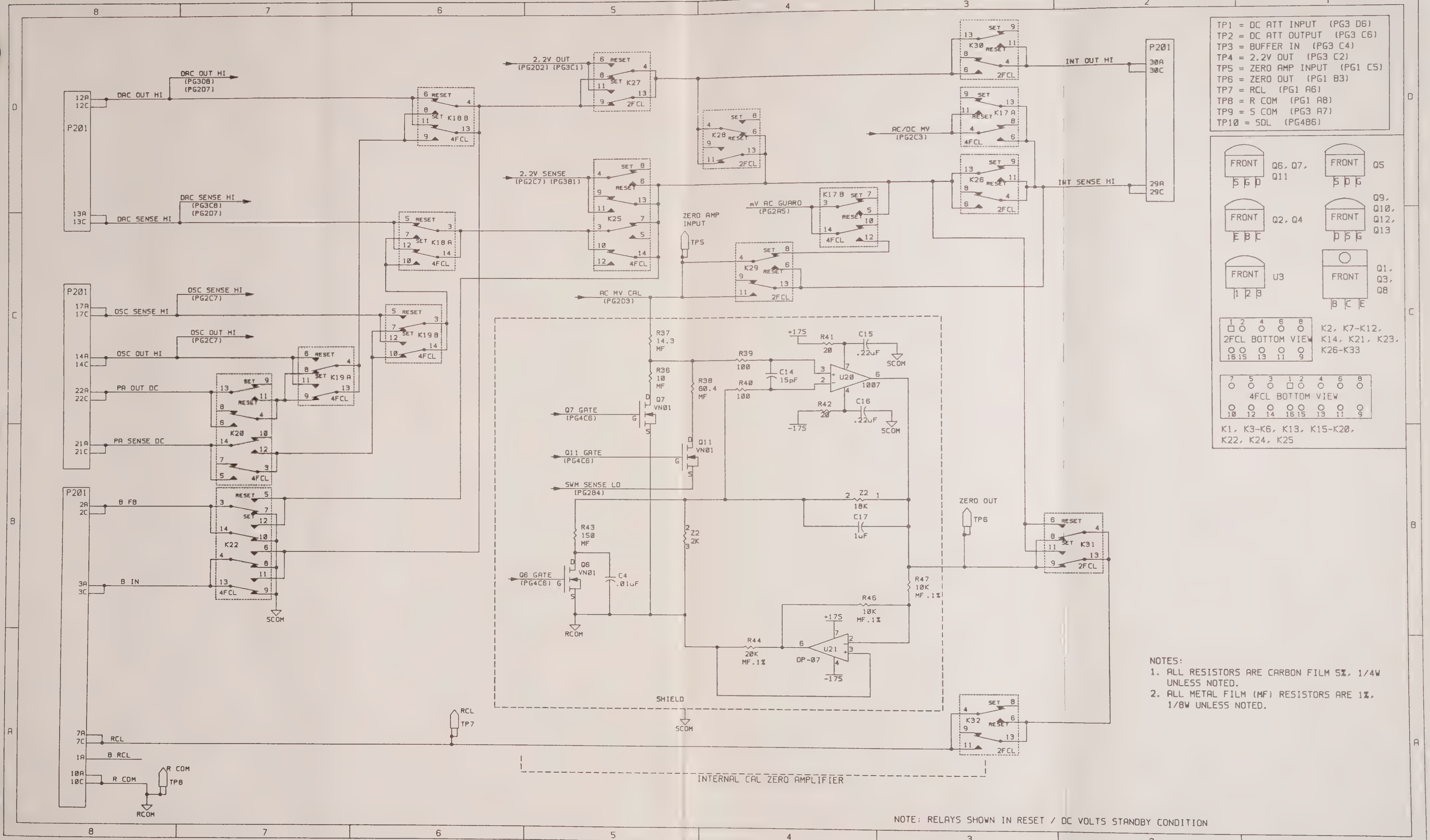

A8
TP9
C23
R21
C11
R48
TP2
TP1
TP4
TP8
TP5
TP7
TP6
TP10
Q13
Q12
R20
TP3
R23
C20
R24
H1
Q3
K2
R47
R41
U21
R46
R44
C15
C16
U20
C17
R40
C14
Q6
C4
C25
R42
Z2
R43
R39
Q11
Q7
R38
R37
R36
Z3
R15
U12
U5
C10
R35
R33
R34
R19
R18
U11
U2
Z5
Z6
U10
U4
Q8
K6
Q4
T1
K7
K9
K11
K12
K23
K1
K16
U19
C13
C12
CR7
K28
K17
K13
K25
K27
K14
K21
K31
K32
K8
U9
C3
C18
U13
C27
L3
R30
R29
CR9
CR8
R14
VR1
R28
R27
R26
R25
K29
Q9
Q10
U8
C2
U1
R4
R3
U15
R22
VR2
R31
R32
CR5
C1
C5
R5
CR6
Z4
U7
R2
R6
R8
U17
CR3
R9
R7
C29
CR4
Q1
K10
K26
K30
K15
K20
K19
K18
K22
K5
K3
K24
K4
U6
C26
R1
R17
R13
K33
CR13
CR12
C9
C8
C22
C24
L1
C7
C6
CR1
Q2
CR10
R16
CR2
R10
C-1
R11
R12
L2
C21
L3
P201
P202

Figure 7-8. A8 Switch Matrix PCA


P201
12A
12C
DAC OUT HI
DAC OUT HI (PG3D8) (PG2D7)
13A
13C
DAC SENSE HI
DAC SENSE HI (PG3C8) (PG2D7)
17A
17C
OSC SENSE HI
OSC SENSE HI (PG2C7)
14A
14C
OSC OUT HI
OSC OUT HI (PG2C7)
22A
22C
PA OUT DC
21A
21C
PA SENSE DC
2A
2C
B FB
3A
3C
B IN
7A
7C
RCL
1A
B RCL
10A
10C
R COM
RCL
TP7
R COM
TP8
RCOM
SCOM
K18 B
K18 A
K19 B
K19 A
K20
K22
K27
K25
K28
K29
K17 B
K30
K17 A
K26
K31
K32
SET
RESET
4FCL
2FCL
2.2V OUT (PG2D2) (PG3C1)
2.2V SENSE (PG2C7) (PG3B1)
ZERO AMP INPUT
TP5
AC MV CAL (PG2D3)
mV AC GUARD (PG2A5)
AC/DC MV (PG2C3)
INT OUT HI
INT SENSE HI
30A
30C
29A
29C
R37 14.3 MF
R36 10 MF
R38 60.4 MF
Q7 VN01
Q11 VN01
Q7 GATE (PG4C6)
Q11 GATE (PG4C6)
SWM SENSE LO (PG2B4)
R39 100
R40 100
C14 15pF
+17S
R41 20
C15 .22uF
U20 1007
R42 20
C16 .22uF
-17S
2 Z2 1 10K
C17 1uF
Z2 2K
R43 150 MF
Q6 VN01
Q6 GATE (PG4C6)
C4 .01uF
RCOM
R47 10K MF .1%
R46 10K MF .1%
R44 20K MF.1%
U21 OP-07
ZERO OUT
TP6
SHIELD
INTERNAL CAL ZERO AMPLIFIER
FRONT
Q6, Q7, Q11
S G D
Q5
S D G
Q2, Q4
E B C
Q9, Q10, Q12, Q13
D S G
U3
1 2 3
Q1, Q3, Q8
B C E
2FCL BOTTOM VIEW
K2, K7-K12, K14, K21, K23, K26-K33
4FCL BOTTOM VIEW
K1, K3-K6, K13, K15-K20, K22, K24, K25

TP1 = DC ATT INPUT (PG3 D6)
TP2 = DC ATT OUTPUT (PG3 C6)
TP3 = BUFFER IN (PG3 C4)
TP4 = 2.2V OUT (PG3 C2)
TP5 = ZERO AMP INPUT (PG1 C5)
TP6 = ZERO OUT (PG1 B3)
TP7 = RCL (PG1 A6)
TP8 = R COM (PG1 A8)
TP9 = S COM (PG3 A7)
TP10 = SDL (PG4B6)

NOTES:

1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

NOTE: RELAYS SHOWN IN RESET / DC VOLTS STANDBY CONDITION

SWITCH MATRIX 5700A-1020 1 OF 5 AUG.18,1988

Figure 7-8. A8 Switch Matrix PCA (cont)

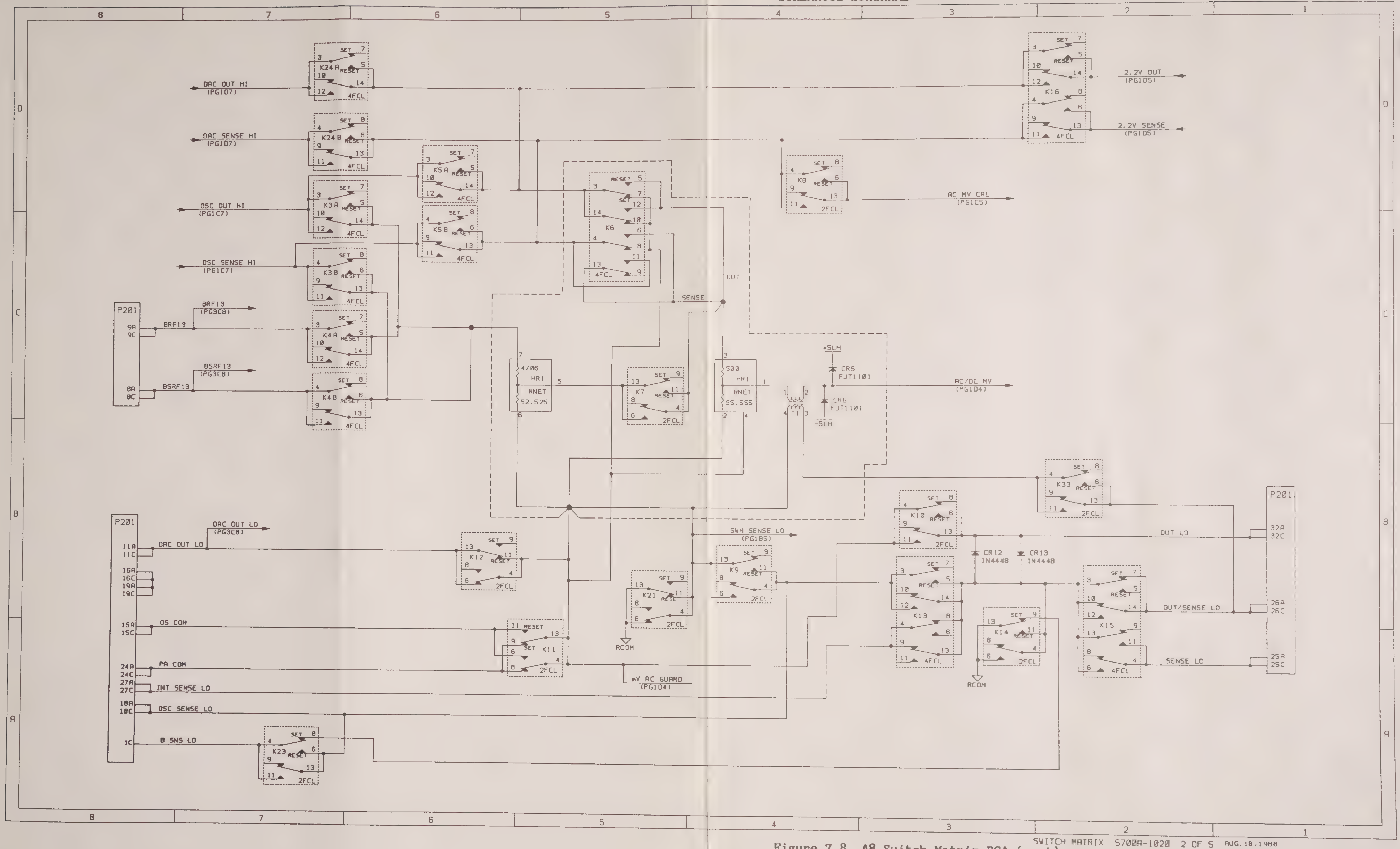
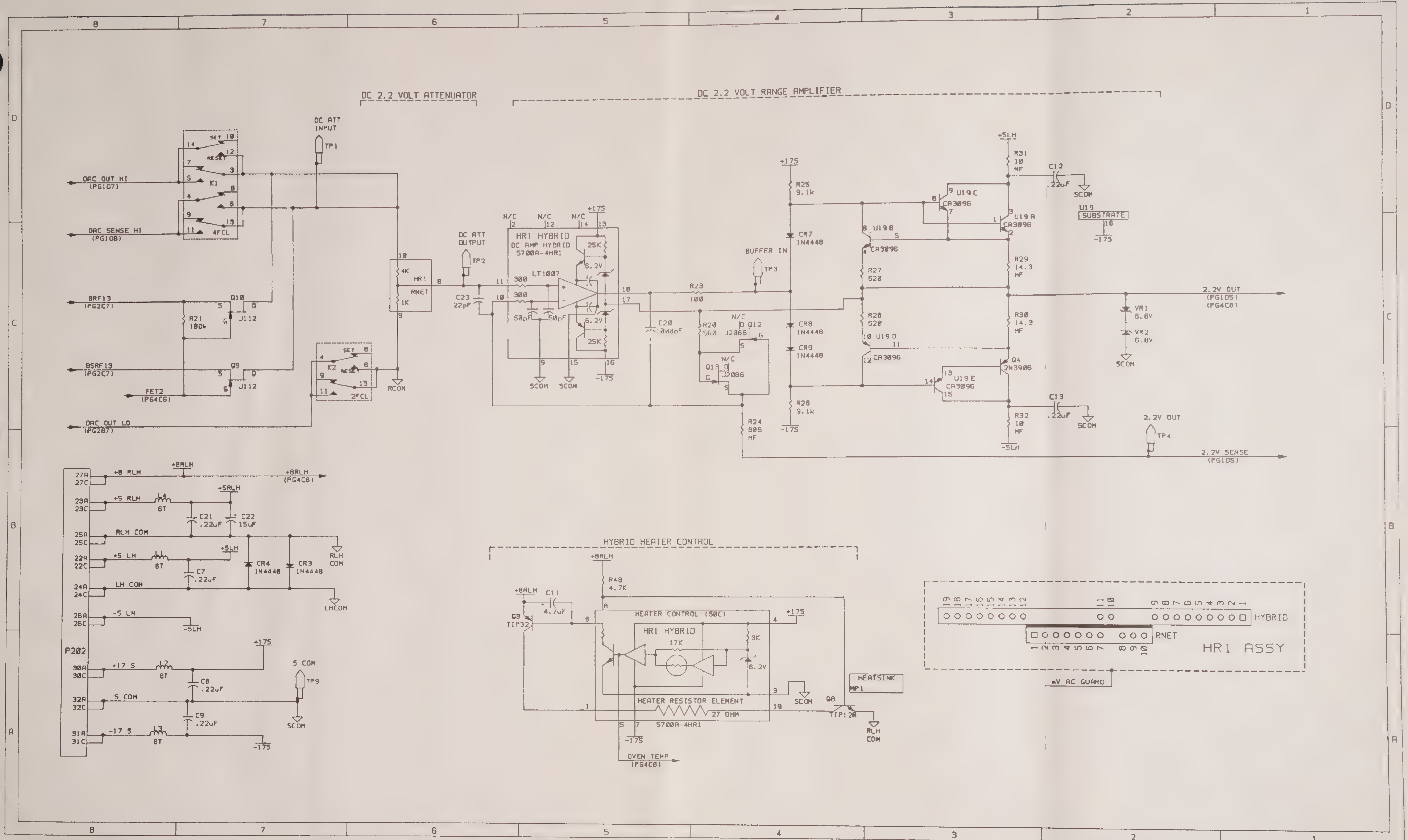
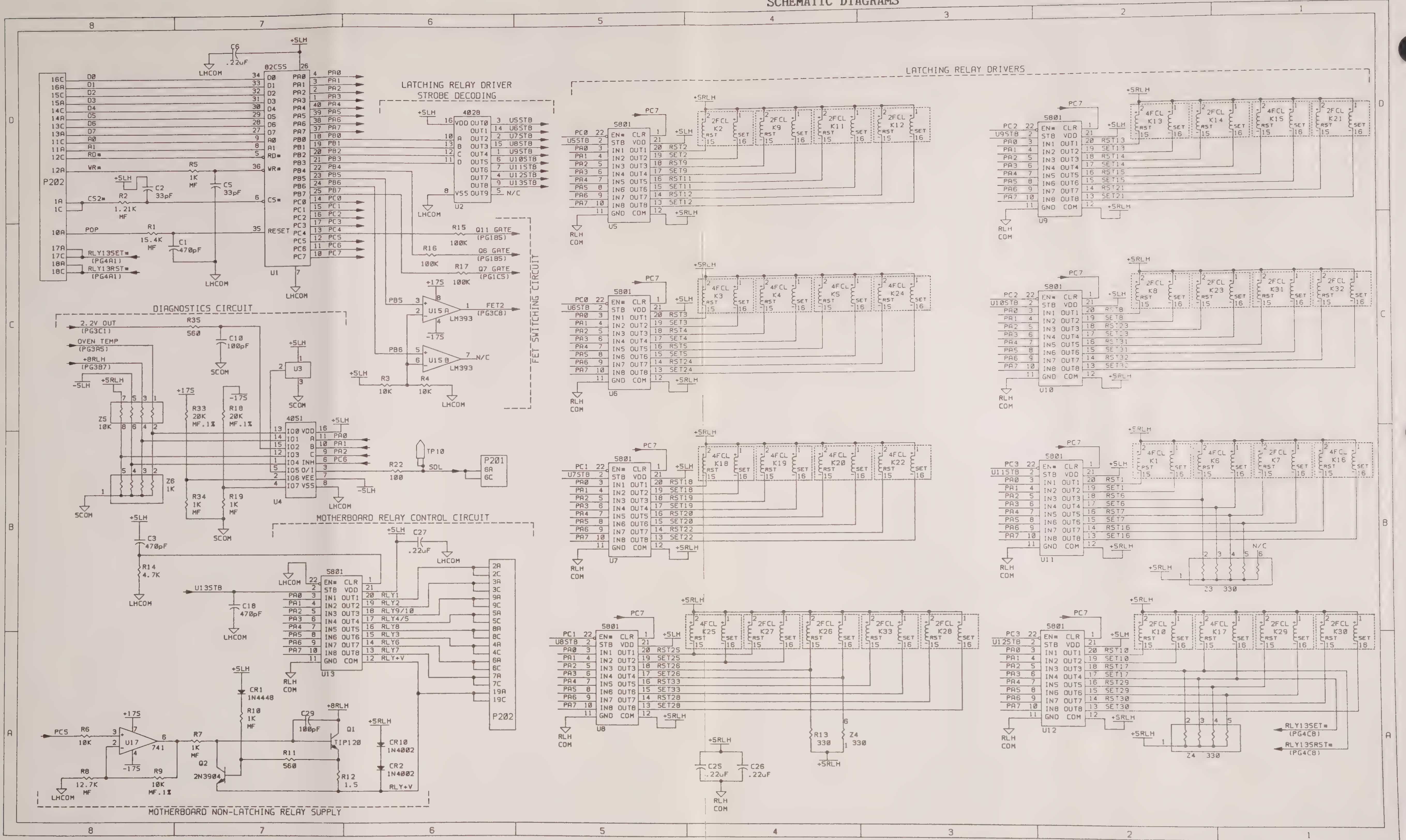

DAC OUT HI (PG1D7)
DAC SENSE HI (PG1D7)
OSC OUT HI (PG1C7)
OSC SENSE HI (PG1C7)
BRF13 (PG3C8)
BSRF13 (PG3C8)
P201
9A
9C
8A
8C
BRF13
BSRF13
K24A
K24B
K3A
K3B
K4A
K4B
K5A
K5B
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K21
K23
K33
SET
RESET
4FCL
2FCL
4706 HR1 RNET 52.525
500 HR1 RNET 55.555
T1
OUT
SENSE
+SLH
-SLH
CR5 FJT1101
CR6 FJT1101
CR12 1N4448
CR13 1N4448
2.2V OUT (PG1D5)
2.2V SENSE (PG1D5)
AC MV CAL (PG1C5)
AC/DC MV (PG1D4)
DAC OUT LO (PG3C8)
DAC OUT LO
11A
11C
16A
16C
19A
19C
15A
15C
OS COM
24A
24C
27A
27C
PA COM
INT SENSE LO
18A
18C
OSC SENSE LO
1C
B SNS LO
SWM SENSE LO (PG1B5)
mV AC GUARD (PG1D4)
RCOM
OUT LO
OUT/SENSE LO
SENSE LO
32A
32C
26A
26C
25A
25C
8
7
6
5
4
3
2
1
D
C
B
A
SWITCH MATRIX 5700A-1020 2 OF 5 AUG.18.1988

Figure 7-8. A8 Switch Matrix PCA (cont)


DC 2.2 VOLT ATTENUATOR
DC 2.2 VOLT RANGE AMPLIFIER
HYBRID HEATER CONTROL
DAC OUT HI (PG1D7)
DAC SENSE HI (PG1D8)
BRF13 (PG2C7)
BSRF13 (PG2C7)
FET2 (PG4C6)
DAC OUT LO (PG2B7)
K1 4FCL
K2 2FCL
SET
RESET
Q10 J112
Q9 J112
R21 100k
DC ATT INPUT
TP1
DC ATT OUTPUT
TP2
HR1 RNET 4K 1K
RCOM
C23 22pF
HR1 HYBRID DC AMP HYBRID 5700A-4HR1
LT1007
N/C
+175
-175
300
50pF
6.2V
25K
SCOM
C20 1000pF
R23 100
BUFFER IN
TP3
R20 560
Q12 J2086
Q13 J2086
R24 806 MF
R25 9.1k
CR7 1N4448
CR8 1N4448
CR9 1N4448
R26 9.1k
R27 620
R28 620
U19 B CA3096
U19 C CA3096
U19 A CA3096
U19 D CA3096
U19 E CA3096
Q4 2N3906
+5LH
-5LH
R31 10 MF
R29 14.3 MF
R30 14.3 MF
R32 10 MF
C12 .22uF
C13 .22uF
U19 SUBSTRATE
VR1 6.8V
VR2 6.8V
2.2V OUT (PG1D5) (PG4C8)
2.2V OUT
TP4
2.2V SENSE (PG1D5)
P202
27A 27C +8 RLH
+8RLH (PG4C8)
23A 23C +5 RLH
+5RLH
L4 6T
C21 .22uF
C22 15uF
25A 25C RLH COM
22A 22C +5 LH
+5LH
C7 .22uF
CR4 1N4448
CR3 1N4448
RLH COM
24A 24C LH COM
LHCOM
26A 26C -5 LH
-5LH
30A 30C +17 S
L2 6T
C8 .22uF
32A 32C S COM
S COM
TP9
C9 .22uF
31A 31C -17 S
L3 6T
-17S
+17S
+8RLH
R48 4.7K
C11 4.7uF
Q3 TIP32
HEATER CONTROL (50C)
HR1 HYBRID
17K
3K
6.2V
HEATER RESISTOR ELEMENT
27 OHM
5700A-4HR1
OVEN TEMP (PG4C8)
Q8 TIP120
HEATSINK MP1
RLH COM
HYBRID
RNET
HR1 ASSY
mV AC GUARD
8 7 6 5 4 3 2 1
D C B A

SWITCH MATRIX 5700A-1020 3 OF 5 AUG.18,1988

Figure 7-8. A8 Switch Matrix PCA (cont)


LATCHING RELAY DRIVER STROBE DECODING
LATCHING RELAY DRIVERS
DIAGNOSTICS CIRCUIT
FET SWITCHING CIRCUIT
MOTHERBOARD RELAY CONTROL CIRCUIT
MOTHERBOARD NON-LATCHING RELAY SUPPLY
P202
P201
82C55
U1
4028
U2
4051
U4
5801
U5
U6
U7
U8
U9
U10
U11
U12
U13
U15A
U15B
LM393
U17
741
Q1
TIP120
Q2
2N3904
CR1
1N4448
CR10
1N4002
CR2
1N4002
Z3 330
Z4 330
Z5 10K
Z6 1K
TP10
+SLH
+SRLH
+SRLH
LHCOM
RLH COM
SCOM
RLY13SET=
(PG4A1)
RLY13RST=
(PG4A1)
Q11 GATE (PG1B5)
Q6 GATE (PG1B5)
Q7 GATE (PG1C5)
FET2 (PG3C8)
2.2V OUT (PG3C1)
OVEN TEMP (PG3A5)
+8RLH (PG3B7)
RLY13SET= (PG4C8)
RLY13RST= (PG4C8)
RLY+V
U13STB
PCS

SWITCH MATRIX 5700A-1020 4 OF 5 AUG.18,1988

Figure 7-8. A8 Switch Matrix PCA (cont)

	SWITCH MATRIX RELAYS AND FETS																																				MOTHERBOARD RELAYS								
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	Q6	Q7	Q9/Q10	Q11	K1	K2	K3	K4/K5	K6	K7	K8	K9/K10	K13
RESET / DC VOLTS STANDBY												R						R			R							R								✱											
DC 220mV RANGE	R	R				R										R	R				R												R						■			■	■	■		R
DC 2.2V RANGE	R	R								R				R	E										R	R	R			R					✱			■	■	E		■	■	■		
DC 11V/22V RANGE										R		R		R	E			R								R				R					✱			■	■	E		■	■	■		
DC 220V RANGE										R		R		R	E					R						R				R					✱			■	■	E		■	■	■		
DC 1100V RANGE										R		R		R	E																				✱					E		■	■	■	■	
DC 1100V 5205 MODE													R						R				R	R											✱											
AC VOLTS STANDBY									R		R								R									R							✱											
AC 2.2mV RANGE			R				R		R		R				R		R																R						■			■	■	■		R
AC 22mV RANGE			R				R		R		R				R		R																R						■			■	■	■		R
AC 220mV RANGE					R	R			R		R				R		R																R						■			■	■	■		R
AC 2.2V/22V RANGE										R	R		R		E				R							R				R					✱			■	■	E		■	■	■		
AC 220V RANGE										R			R		E																				✱					E		■	■	■	■	
AC 1100V RANGE										R			R		E																				✱					E		■	■	■	■	
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	Q6	Q7	Q9/Q10	Q11	K1	K2	K3	K4/K5	K6	K7	K8	K9/K10	
AC 1100V BOOST MODE										R			R						R			R													✱						■					
AC 1100V 5205 MODE												R		R				R				R	R		R		R								✱											
BOOST DC CURRENT MODE	R	R										R										R			R		R	R							✱											
BOOST AC CURRENT MODE									R										R			R	R												✱											
DC 11V RANGE ZERO CAL												R						R			R					R		R	R			R		✱												
CAL 10V DC TO EXT 10V STD										R		R		R												R					R	R			✱				■							
2.2V RANGE OFFSET CAL	R	R										R													R	R	R	R	R			R		✱												
2.2V RANGE GAIN CAL		R										R													R		R	R	R		R	R			✱	✱										
220mV RANGE CHECKPOINT	R	R				R										R					R											R		✱			✱									R
220mV RANGE OFFSET CAL	R	R				R										R	R				R								R			R		✱												R
220mV RANGE GAIN CAL						R						R					R				R			R					R			R														R
22mV RANGE GAIN CAL				R		R	R	R				R						R			R							R				R													
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	Q6	Q7	Q9/Q10	Q11	K1	K2	K3	K4/K5	K6	K7	K8	K9/K10	

R = RESET POSITION FOR ALL LATCHING RELAYS

■ = ENERGIZED FOR NON-LATCHING RELAYS

✱ = ON FOR FETS

E = EXTERNAL SENSE STATE FOR K15 RESET AND MOTHERBOARD RELAY K3 ENERGIZED

THE SCHEMATIC IS SHOWN WITH THE RELAYS IN THE RESET / DC VOLTS STANDBY CONDITION

SWITCH MATRIX 5700A-1020 5 OF 5 AUG.18,1988

Figure 7-8. A8 Switch Matrix PCA (cont)

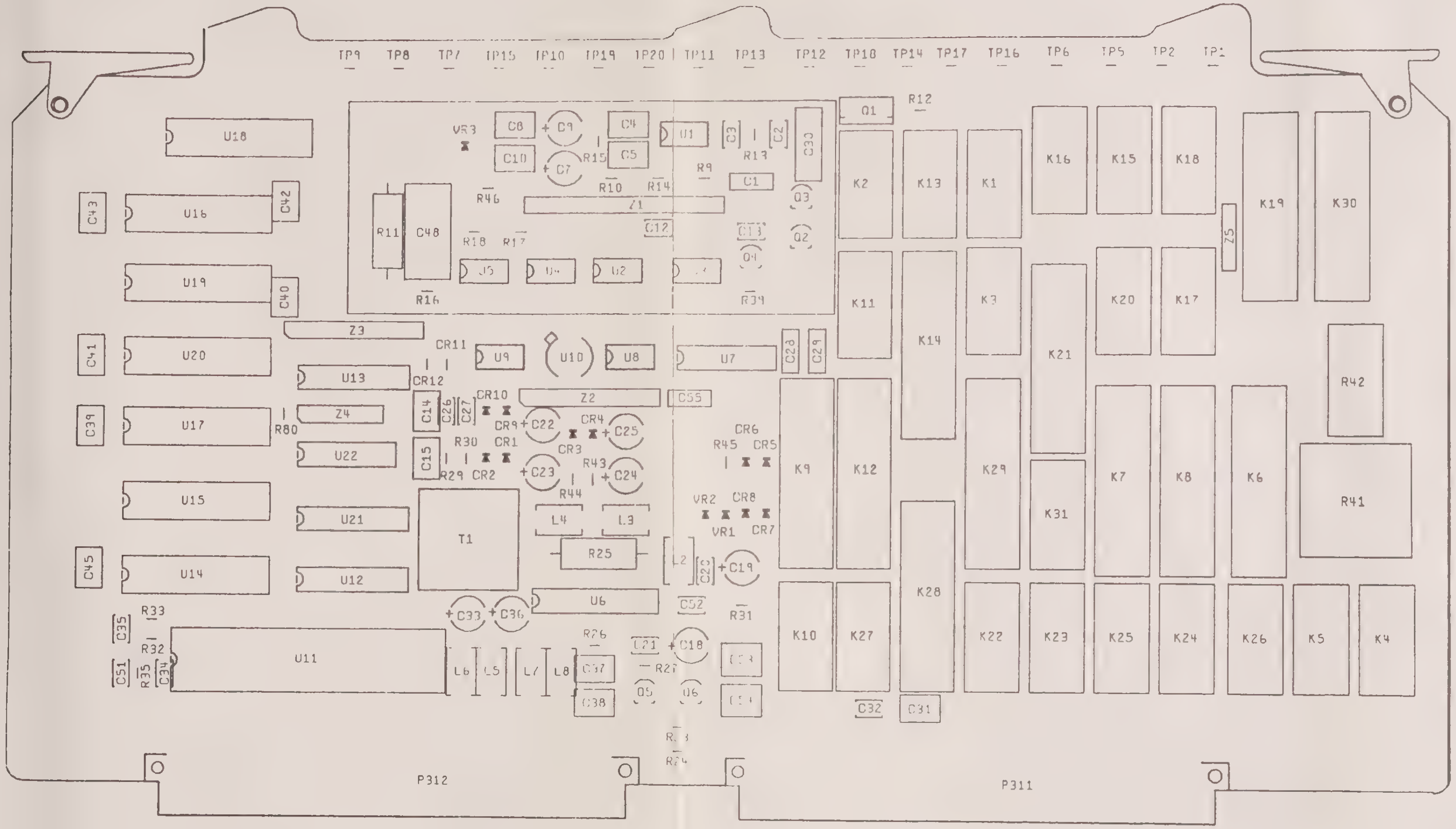
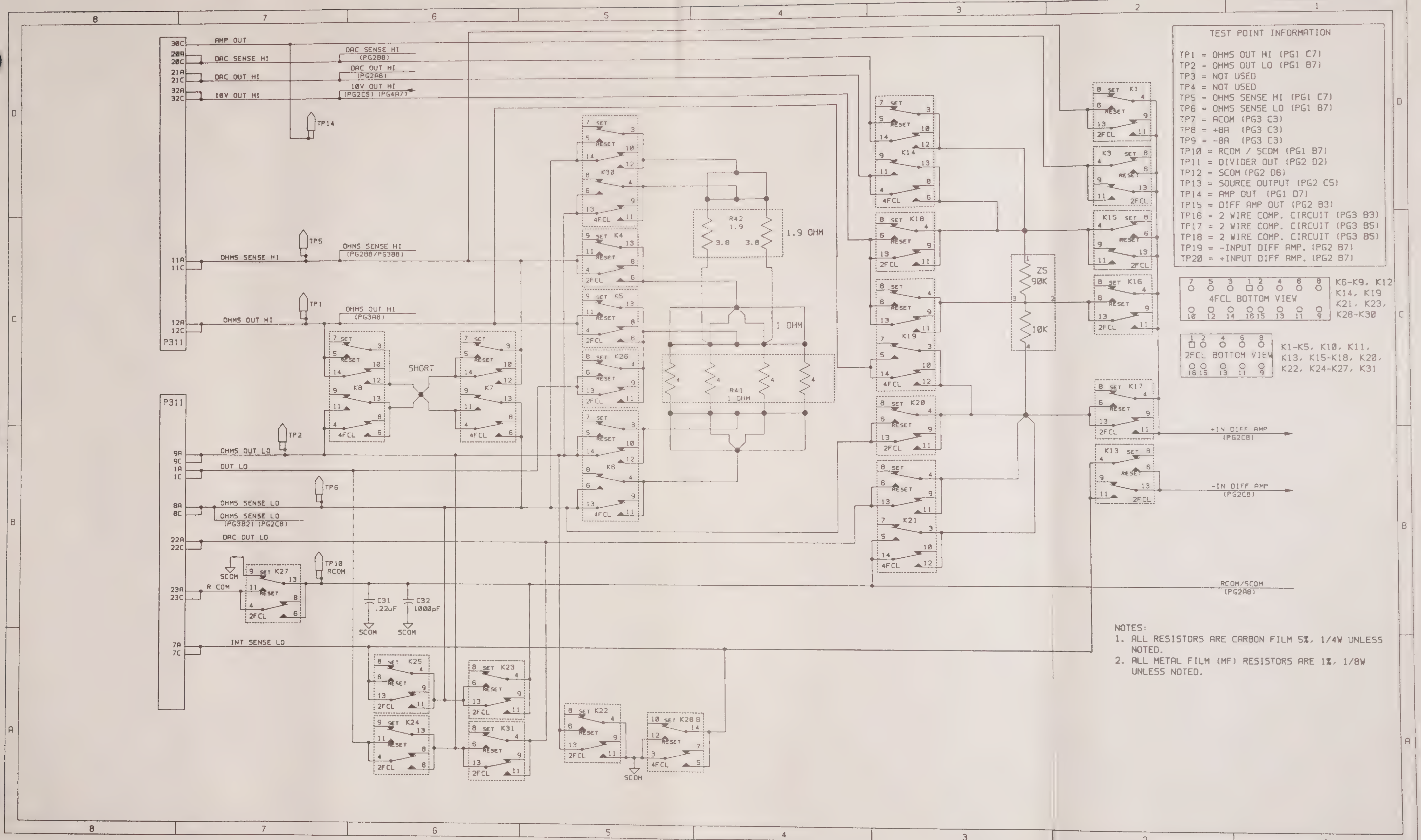

TP9
TP8
TP7
TP15
TP10
TP19
TP20
TP11
TP13
TP12
TP18
TP14
TP17
TP16
TP6
TP5
TP2
TP1
U18
VR3
C8
C9
C4
U1
C3
C2
C30
Q1
R12
C10
C7
R15
C5
R13
R9
C1
K16
K15
K18
K2
K13
K1
R46
R10
R14
Z1
Q3
C43
U16
C42
R11
C48
C12
C13
Q2
Z5
K19
K30
R18
R17
U5
U4
U2
U3
Q4
U19
C40
R16
R34
K11
K3
K20
K17
K21
K14
Z3
CR11
C41
U20
U9
U10
U8
U7
C28
C29
R42
U13
CR12
Z2
C55
C14
C26
C27
CR10
C39
U17
Z4
CR9
C22
CR4
C25
CR6
R80
R30
CR1
CR3
R45
CR5
K9
K12
K29
K7
K8
K6
U22
C15
R43
R29
CR2
C23
C24
R44
VR2
CR8
K31
R41
U15
U21
T1
L4
L3
VR1
CR7
R25
L2
C22
C19
K28
C45
U14
U12
U6
C52
C33
C36
R33
R31
C35
R32
R26
C21
C18
C20
K10
K27
K22
K23
K25
K24
K26
K5
K4
U11
L6
L5
L7
L8
C37
R27
C51
R35
C34
Q5
Q6
C38
C16
C32
C31
R23
R24
P312
P311

Figure 7-9. A9 Ohms Cal PCA


P311
30C AMP OUT
20A 20C DAC SENSE HI
21A 21C DAC OUT HI
32A 32C 10V OUT HI
DAC SENSE HI (PG2B8)
DAC OUT HI (PG2A8)
10V OUT HI (PG2C5) (PG4A7)
TP14
TP5
11A 11C OHMS SENSE HI
OHMS SENSE HI (PG2B8/PG3B8)
TP1
12A 12C OHMS OUT HI
OHMS OUT HI (PG3A8)
K8
SHORT
K7
K30
K4
K5
K26
K6
R42 1.9
3.8
3.8
1.9 OHM
1 OHM
R41 1 OHM
K14
K18
K19
K20
K21
Z5 90K
10K
K1
K3
K15
K16
K17
K13
+IN DIFF AMP (PG2C8)
-IN DIFF AMP (PG2C8)
TP2
9A 9C OHMS OUT LO
1A 1C OUT LO
TP6
8A 8C OHMS SENSE LO
OHMS SENSE LO (PG3B2) (PG2C8)
22A 22C DAC OUT LO
SCOM
K27
TP10 RCOM
23A 23C R COM
C31 .22uF
C32 1000pF
SCOM
SCOM
RCOM/SCOM (PG2A8)
7A 7C INT SENSE LO
K25
K23
K24
K31
K22
K28 B
SCOM
SET
RESET
2FCL
4FCL
7 5 3 1 2 4 6 8
4FCL BOTTOM VIEW
10 12 14 16 15 13 11 9
K6-K9, K12
K14, K19
K21, K23,
K28-K30
1 2 4 6 8
2FCL BOTTOM VIEW
16 15 13 11 9
K1-K5, K10, K11,
K13, K15-K18, K20,
K22, K24-K27, K31
8
7
6
5
4
3
2
1
D
C
B
A

TEST POINT INFORMATION

TP1 = OHMS OUT HI (PG1 C7)
TP2 = OHMS OUT LO (PG1 B7)
TP3 = NOT USED
TP4 = NOT USED
TP5 = OHMS SENSE HI (PG1 C7)
TP6 = OHMS SENSE LO (PG1 B7)
TP7 = ACOM (PG3 C3)
TP8 = +8A (PG3 C3)
TP9 = -8A (PG3 C3)
TP10 = RCOM / SCOM (PG1 B7)
TP11 = DIVIDER OUT (PG2 D2)
TP12 = SCOM (PG2 D6)
TP13 = SOURCE OUTPUT (PG2 C5)
TP14 = AMP OUT (PG1 D7)
TP15 = DIFF AMP OUT (PG2 B3)
TP16 = 2 WIRE COMP. CIRCUIT (PG3 B3)
TP17 = 2 WIRE COMP. CIRCUIT (PG3 B5)
TP18 = 2 WIRE COMP. CIRCUIT (PG3 B5)
TP19 = -INPUT DIFF AMP. (PG2 B7)
TP20 = +INPUT DIFF AMP. (PG2 B7)

NOTES:

1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

OHMS CAL. 5700A-1031 1 OF 4 AUG.17,1988

Figure 7-9. A9 Ohms Cal PCA (cont)

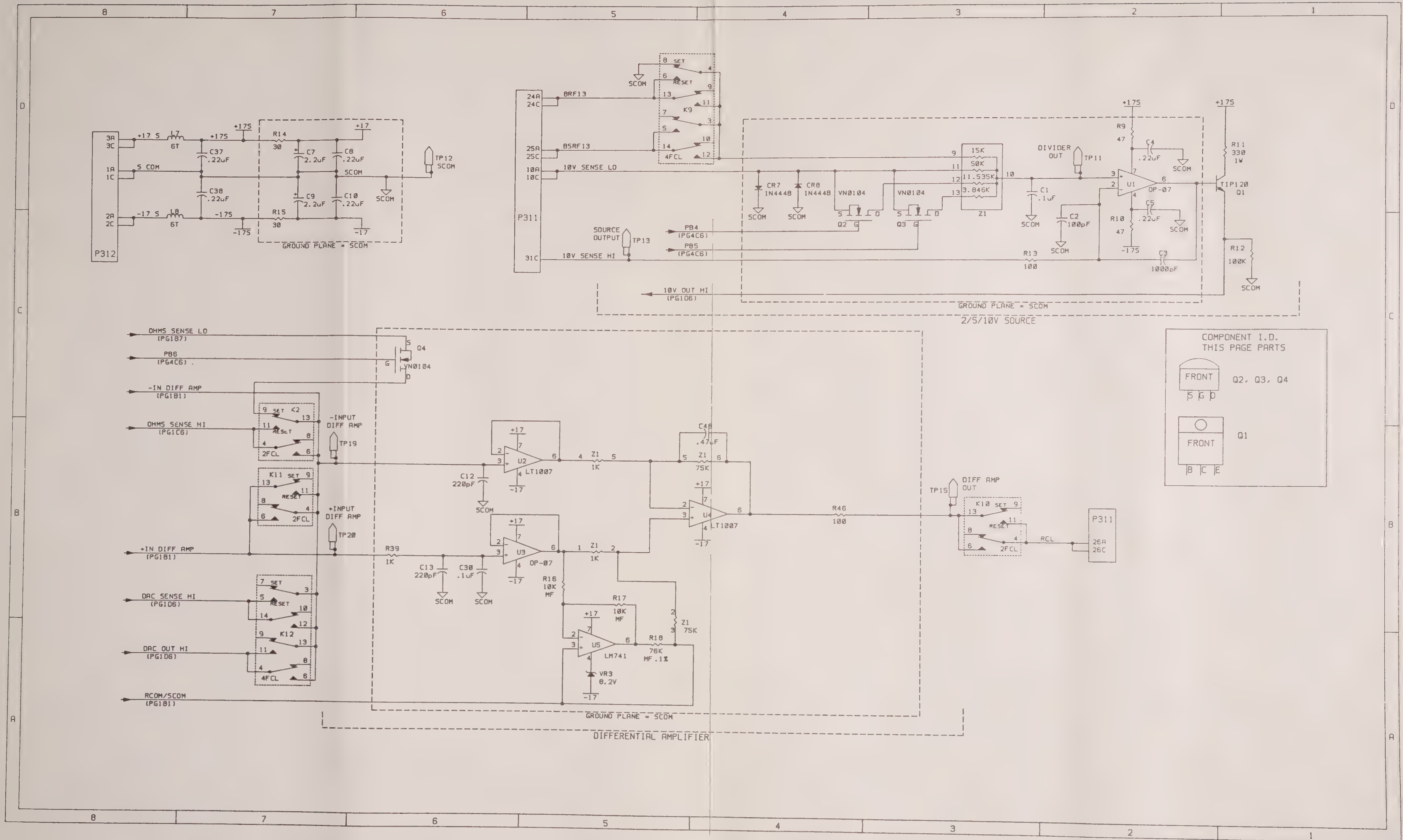

P312
3A
3C
+17 S
L7
6T
+175
+175
1A
1C
S COM
C37
.22uF
C38
.22uF
2A
2C
-17 S
L8
6T
-175
-175
R14
30
R15
30
C7
2.2uF
C8
.22uF
C9
2.2uF
C10
.22uF
+17
SCOM
SCOM
-17
GROUND PLANE = SCOM
TP12
SCOM
P311
24A
24C
BRF13
25A
25C
BSRF13
10A
10C
10V SENSE LO
31C
10V SENSE HI
K9
SET
RESET
4FCL
SCOM
SOURCE
OUTPUT
TP13
PB4
(PG4C6)
PB5
(PG4C6)
CR7
1N4448
CR8
1N4448
VN0104
VN0104
Q2
Q3
15K
50K
11.535K
3.846K
Z1
C1
.1uF
C2
100pF
DIVIDER
OUT
TP11
R9
47
C4
.22uF
U1
OP-07
R10
47
C5
.22uF
-175
C3
1000pF
R13
100
R11
330
1W
TIP120
Q1
R12
100K
10V OUT HI
(PG1D6)
GROUND PLANE = SCOM
2/5/10V SOURCE
OHMS SENSE LO
(PG1B7)
PB6
(PG4C6)
Q4
VN0104
-IN DIFF AMP
(PG1B1)
OHMS SENSE HI
(PG1C6)
K2
2FCL
-INPUT
DIFF AMP
TP19
K11
2FCL
+INPUT
DIFF AMP
TP20
+IN DIFF AMP
(PG1B1)
R39
1K
DAC SENSE HI
(PG1D6)
K12
4FCL
DAC OUT HI
(PG1D6)
RCOM/SCOM
(PG1B1)
U2
LT1007
C12
220pF
U3
OP-07
C13
220pF
C30
.1uF
Z1
1K
Z1
1K
C48
.47uF
Z1
75K
U4
LT1007
R16
10K
MF
R17
10K
MF
U5
LM741
VR3
8.2V
R18
76K
MF.1%
Z1
75K
GROUND PLANE = SCOM
DIFFERENTIAL AMPLIFIER
R46
100
TP15
DIFF AMP
OUT
K10
2FCL
RCL
P311
26A
26C
COMPONENT I.D.
THIS PAGE PARTS
FRONT
S G D
Q2, Q3, Q4
FRONT
B C E
Q1
8
7
6
5
4
3
2
1
D
C
B
A

Figure 7-9. A9 Ohms Cal PCA (cont)

OHMS CAL. 5700A-1031 2 OF 4 AUG.17.1988

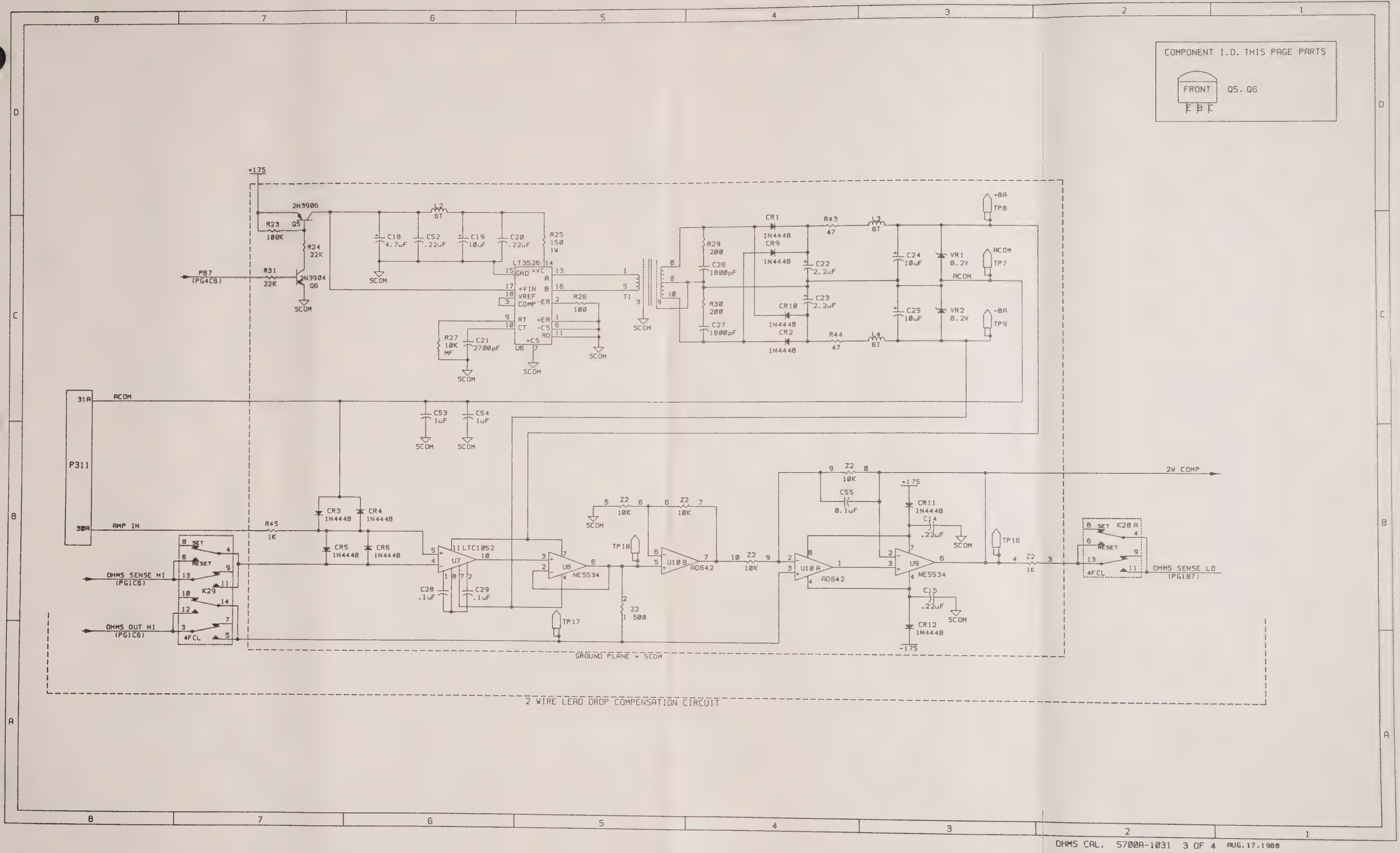

COMPONENT I.D. THIS PAGE PARTS
FRONT
Q5, Q6
E B C
+17S
2N3906
R23 100K
Q5
R24 22K
R31 22K
P87 (PG4C6)
2N3904 Q6
SCOM
L2 6T
C18 4.7uF
C52 .22uF
C19 10uF
C20 .22uF
R25 150 1W
LT3526
GND +VC
+VIN
VREF
COMP
RT
CT
-ER
+ER
-CS
RD
+CS
U6
R26 100
R27 10K MF
C21 2700pF
T1
CR1 1N4448
CR9 1N4448
CR10 1N4448
CR2 1N4448
R29 200
R30 200
C26 1800pF
C27 1800pF
C22 2.2uF
C23 2.2uF
R43 47
R44 47
L3 6T
L4 6T
C24 10uF
C25 10uF
VR1 8.2V
VR2 8.2V
+8A TP8
ACOM TP7
ACOM
-8A TP9
P311
31A ACOM
30A AMP IN
C53 1uF
C54 1uF
R45 1K
CR3 1N4448
CR4 1N4448
CR5 1N4448
CR6 1N4448
SET
RESET
K29
4FCL
OHMS SENSE HI (PG1C6)
OHMS OUT HI (PG1C6)
LTC1052 U7
C28 .1uF
C29 .1uF
U8 NE5534
TP17
TP18
Z2 10K
Z2 500
U10 B AD642
U10 A AD642
C55 0.1uF
+17S
CR11 1N4448
C14 .22uF
C15 .22uF
CR12 1N4448
-17S
U9 NE5534
TP16
Z2 1K
2W COMP
K28 A
OHMS SENSE LO (PG1B7)
GROUND PLANE = SCOM
2 WIRE LEAD DROP COMPENSATION CIRCUIT
OHMS CAL. 5700A-1031 3 OF 4 AUG.17,1988

Figure 7-9. A9 Ohms Cal PCA (cont)

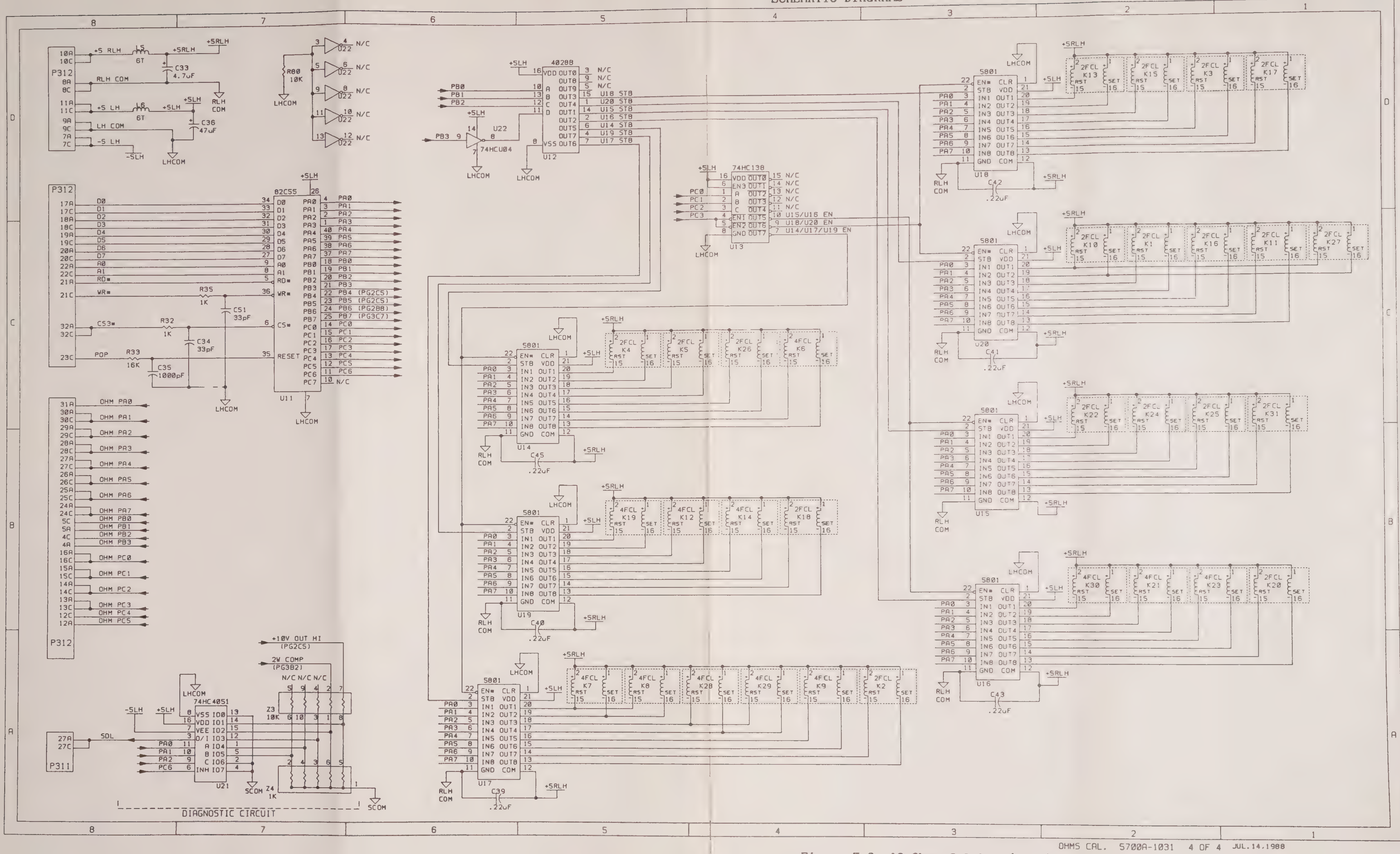

P312
P311
82C55
U11
40288
U12
74HC138
U13
74HCU04
U22
74HC4051
U21
5801
U14
U15
U16
U17
U18
U19
U20
Z3 10K
Z4 1K
C33 4.7uF
C36 47uF
C34 33pF
C35 1000pF
C51 33pF
R80 10K
R32 1K
R33 16K
R35 1K
L5 6T
L6 6T
C39 .22uF
C40 .22uF
C41 .22uF
C42 .22uF
C43 .22uF
C45 .22uF
+5 RLH
+SRLH
RLH COM
+5 LH
+SLH
LH COM
-5 LH
-SLH
LHCOM
SCOM
SDL
POP
WR=
RD=
CS3=
RESET
U18 STB
U20 STB
U15 STB
U16 STB
U14 STB
U19 STB
U17 STB
U15/U16 EN
U18/U20 EN
U14/U17/U19 EN
N/C
PB4 (PG2C5)
PB5 (PG2C5)
PB6 (PG2B8)
PB7 (PG3C7)
OHM PA0
OHM PA1
OHM PA2
OHM PA3
OHM PA4
OHM PA5
OHM PA6
OHM PA7
OHM PB0
OHM PB1
OHM PB2
OHM PB3
OHM PC0
OHM PC1
OHM PC2
OHM PC3
OHM PC4
OHM PC5
+10V OUT HI (PG2C5)
2W COMP (PG3B2)
DIAGNOSTIC CIRCUIT
2FCL K13
2FCL K15
2FCL K3
2FCL K17
2FCL K10
2FCL K1
2FCL K16
2FCL K11
2FCL K27
2FCL K22
2FCL K24
2FCL K25
2FCL K31
4FCL K30
4FCL K21
4FCL K23
2FCL K20
2FCL K4
2FCL K5
2FCL K26
4FCL K6
4FCL K19
4FCL K12
4FCL K14
2FCL K18
4FCL K7
4FCL K8
4FCL K28
4FCL K29
4FCL K9
2FCL K2
RST
SET
OHMS CAL. 5700A-1031 4 OF 4 JUL.14,1988

Figure 7-9. A9 Ohms Cal PCA (cont)

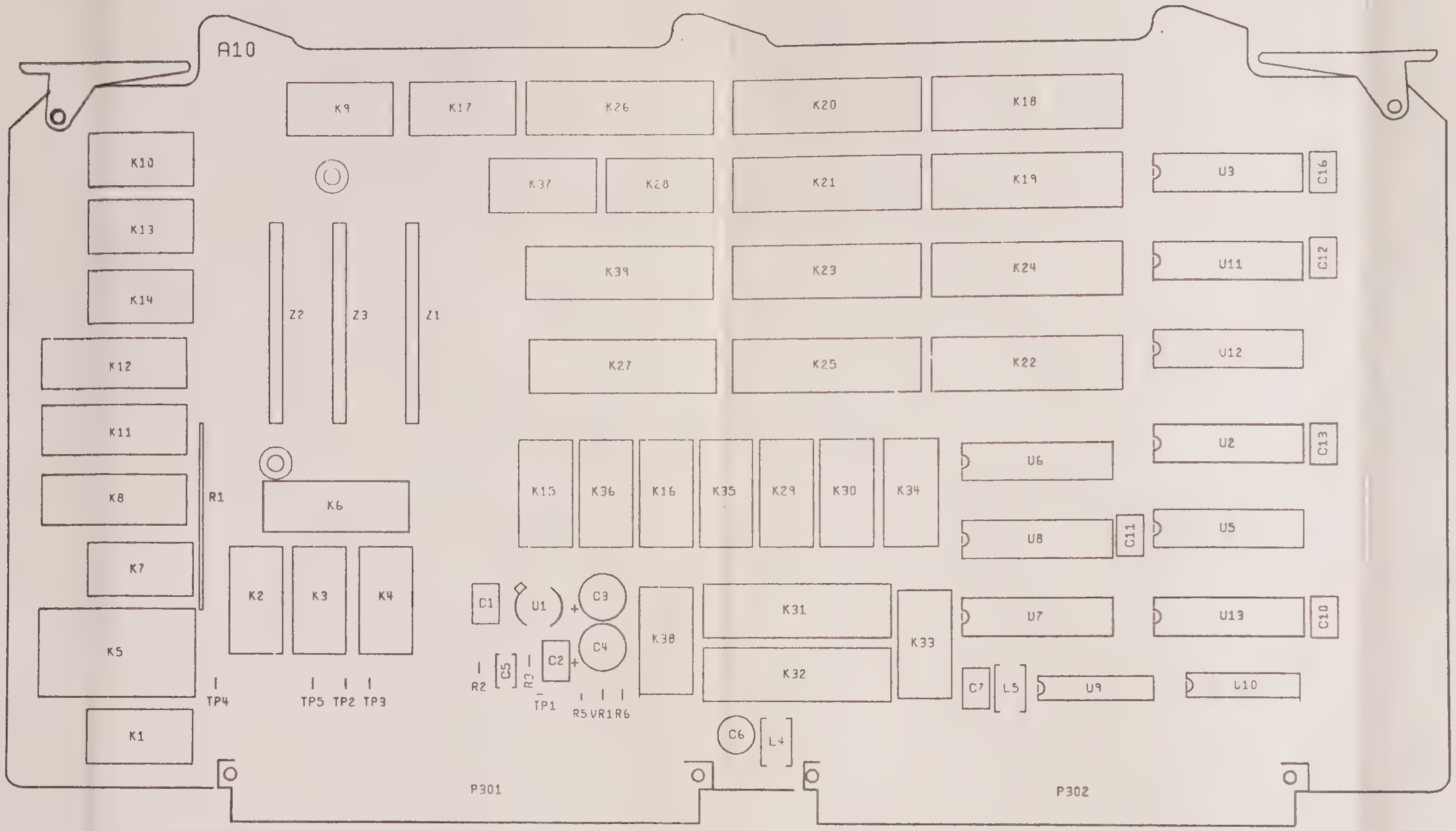
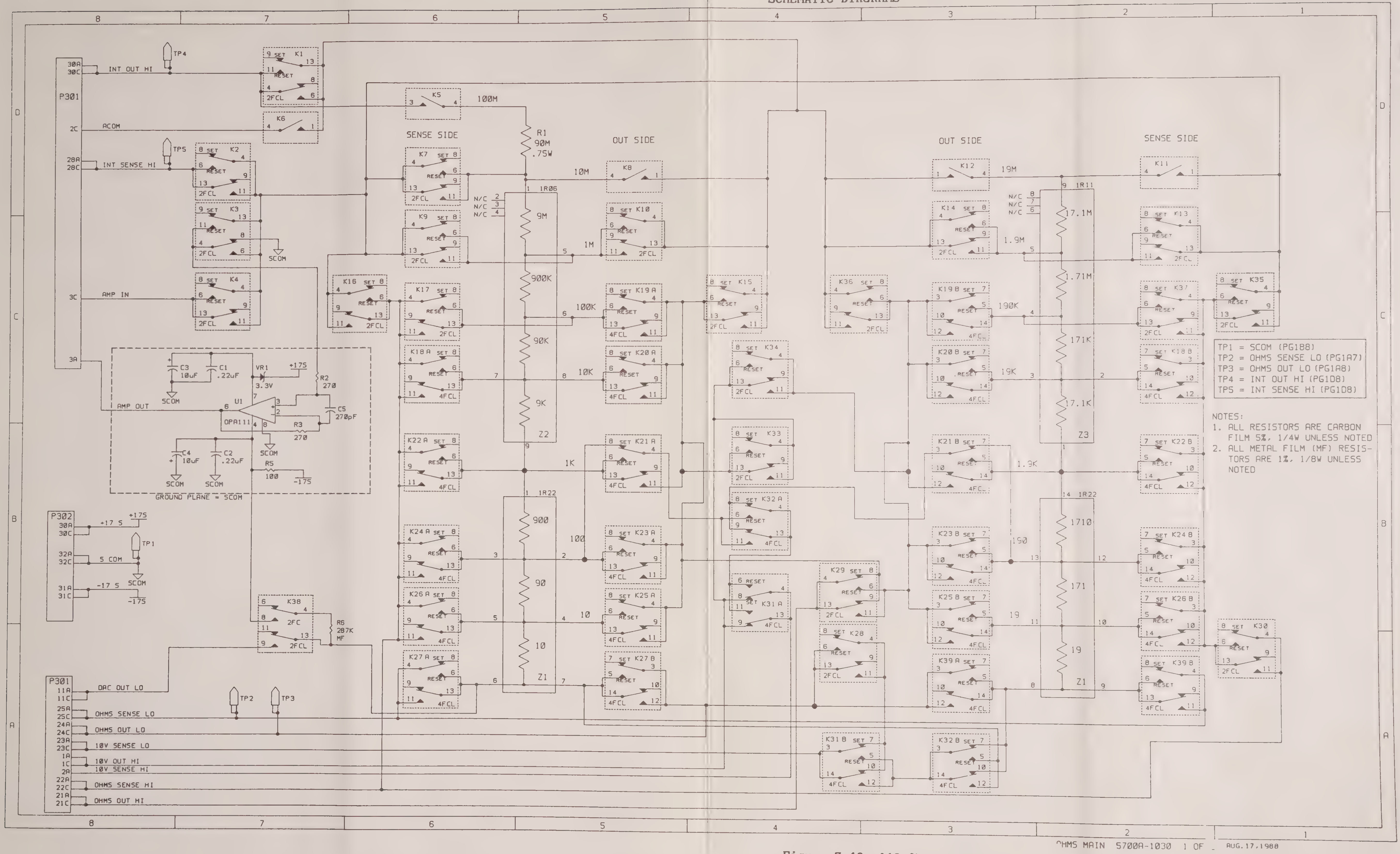

A10
K9
K17
K26
K20
K18
K10
K37
K28
K21
K19
U3
C16
K13
K39
K23
K24
U11
C12
K14
Z2
Z3
Z1
K12
K27
K25
K22
U12
K11
U2
C13
R1
K15
K36
K16
K35
K29
K30
K34
U6
K8
K6
U8
C11
U5
K7
K2
K3
K4
C1
U1
C3
K31
K33
U7
U13
C10
K5
C4
K38
R2
C5
R3
C2
K32
C7
L5
U9
U10
TP4
TP5
TP2
TP3
TP1
R5
VR1
R6
K1
C6
L4
P301
P302

Figure 7-10. A10 Ohms Main PCA


P301
30A
30C
INT OUT HI
TP4
2C
ACOM
28A
28C
INT SENSE HI
TP5
3C
AMP IN
3A
AMP OUT
K1
K2
K3
K4
K5
K6
100M
R1
90M
.75W
SENSE SIDE
OUT SIDE
10M
1M
100K
10K
1K
100
10
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
K18 A
K19 A
K20 A
K21 A
K22 A
K23 A
K24 A
K25 A
K26 A
K27 A
K27 B
K28
K29
K30
K31 A
K31 B
K32 A
K32 B
K33
K34
K35
K36
K37
K38
K39 A
K39 B
K18 B
K19 B
K20 B
K21 B
K22 B
K23 B
K24 B
K25 B
K26 B
SET
RESET
2FCL
4FCL
2FC
N/C
1R06
9M
900K
90K
9K
Z2
1R22
900
90
10
Z1
1R11
17.1M
1.71M
171K
17.1K
Z3
1710
171
19
19M
1.9M
190K
19K
1.9K
190
C3
10uF
C1
.22uF
VR1
3.3V
+175
R2
270
U1
OPA111
C5
270pF
R3
270
SCOM
C4
10uF
C2
.22uF
R5
100
-175
GROUND PLANE = SCOM
P302
+17 S
5 COM
-17 S
TP1
R6
287K
MF
DAC OUT LO
TP2
TP3
11A
11C
25A
25C
OHMS SENSE LO
24A
24C
OHMS OUT LO
23A
23C
10V SENSE LO
1A
1C
10V OUT HI
2A
10V SENSE HI
22A
22C
OHMS SENSE HI
21A
21C
OHMS OUT HI
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TP1 = SCOM (PG1B8)
TP2 = OHMS SENSE LO (PG1A7)
TP3 = OHMS OUT LO (PG1A8)
TP4 = INT OUT HI (PG1D8)
TP5 = INT SENSE HI (PG1D8)

NOTES:

1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED

Figure 7-10. A10 Ohms Main PCA (cont)

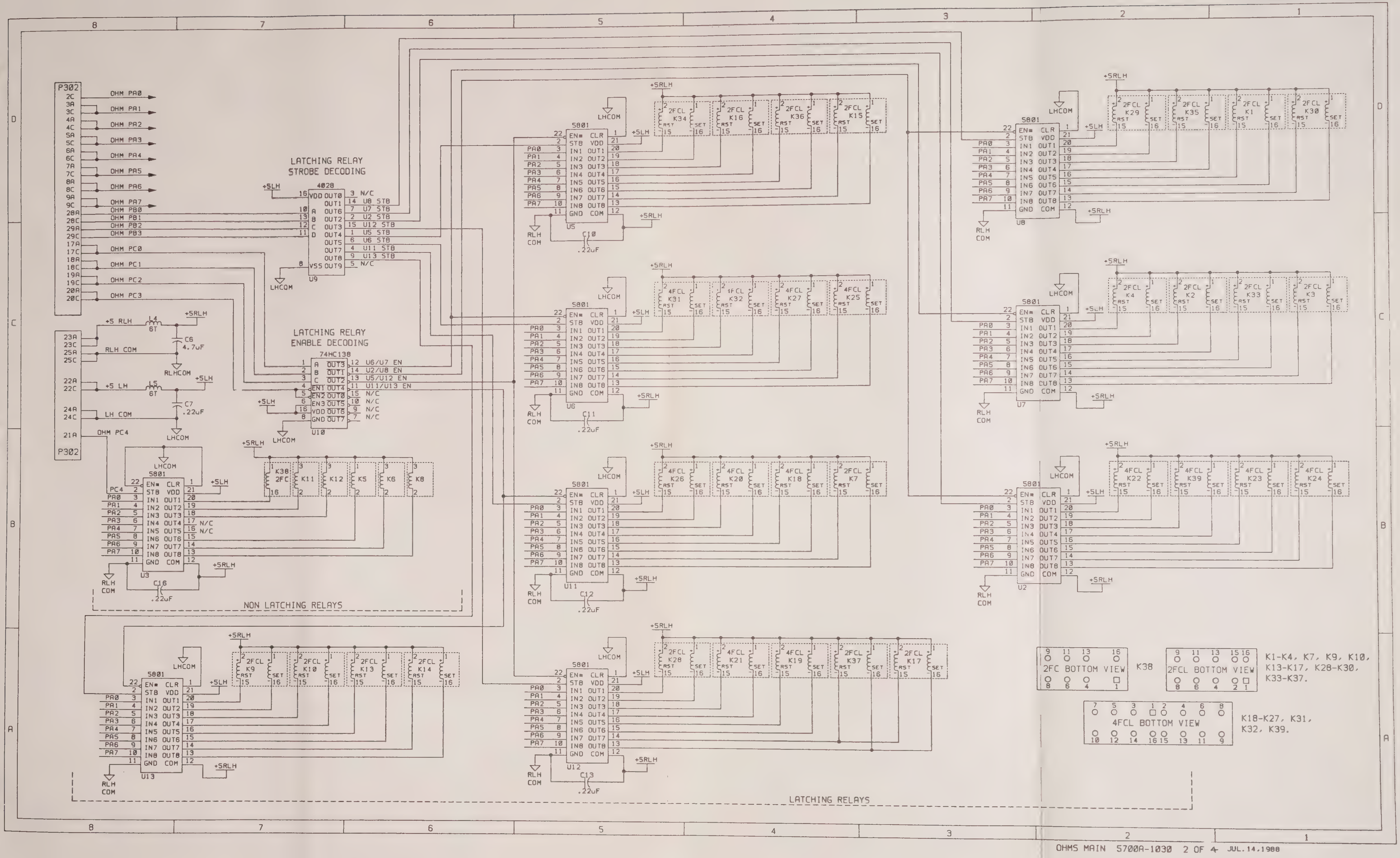
P302
LATCHING RELAY STROBE DECODING
4028
U9
LATCHING RELAY ENABLE DECODING
74HC138
U10
NON LATCHING RELAYS
LATCHING RELAYS
5801
U2
U3
U5
U6
U7
U8
U11
U12
U13
+SRLH
+SLH
LHCOM
RLH COM
RLHCOM
+5 RLH
+5 LH
LH COM
OHM PC4
C6 4.7uF
C7 .22uF
C10 .22uF
C11 .22uF
C12 .22uF
C13 .22uF
C16 .22uF
L4 6T
L5 6T
2FC BOTTOM VIEW
K38
2FCL BOTTOM VIEW
K1-K4, K7, K9, K10, K13-K17, K28-K30, K33-K37.
4FCL BOTTOM VIEW
K18-K27, K31, K32, K39.
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Figure 7-10. A10 Ohms Main PCA (cont)

OHMS MAIN ASSEMBLY RELAYS

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	K34	K35	K36	K37	K38	K39
DORMANT																																							
4 WIRE SHORT	R	R													R	R																							
4 WIRE 1 OHM	R	R													R	R																							
4 WIRE 1.9 OHM	R	R													R	R																							
4 WIRE 10 OHM	R	R													R	R									R	R	R												
4 WIRE 19 OHM	R	R																							R	R									R	R			R
4 WIRE 100 OHM	R	R													R	R							R	R			R												
4 WIRE 190 OHM	R	R																					R	R											R	R			R
4 WIRE 1K OHM	R	R													R	R					R	R					R												
4 WIRE 1.9K OHM	R	R																			R	R													R	R			R
4 WIRE 10K OHM	R	R													R	R		R		R							R												
4 WIRE 19K OHM	R	R																R		R															R	R			R
4 WIRE 100K OHM	R	R													R	R	R		R								R										R		
4 WIRE 190K OHM	R	R															R		R																R	R	R		R
4 WIRE 1M OHM	R	R							R	R																	R												

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	K34	K35	K36	K37	K38	K39
4 WIRE 1.9M OHM	R	R											R	R																									R
4 WIRE 10M OHM	R	R					R	*																			R												
4 WIRE 19M OHM	R	R									*	*																											R
2 WIRE 100M OHM					*																						R												
2 WIRE COMP. SHORT	R	R		R		*																																	
2 WIRE COMP. 1 OHM	R	R		R		*																																	
2 WIRE COMP. 1.9 OHM	R	R		R		*																																	
2 WIRE COMP. 10 OHM	R	R		R		*																			R	R	R												
2 WIRE COMP. 19 OHM	R	R		R		*																			R	R			R	R									R
2 WIRE COMP. 100 OHM	R	R		R		*																	R	R			R												
2 WIRE COMP. 190 OHM	R	R		R		*																	R	R					R	R									R
2 WIRE COMP. 1K OHM	R	R		R		*															R	R					R												
2 WIRE COMP. 1.9K OHM	R	R		R		*															R	R							R	R									R
2 WIRE COMP. 10K OHM	R	R		R		*												R		R							R												
2 WIRE COMP. 19K OHM	R	R		R		*												R		R									R	R									R

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	K34	K35	K36	K37	K38	K39
DIAG SOURCE10																											R	R											
DIAG SOURCES																											R	R											
DIAG SOURCE2																											R	R											
DIAG DIFFAMP																											R	R											
DIAG DIVIDER1																											R	R											
DIAG DIVIDER2																											R	R											
DIAG 10K CAL																				R							R	R											
DIAG 19K CAL																				R								R	R										R
DIAG CHK 10K	R														R			R		R							R												
DIAG CHK 19K	R																	R		R										R						R			R
DIAG CHK 1K	R														R						R	R					R												
DIAG CHK 1.9K	R																				R	R								R						R			R
DIAG CHK 100	R														R								R	R			R												
DIAG CHK 190	R																						R	R						R						R			R

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	K34	K35	K36	K37	K38	K39
DIAG CHK 10	R														R										R	R	R												
DIAG CHK 19	R																								R	R				R						R			R
DIAG 10 CAL																							R			R	R				R	R	R						
DIAG 19 CAL																							R			R				R	R			R					R
DIAG RATIO 100K																		R	R								R	R					R						
DIAG RATIO 190K																		R	R									R		R				R					R
DIAG RATIO 1M			R							R					R	R	R										R	R					R				R		
DIAG RATIO 1.9M			R											R			R											R						R	R	R	R		R
DIAG RATIO 10M			R					*	R						R												R	R					R						
DIAG RATIO 19M1			R									*	R															R						R		R			R
DIAG RATIO 19M2			R								*	*																R						R		R			R
DIAG RATIO 100M	R		R		*		R								R												R	R					R						
DIAG CHK 1	R														R																								
DIAG CHK 1.9	R														R																								
DIAG CHK SHORT	R														R																								
DIAG 2W COMP	R			R		*							R	R											R	R	R												

OHMS CAL ASSEMBLY RELAYS AND FETS

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	Q2	Q3	Q4	Q6
INIT AND STANDBY											R				R			R																	
4 WIRE SHORT							R	R			R				R			R				R		R	R										
4 WIRE 1 OHM				R	R	R					R				R			R				R		R	R										
4 WIRE 1.9 OHM				R	R						R				R			R				R		R	R					R					
4 WIRE 10 OHM											R				R			R				R		R	R										
4 WIRE 19 OHM											R				R			R				R		R	R										
4 WIRE 100 OHM											R				R			R				R		R	R										
4 WIRE 190 OHM											R				R			R				R		R	R										
4 WIRE 1K OHM											R				R			R				R		R	R										
4 WIRE 1.9K OHM											R				R			R				R		R	R										
4 WIRE 10K OHM											R				R			R				R		R	R										
4 WIRE 19K OHM											R				R			R				R		R	R										
4 WIRE 100K OHM											R				R			R				R		R	R										
4 WIRE 190K OHM											R				R			R				R		R	R										
4 WIRE 1M OHM											R				R			R				R		R	R										

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	Q2	Q3	Q4	Q6
4 WIRE 1.9M OHM											R				R			R				R		R	R										
4 WIRE 10M OHM											R				R			R				R		R	R										
4 WIRE 19M OHM											R				R			R				R		R	R										
2 WIRE 100M OHM											R				R			R				R		R											
2 WIRE COMP. SHORT							R	R			R				R			R						R					R	R						*
2 WIRE COMP. 1 OHM				R	R	R					R				R			R						R					R	R						*
2 WIRE COMP. 1.9 OHM				R	R						R				R			R						R					R	R	R					*
2 WIRE COMP. 10 OHM											R				R			R						R					R	R						*
2 WIRE COMP. 19 OHM											R				R			R						R					R	R						*
2 WIRE COMP. 100 OHM											R				R			R						R					R	R						*
2 WIRE COMP. 190 OHM											R				R			R						R					R	R						*
2 WIRE COMP. 1K OHM											R				R			R						R					R	R						*
2 WIRE COMP. 1.9K OHM											R				R			R						R					R	R						*
2 WIRE COMP. 10K OHM											R				R			R						R					R	R						*
2 WIRE COMP. 19K OHM											R				R			R						R					R	R						*

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	Q2	Q3	Q4	Q6
DIAG SOURCE10									R	R	R	R										R	R				R				R				
DIAG SOURCES									R	R	R	R										R	R				R				R	*			
DIAG SOURCE2									R	R	R	R										R	R				R				R	*	*		
DIAG DIFFAMP									R	R		R					R	R		R	R	R					R								
DIAG DIVIDER1									R	R		R				R		R		R	R	R					R								
DIAG DIVIDER2									R	R		R			R			R		R	R	R					R								
DIAG 10K CAL									R	R		R					R		R			R	R				R				R				
DIAG 19K CAL									R	R		R					R		R			R	R				R				R				
DIAG CHK 10K	R									R		R										R	R				R				R				
DIAG CHK 19K	R									R		R										R	R				R				R				
DIAG CHK 1K	R									R		R										R	R				R				R				
DIAG CHK 1.9K	R									R		R										R	R				R				R				
DIAG CHK 100	R									R		R										R	R				R				R				
DIAG CHK 190	R									R		R										R	R				R				R				

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	Q2	Q3	Q4	Q6
DIAG CHK 10	R									R		R										R	R				R				R				
DIAG CHK 19	R									R		R										R	R				R				R				
DIAG 10 CAL		R							R	R				R		R				R	R	R					R					*	*		
DIAG 19 CAL		R							R	R				R		R				R	R	R					R					*	*		
DIAG RATIO 100K	R								R	R		R										R	R				R				R				
DIAG RATIO 190K	R								R	R		R										R	R				R				R				
DIAG RATIO 1M			R						R	R		R										R	R				R				R				
DIAG RATIO 1.9M			R						R	R		R										R	R				R				R				
DIAG RATIO 10M			R						R	R		R										R	R				R				R				
DIAG RATIO 19M1			R						R	R		R										R	R				R				R				
DIAG RATIO 19M2			R						R	R		R										R	R				R				R				
DIAG RATIO 100M			R						R	R		R										R	R				R				R				
DIAG CHK 1	R			R	R	R				R												R					R				R			*	
DIAG CHK 1.9	R			R	R					R												R					R			R	R			*	
DIAG CHK SHORT	R						R	R		R												R					R				R			*	
DIAG 2W COMP																						R						R	R						*

R = RESET POSITION FOR LATCHING RELAYS
* = ENERGIZED POSITION FOR NON LATCHING RELAYS
NOTE: RELAYS SHOWN IN THE SET POSITION ON THE SCHEMATICS

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Figure 7-10. A10 Ohms Main PCA (cont)

OHMS MAIN ASSEMBLY RELAYS

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	K32	K33	K34	K35	K36	K37	K38	K39
10K OHM COMMON MODE MEASUREMENT																											R												
10K BIAS CURRENT MEASUREMENT 1ST																											R												
2ND																											R												
CAL INT 10K STD FROM EXT 10K STD 1ST	R														R													R											
2ND	R														R													R											
3RD	R	R													R	R												R											
CAL 10K FROM INT 10K STD 1ST																				R							R	R											
2ND																				R							R	R											
3RD																		R		R							R	R											
CAL 19K FROM INT 10K STD 1ST																				R								R	R	R									R
2ND																				R								R	R	R									R
3RD																		R		R								R	R	R									R
RATIO CAL 100K FROM 10K 1ST																	R		R								R	R					R				R		
2ND																		R	R								R	R					R						
RATIO CAL 190K FROM 19K 1ST																	R		R									R		R				R			R		R
2ND																		R	R									R		R				R					R
1M OHM COMMON MODE MEASUREMENT			R													R											R												
RATIO CAL 1M FROM 100K 1ST			R						R	R					R												R	R					R						
2ND			R							R					R	R	R										R	R					R				R		
RATIO CAL 1.9M FROM 190K 1ST			R										R	R														R						R		R			R
2ND			R											R			R											R						R	R	R	R		R
RATIO CAL 10M FROM 1M 1ST			R				R	*							R												R	R					R						
2ND			R					*	R						R												R	R					R						
RATIO CAL 19M FROM 1.9M 1ST			R								*	*																R						R		R			R
2ND			R									*	R															R						R		R			R
100M BIAS CURRENT MEASUREMENT 1ST			R													R		R									R												
2ND			R				R																				R												
RATIO CAL 100M FROM 10M	R		R		*		R								R												R	R					R						
RATIO CAL 1K FROM 10K 1ST																		R		R							R	R					R						
2ND																				R		R					R	R					R						
RATIO CAL 1.9K FROM 19K 1ST																		R		R								R		R				R					R
2ND																				R		R						R		R				R					R
CAL INT DIVIDER 1ST																											R	R											
2ND																											R	R											
RATIO CAL 100 OHM FROM 1K 1ST																					R	R					R	R			R	R	R						
2ND																					R			R			R	R			R	R	R						
RATIO CAL 190 OHM FROM 1.9K 1ST																					R	R						R		R	R			R					R
2ND																					R			R				R		R	R			R					R
RATIO CAL 10 OHM FROM 100 OHM 1ST																							R	R			R	R			R	R	R						
2ND																							R			R	R	R			R	R	R						
RATIO CAL 19 OHM FROM 190 OHM 1ST																							R	R				R		R	R			R					R
2ND																							R			R		R		R	R			R					R
1 OHM COMMON MODE MEASUREMENT 1ST		R														R																							
CAL 1 OHM FROM EXT 1 OHM STD 1ST		R														R																							
1 OHM COMMON MODE MEASUREMENT 2ND																																							
CAL 1 OHM FROM EXT 1 OHM STD 2ND																																							
1.9 OHM COMMON MODE MEASUREMENT 1ST		R														R																							
CAL 1.9 OHM FROM EXT 1 OHM STD 1ST		R														R																							
1.9 OHM COMMON MODE MEASUREMENT 2ND																																							
CAL 1.9 OHM FROM EXT 1 OHM STD 2ND																																							
5725A AMP ZERO	R		R												R	R									R	R	R												

OHMS CAL ASSEMBLY RELAYS AND FETS

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31	Q2	Q3	Q4	Q6
10K OHM COMMON MODE MEASUREMENT										R	R	R										R	R				R				R				
10K BIAS CURRENT MEASUREMENT 1ST										R							R			R	R	R					R							*	
2ND										R						R				R	R	R					R							*	
CAL INT 10K STD FROM EXT 10K STD 1ST								R	R		R				R			R			R	R	R	R		R				R				
2ND									R	R		R					R		R			R	R	R	R		R				R				
3RD	R								R	R		R							R			R	R	R	R		R				R				
CAL 10K FROM INT 10K STD 1ST									R	R		R				R			R			R	R				R				R				
2ND									R	R		R					R		R			R	R				R				R				
3RD	R								R	R		R							R			R	R				R				R				
CAL 19K FROM INT 10K STD 1ST									R	R		R				R			R			R	R				R				R				
2ND									R	R		R					R		R			R	R				R				R				
3RD	R								R	R		R							R			R	R				R				R				
RATIO CAL 100K FROM 10K 1ST	R								R	R		R										R	R				R				R				
2ND	R								R	R		R										R	R				R				R				
RATIO CAL 190K FROM 19K 1ST	R								R	R		R										R	R				R				R				
2ND	R								R	R		R										R	R				R				R				
1M OHM COMMON MODE MEASUREMENT		R	R							R		R										R	R				R				R				
RATIO CAL 1M FROM 100K 1ST			R						R	R		R										R	R				R				R				
2ND			R						R	R		R										R	R				R				R				
RATIO CAL 1.9M FROM 190K 1ST			R						R	R		R										R	R				R				R				
2ND			R						R	R		R										R	R				R				R				
RATIO CAL 10M FROM 1M 1ST			R						R	R		R										R	R				R				R				
2ND			R						R	R		R										R	R				R				R				
RATIO CAL 19M FROM 1.9M 1ST			R						R	R		R										R	R				R				R				
2ND			R						R	R		R										R	R				R				R				
100M BIAS CURRENT MEASUREMENT 1ST			R							R												R	R				R				R			*	
2ND			R							R												R	R				R				R			*	
RATIO CAL 100M FROM 10M			R						R	R		R										R	R				R				R				
RATIO CAL 1K FROM 10K 1ST	R								R	R		R										R	R				R				R				
2ND	R								R	R		R										R	R				R				R				
RATIO CAL 1.9K FROM 19K 1ST	R								R	R		R										R	R				R				R				
2ND	R								R	R		R										R	R				R				R				
CAL INT DIVIDER 1ST									R	R		R			R			R		R	R	R					R								
2ND									R	R		R				R		R		R	R	R					R								
RATIO CAL 100 OHM FROM 1K 1ST		R							R	R				R	R					R	R	R					R					*	*		
2ND		R							R	R				R		R				R	R	R					R					*	*		
RATIO CAL 190 OHM FROM 1.9K 1ST		R							R	R				R	R					R	R	R					R					*	*		
2ND		R							R	R				R		R				R	R	R					R					*	*		
RATIO CAL 10 OHM FROM 100 OHM 1ST		R							R	R				R	R					R	R	R					R					*	*		
2ND		R							R	R				R		R				R	R	R					R					*	*		
RATIO CAL 19 OHM FROM 190 OHM 1ST		R							R	R				R	R					R	R	R					R					*	*		
2ND		R							R	R				R		R				R	R	R					R					*	*		
1 OHM COMMON MODE MEASUREMENT 1ST	R					R				R	R											R				R	R				R				
CAL 1 OHM FROM EXT 1 OHM STD 1ST	R					R				R			R									R				R	R				R				
1 OHM COMMON MODE MEASUREMENT 2ND	R			R		R				R	R											R				R	R				R				
CAL 1 OHM FROM EXT 1 OHM STD 2ND	R			R		R				R												R				R	R				R			*	
1.9 OHM COMMON MODE MEASUREMENT 1ST	R									R	R											R				R	R			R	R				
CAL 1.9 OHM FROM EXT 1 OHM STD 1ST	R									R			R									R				R	R			R	R				
1.9 OHM COMMON MODE MEASUREMENT 2ND	R			R						R	R											R				R	R			R	R				
CAL 1.9 OHM FROM EXT 1 OHM STD 2ND	R			R						R												R				R	R			R	R			*	
5725A AMP ZERO			R																			R					R				R			*	

R = RESET POSITION FOR LATCHING RELAYS
* = ENERGIZED POSITION FOR NON LATCHING RELAYS AND ON FOR FETS
NOTE: RELAYS SHOWN IN THE SET POSITION ON THE SCHEMATICS

OHMS MAIN 5700A-1030 4 OF 4 SEPT.7,1988

Figure 7-10. A10 Ohms Main PCA (cont)

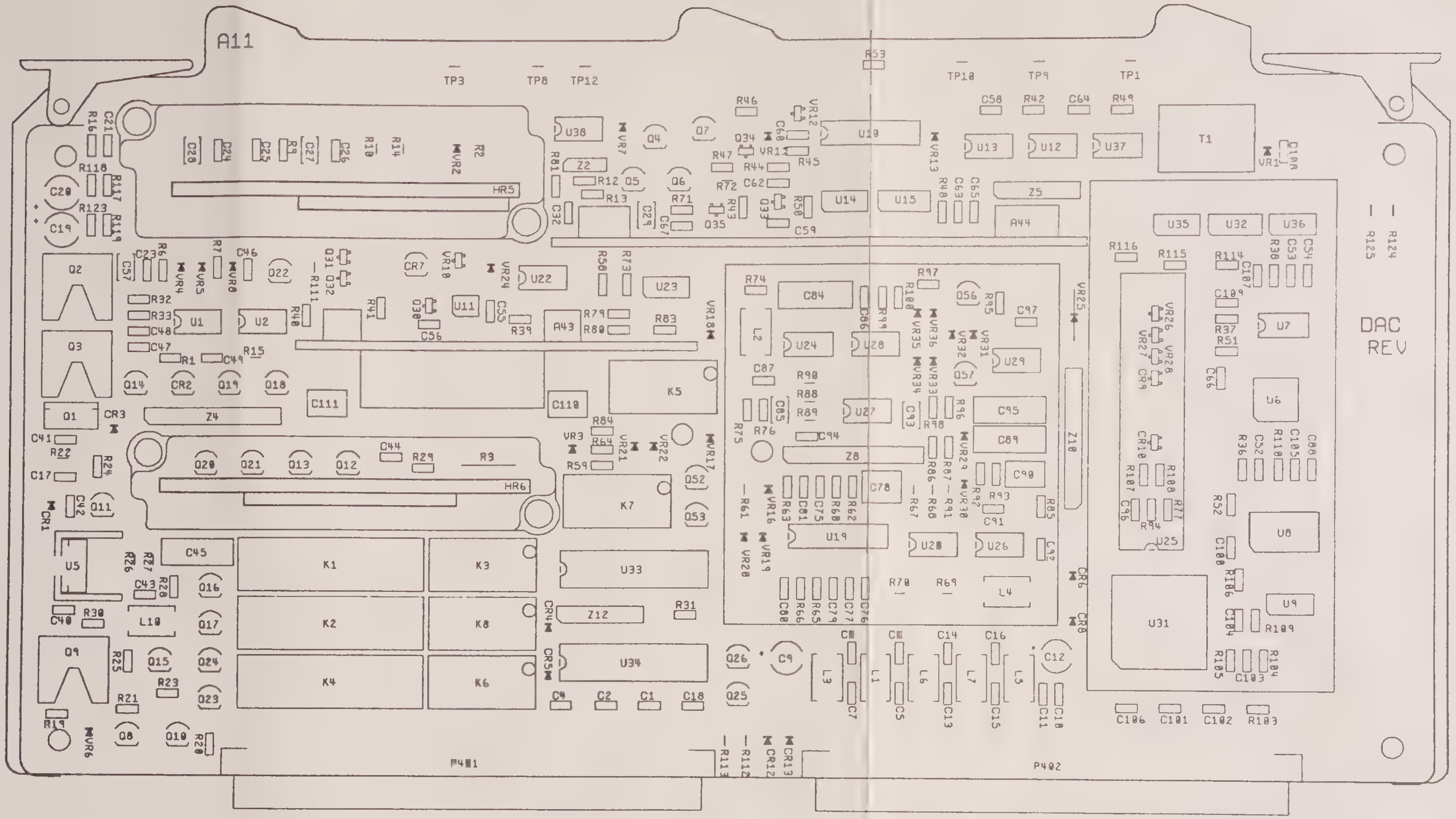
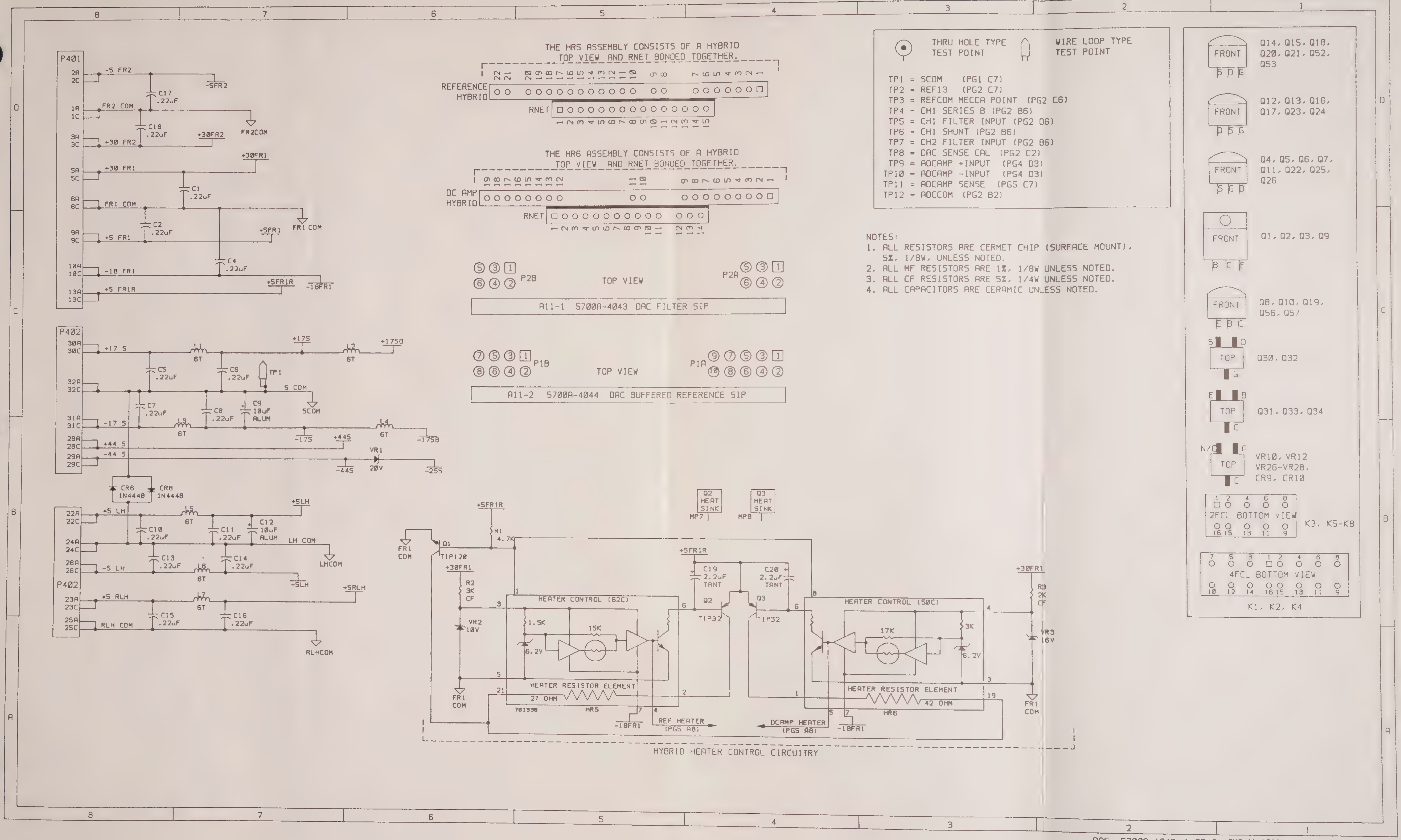

A11
TP3
TP8
TP12
R53
TP10
TP9
TP1
T1
U38
U10
U13
U12
U37
U14
U15
Z5
A44
U35
U32
U36
R125
R124
DAC
REV
HR5
Z2
U22
U23
U1
U2
U11
R43
U24
U28
U29
U27
Z8
C84
C95
C89
C90
C78
U19
U20
U26
L4
Z10
U7
U6
U8
U25
U9
U31
Q2
Q3
Q1
CR3
Z4
C111
C110
K5
HR6
K7
Q52
Q53
U5
C45
K1
K3
U33
K2
K8
Z12
K4
K6
U34
Q9
L10
C9
C12
L3
L1
L6
L7
L5
C106
C101
C102
R103
P401
P402
R111
R112
CR12
CR13

Figure 7-11. A11 DAC PCA


P401
2A 2C -5 FR2
C17 .22uF
-5FR2
1A 1C FR2 COM
C18 .22uF
FR2COM
3A 3C +30 FR2
+30FR2
+30FR1
5A 5C +30 FR1
C1 .22uF
6A 6C FR1 COM
C2 .22uF
FR1 COM
9A 9C +5 FR1
+5FR1
C4 .22uF
10A 10C -18 FR1
13A 13C +5 FR1R
+5FR1R
-18FR1
P402
30A 30C +17 S
L1 6T
+17S
L2 6T
+17SB
C5 .22uF
C6 .22uF
TP1
32A 32C
S COM
C7 .22uF
C8 .22uF
C9 10uF ALUM
SCOM
31A 31C -17 S
L3 6T
L4 6T
-17S
+44S
-17SB
28A 28C +44 S
29A 29C -44 S
VR1 20V
-44S
-25S
CR6 1N4448
CR8 1N4448
22A 22C +5 LH
L5 6T
+5LH
C10 .22uF
C11 .22uF
C12 10uF ALUM
24A 24C
LH COM
LHCOM
26A 26C -5 LH
C13 .22uF
L6 6T
C14 .22uF
-5LH
P402
23A 23C +5 RLH
L7 6T
+5RLH
C15 .22uF
C16 .22uF
25A 25C RLH COM
RLHCOM
THE HR5 ASSEMBLY CONSISTS OF A HYBRID TOP VIEW AND RNET BONDED TOGETHER.
REFERENCE HYBRID
RNET
THE HR6 ASSEMBLY CONSISTS OF A HYBRID TOP VIEW AND RNET BONDED TOGETHER.
DC AMP HYBRID
RNET
P2B
TOP VIEW
P2A
A11-1 5700A-4043 DAC FILTER SIP
P1B
TOP VIEW
P1A
A11-2 5700A-4044 DAC BUFFERED REFERENCE SIP
Q2 HEAT SINK
MP7
Q3 HEAT SINK
MP8
+5FR1R
R1 4.7K
FR1 COM
Q1 TIP120
+30FR1
R2 3K CF
VR2 10V
FR1 COM
+5FR1R
C19 2.2uF TANT
C20 2.2uF TANT
Q2 TIP32
Q3 TIP32
HEATER CONTROL (62C)
1.5K
15K
6.2V
HEATER RESISTOR ELEMENT
27 OHM
HR5
781330
-18FR1
REF HEATER (PG5 A8)
DCAMP HEATER (PG5 A8)
-18FR1
HEATER CONTROL (50C)
17K
3K
6.2V
HEATER RESISTOR ELEMENT
42 OHM
HR6
+30FR1
R3 2K CF
VR3 16V
FR1 COM
HYBRID HEATER CONTROL CIRCUITRY
FRONT
Q14, Q15, Q18, Q20, Q21, Q52, Q53
Q12, Q13, Q16, Q17, Q23, Q24
Q4, Q5, Q6, Q7, Q11, Q22, Q25, Q26
Q1, Q2, Q3, Q9
B C E
Q8, Q10, Q19, Q56, Q57
E B C
TOP
Q30, Q32
Q31, Q33, Q34
N/C
VR10, VR12 VR26-VR28, CR9, CR10
2FCL BOTTOM VIEW
K3, K5-K8
4FCL BOTTOM VIEW
K1, K2, K4

THRU HOLE TYPE TEST POINT

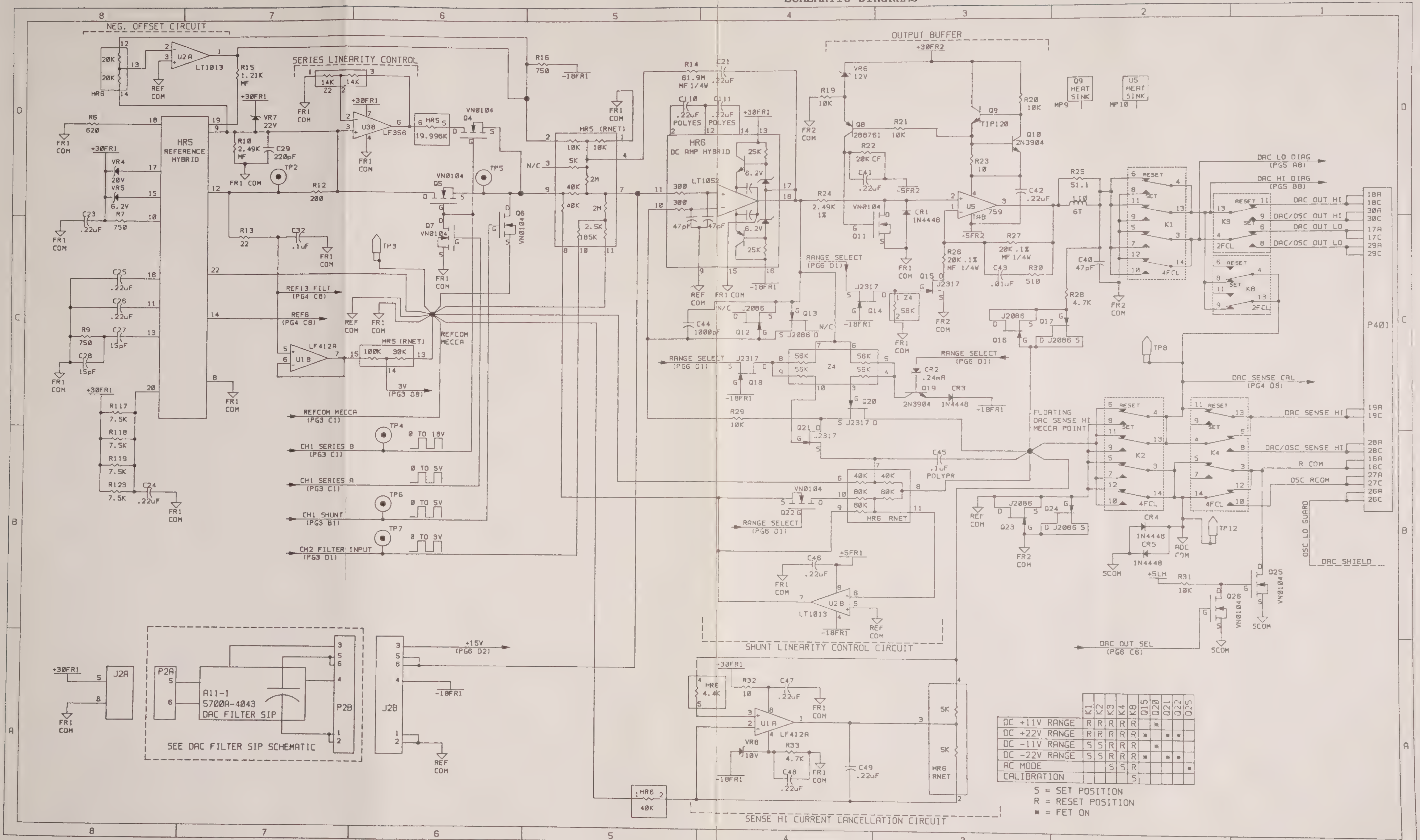
WIRE LOOP TYPE TEST POINT

TP1 = SCOM (PG1 C7)
TP2 = REF13 (PG2 C7)
TP3 = REFCOM MECCA POINT (PG2 C6)
TP4 = CH1 SERIES B (PG2 B6)
TP5 = CH1 FILTER INPUT (PG2 D6)
TP6 = CH1 SHUNT (PG2 B6)
TP7 = CH2 FILTER INPUT (PG2 B6)
TP8 = DAC SENSE CAL (PG2 C2)
TP9 = ADCAMP +INPUT (PG4 D3)
TP10 = ADCAMP -INPUT (PG4 D3)
TP11 = ADCAMP SENSE (PG5 C7)
TP12 = ADCCOM (PG2 B2)

NOTES:
1. ALL RESISTORS ARE CERMET CHIP (SURFACE MOUNT), 5%, 1/8W, UNLESS NOTED.
2. ALL MF RESISTORS ARE 1%, 1/8W UNLESS NOTED.
3. ALL CF RESISTORS ARE 5%, 1/4W UNLESS NOTED.
4. ALL CAPACITORS ARE CERAMIC UNLESS NOTED.

DAC 5700A-1040 1 OF 6 AUG.11,1988

Figure 7-11. A11 DAC PCA (cont)


NEG. OFFSET CIRCUIT
SERIES LINEARITY CONTROL
OUTPUT BUFFER
U2A
LT1013
R15
1.21K
MF
HR6
REF COM
+30FR1
VR7
22V
R6
620
FR1 COM
HR5
REFERENCE HYBRID
VR4
20V
VR5
6.2V
C23
.22uF
R7
750
R10
2.49K
MF
C29
220pF
TP2
R12
200
U3B
LF356
HR5
19.996K
VN0104
Q4
TP5
Q5
Q6
Q7
R16
750
-18FR1
HR5 (RNET)
N/C
TP3
R13
22
C32
.1uF
C25
.22uF
C26
.22uF
R9
750
C27
15pF
C28
15pF
REF13 FILT
(PG4 C8)
REF6
(PG4 C8)
LF412A
U1B
3V
(PG3 D8)
REFCOM MECCA
R117
7.5K
R118
7.5K
R119
7.5K
R123
7.5K
C24
.22uF
REFCOM MECCA
(PG3 C1)
TP4
0 TO 18V
CH1 SERIES B
(PG3 C1)
0 TO 5V
CH1 SERIES A
(PG3 C1)
TP6
0 TO 5V
CH1 SHUNT
(PG3 B1)
TP7
0 TO 3V
CH2 FILTER INPUT
(PG3 D1)
R14
61.9M
MF 1/4W
C21
.22uF
C110
.22uF
POLYES
C111
.22uF
POLYES
HR6
DC AMP HYBRID
LT1052
6.2V
25K
47pF
C44
1000pF
Q12
Q13
J2086
RANGE SELECT
(PG6 D1)
J2317
Q18
R29
10K
Z4
56K
Q20
Q21
VN0104
Q22
HR6 RNET
40K
80K
C45
.22uF
+5FR1
U2B
LT1013
SHUNT LINEARITY CONTROL CIRCUIT
VR6
12V
R19
10K
Q8
2N3904
R21
10K
Q9
TIP120
Q10
2N3904
R20
10K
R22
20K CF
C41
.22uF
R23
10
-5FR2
R24
2.49K
1%
VN0104
Q11
CR1
1N4448
U5
759
TAB
C42
.22uF
R26
20K .1%
MF 1/4W
R27
20K .1%
MF 1/4W
C43
.01uF
R30
510
Q15
Q14
R28
4.7K
Q16
Q17
CR2
.24mA
Q19
CR3
1N4448
Q9
HEAT SINK
MP9
U5
HEAT SINK
MP10
R25
51.1
L10
6T
C40
47pF
K1
K3
K8
4FCL
2FCL
RESET
SET
DAC LO DIAG
(PG5 A8)
DAC HI DIAG
(PG5 B8)
DAC OUT HI
DAC/OSC OUT HI
DAC OUT LO
DAC/OSC OUT LO
P401
TP8
DAC SENSE CAL
(PG4 D8)
FLOATING DAC SENSE HI MECCA POINT
K2
K4
DAC SENSE HI
DAC/OSC SENSE HI
R COM
OSC RCOM
C45
.1uF
POLYPR
Q23
Q24
CR4
1N4448
CR5
1N4448
SCOM
ADC COM
TP12
OSC LO GUARD
DAC SHIELD
+5LH
R31
10K
Q25
Q26
VN0104
DAC OUT SEL
(PG6 C6)
J2A
P2A
A11-1
5700A-4043
DAC FILTER SIP
P2B
SEE DAC FILTER SIP SCHEMATIC
J2B
+15V
(PG6 D2)
REF COM
HR6
4.4K
R32
10
C47
.22uF
U1A
LF412A
VR8
10V
R33
4.7K
C48
.22uF
C49
.22uF
5K
HR6 RNET
HR6
40K
SENSE HI CURRENT CANCELLATION CIRCUIT

	K1	K2	K3	K4	K8	Q15	Q20	Q21	Q22	Q25
DC +11V RANGE	R	R	R	R	R		■			
DC +22V RANGE	R	R	R	R	R	■		■	■	
DC -11V RANGE	S	S	R	R	R		■			
DC -22V RANGE	S	S	R	R	R	■		■	■	
AC MODE			S	S	R					■
CALIBRATION					S					

S = SET POSITION
R = RESET POSITION
■ = FET ON

DAC 5700A-1040 2 OF 6 AUG.11,1988

Figure 7-11. A11 DAC PCA (cont)

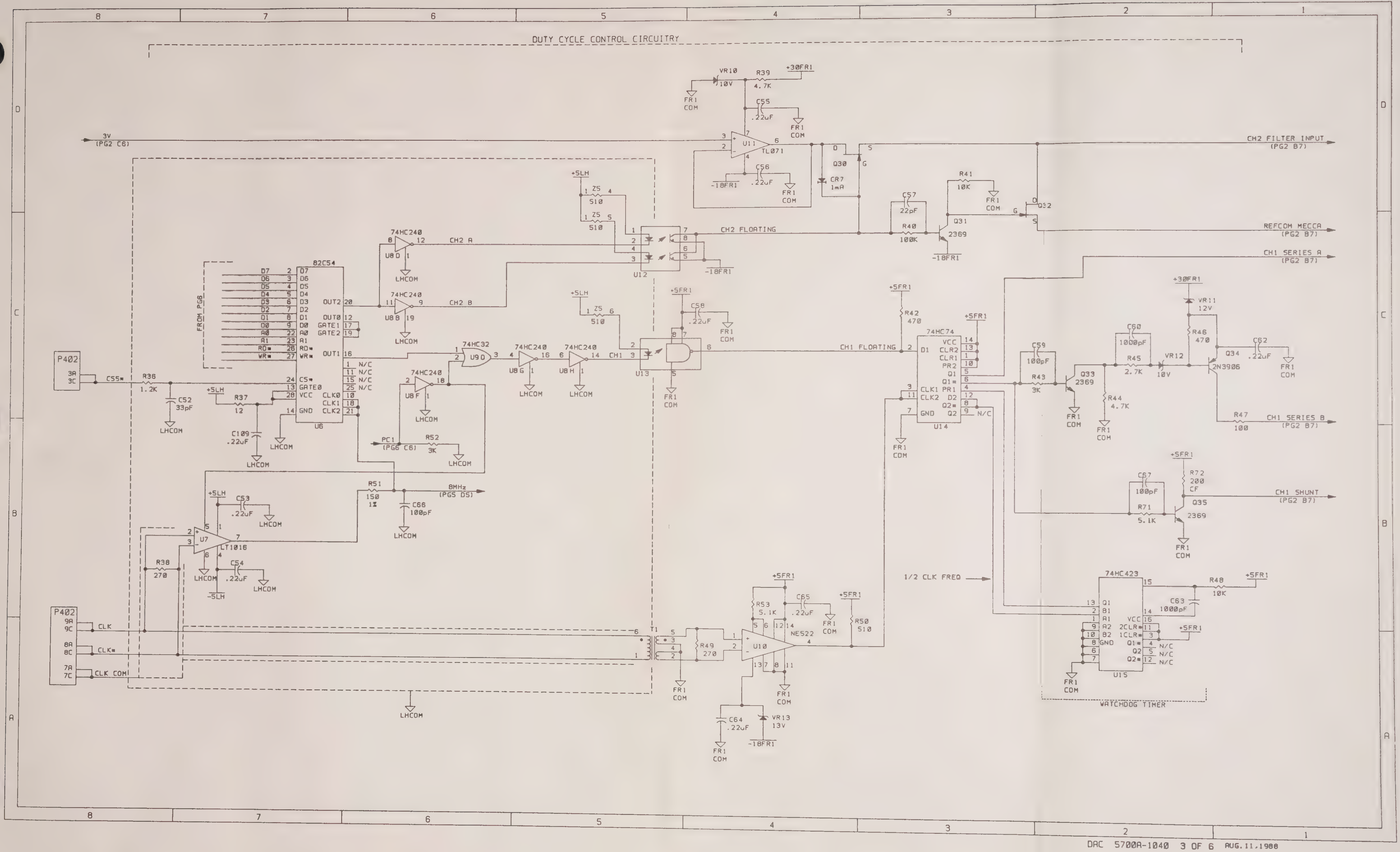

DUTY CYCLE CONTROL CIRCUITRY
VR10 10V
R39 4.7K
+30FR1
C55 .22uF
FR1 COM
3V (PG2 C6)
U11 TL071
C56 .22uF
-18FR1
Q30
CR7 1mA
CH2 FILTER INPUT (PG2 B7)
R41 10K
Q32
C57 22pF
R40 100K
Q31 2369
REFCOM MECCA (PG2 B7)
CH1 SERIES A (PG2 B7)
+5LH
Z5 510
74HC240
U8 D
U8 B
CH2 A
CH2 B
CH2 FLOATING
U12
LHCOM
82C54
D7 D6 D5 D4 D3 D2 D1 D0 A0 A1 RD* WR*
FROM PG6
OUT2 OUT0 GATE1 GATE2 OUT1
CS* GATE0 VCC GND CLK0 CLK1 CLK2
N/C
U6
P402 3A 3C
CS5*
R36 1.2K
C52 33pF
R37 12
C109 .22uF
74HC32 U9 D
U8 G
U8 H
U8 F
CH1
U13
C58 .22uF
+5FR1
PC1 (PG6 C6)
R52 3K
R51 150 1%
8MHz (PG5 D5)
C66 100pF
C53 .22uF
U7 LT1016
C54 .22uF
-5LH
R38 270
P402 9A 9C 8A 8C 7A 7C
CLK
CLK*
CLK COM
T1
R49 270
U10 NE522
R53 5.1K
C65 .22uF
R50 510
C64 .22uF
VR13 13V
R42 470
CH1 FLOATING
74HC74
D1 VCC CLR2 CLR1 PR2 Q1 Q1* CLK1 PR1 CLK2 D2 Q2* GND Q2
U14
C59 100pF
R43 3K
Q33 2369
C60 1000pF
R45 2.7K
VR12 10V
R44 4.7K
VR11 12V
R46 470
Q34 2N3906
C62 .22uF
R47 100
CH1 SERIES B (PG2 B7)
R72 200 CF
C67 100pF
R71 5.1K
Q35 2369
CH1 SHUNT (PG2 B7)
1/2 CLK FREQ
74HC423
Q1 B1 A1 A2 B2 GND VCC 2CLR* 1CLR* Q1* Q2 Q2*
U15
R48 10K
C63 1000pF
WATCHDOG TIMER
DAC 5700A-1040 3 OF 6 AUG.11.1988

Figure 7-11. A11 DAC PCA (cont)

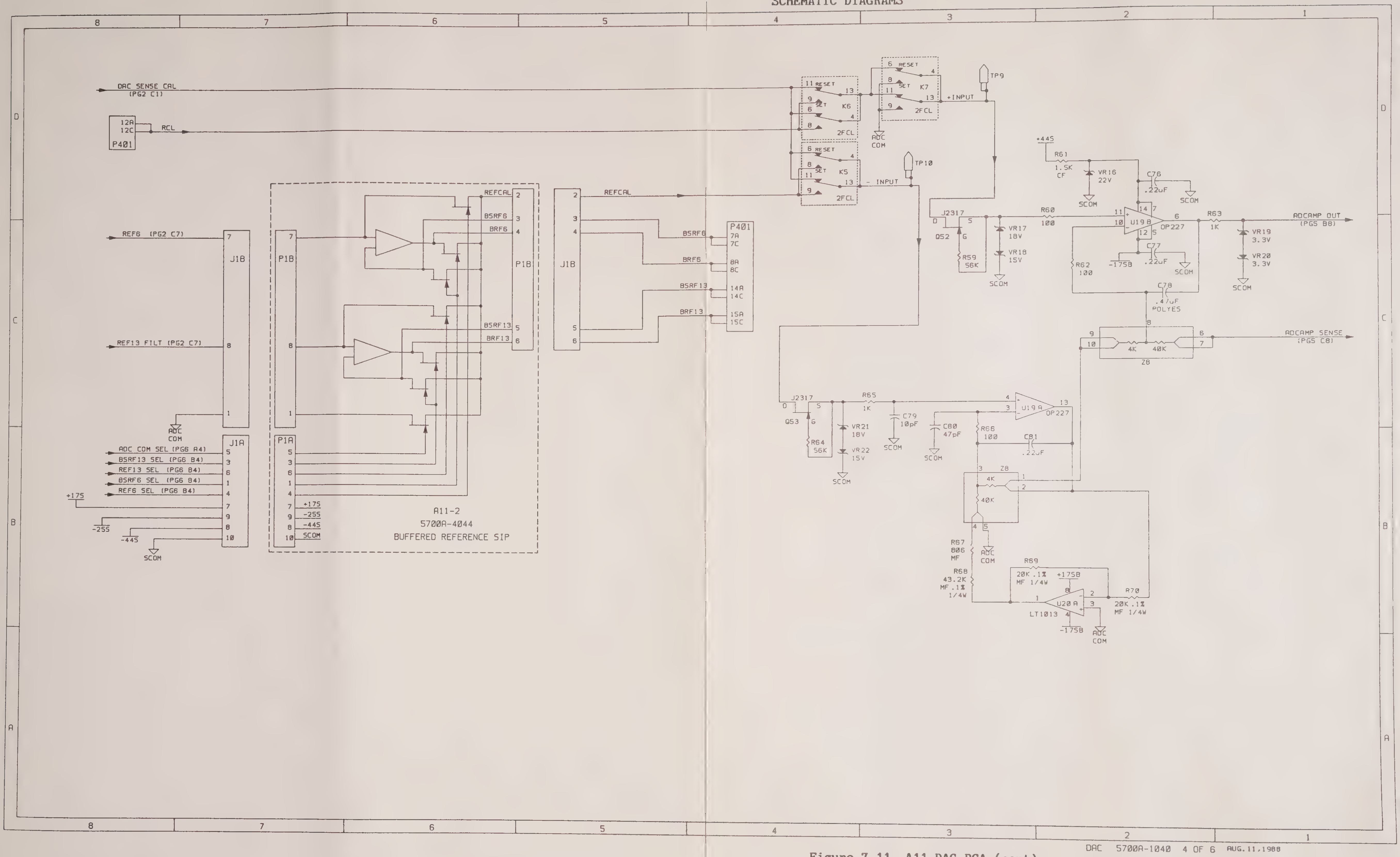

DAC SENSE CAL (PG2 C1)
P401
12A
12C
RCL
REF6 (PG2 C7)
REF13 FILT (PG2 C7)
J1B
P1B
ADC COM
J1A
ADC COM SEL (PG6 A4)
BSRF13 SEL (PG6 B4)
REF13 SEL (PG6 B4)
BSRF6 SEL (PG6 B4)
REF6 SEL (PG6 B4)
+175
-255
-445
SCOM
P1A
REFCAL
BSRF6
BRF6
BSRF13
BRF13
A11-2
5700A-4044
BUFFERED REFERENCE SIP
7A
7C
8A
8C
14A
14C
15A
15C
K6
K7
K5
RESET
SET
2FCL
+INPUT
- INPUT
TP9
TP10
J2317
Q52
Q53
R59 56K
R64 56K
VR17 18V
VR18 15V
VR21 18V
VR22 15V
R60 100
+445
R61 1.5K CF
VR16 22V
C76 .22uF
U19 B
OP227
C77 .22uF
-175B
R62 100
R63 1K
ADCAMP OUT (PG5 B8)
VR19 3.3V
VR20 3.3V
C78 .47uF POLYES
Z8
4K
40K
ADCAMP SENSE (PG5 C8)
R65 1K
C79 10pF
C80 47pF
R66 100
C81 .22uF
U19 A
OP227
R67 806 MF
R68 43.2K MF .1% 1/4W
R69 20K .1% MF 1/4W
+175B
U20 A
LT1013
R70 20K .1% MF 1/4W
DAC 5700A-1040 4 OF 6 AUG.11,1988

Figure 7-11. A11 DAC PCA (cont)

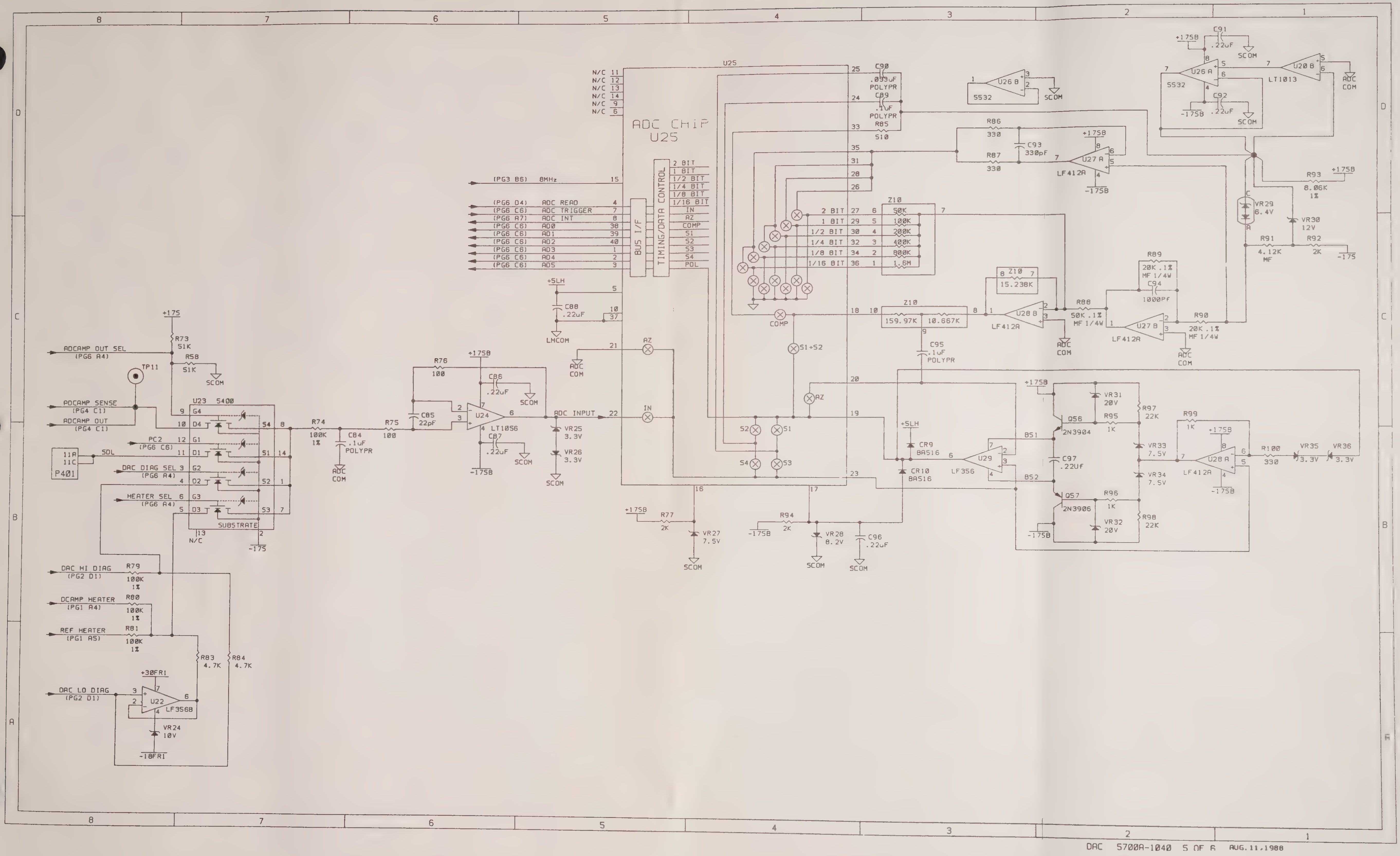

ADC CHIP
U25
BUS I/F
TIMING/DATA CONTROL
(PG3 B6) 8MHz
(PG6 D4) ADC READ
(PG6 C6) ADC TRIGGER
(PG6 A7) ADC INT
(PG6 C6) AD0
(PG6 C6) AD1
(PG6 C6) AD2
(PG6 C6) AD3
(PG6 C6) AD4
(PG6 C6) AD5
2 BIT
1 BIT
1/2 BIT
1/4 BIT
1/8 BIT
1/16 BIT
IN
AZ
COMP
S1
S2
S3
S4
POL
N/C
C90 .033uF POLYPR
C89 .1uF POLYPR
R85 510
Z10 50K 100K 200K 400K 800K 1.6M
R86 330
R87 330
C93 330pF
U27 A LF412A
U26 B 5532
U26 A 5532
U20 B LT1013
C91 .22uF
C92 .22uF
R93 8.06K 1%
VR29 6.4V
VR30 12V
R91 4.12K MF
R92 2K
R89 20K .1% MF 1/4W
C94 1000PF
Z10 15.238K
U28 B LF412A
R88 50K .1% MF 1/4W
U27 B LF412A
R90 20K .1% MF 1/4W
Z10 159.97K 10.667K
C95 .1uF POLYPR
COMP
S1+S2
AZ
IN
ADC INPUT
ADC COM
SCOM
LHCOM
+5LH
C88 .22uF
+175B
-175B
+175
-175
ADCAMP OUT SEL (PG6 A4)
R73 51K
R58 51K
TP11
ADCAMP SENSE (PG4 C1)
ADCAMP OUT (PG4 C1)
PC2 (PG6 C6)
SDL
11A 11C P401
DAC DIAG SEL (PG6 A4)
HEATER SEL (PG6 A4)
U23 5400
SUBSTRATE
N/C
R74 100K 1%
C84 .1uF POLYPR
R75 100
C85 22pF
R76 100
U24 LT1056
C86 .22uF
C87 .22uF
VR25 3.3V
VR26 3.3V
DAC HI DIAG (PG2 D1)
R79 100K 1%
DCAMP HEATER (PG1 A4)
R80 100K 1%
REF HEATER (PG1 A5)
R81 100K 1%
R83 4.7K
R84 4.7K
DAC LO DIAG (PG2 D1)
+30FR1
U22 LF356B
VR24 10V
-18FR1
R77 2K
VR27 7.5V
R94 2K
VR28 8.2V
C96 .22uF
+5LH
CR9 BAS16
CR10 BAS16
U29 LF356
BS1
BS2
C97 .22uF
Q56 2N3904
Q57 2N3906
VR31 20V
VR32 20V
R95 1K
R96 1K
R97 22K
R98 22K
VR33 7.5V
VR34 7.5V
R99 1K
U28 A LF412A
R100 330
VR35 3.3V
VR36 3.3V
DAC 5700A-1040 5 OF 6 AUG.11.1988

Figure 7-11. A11 DAC PCA (cont)

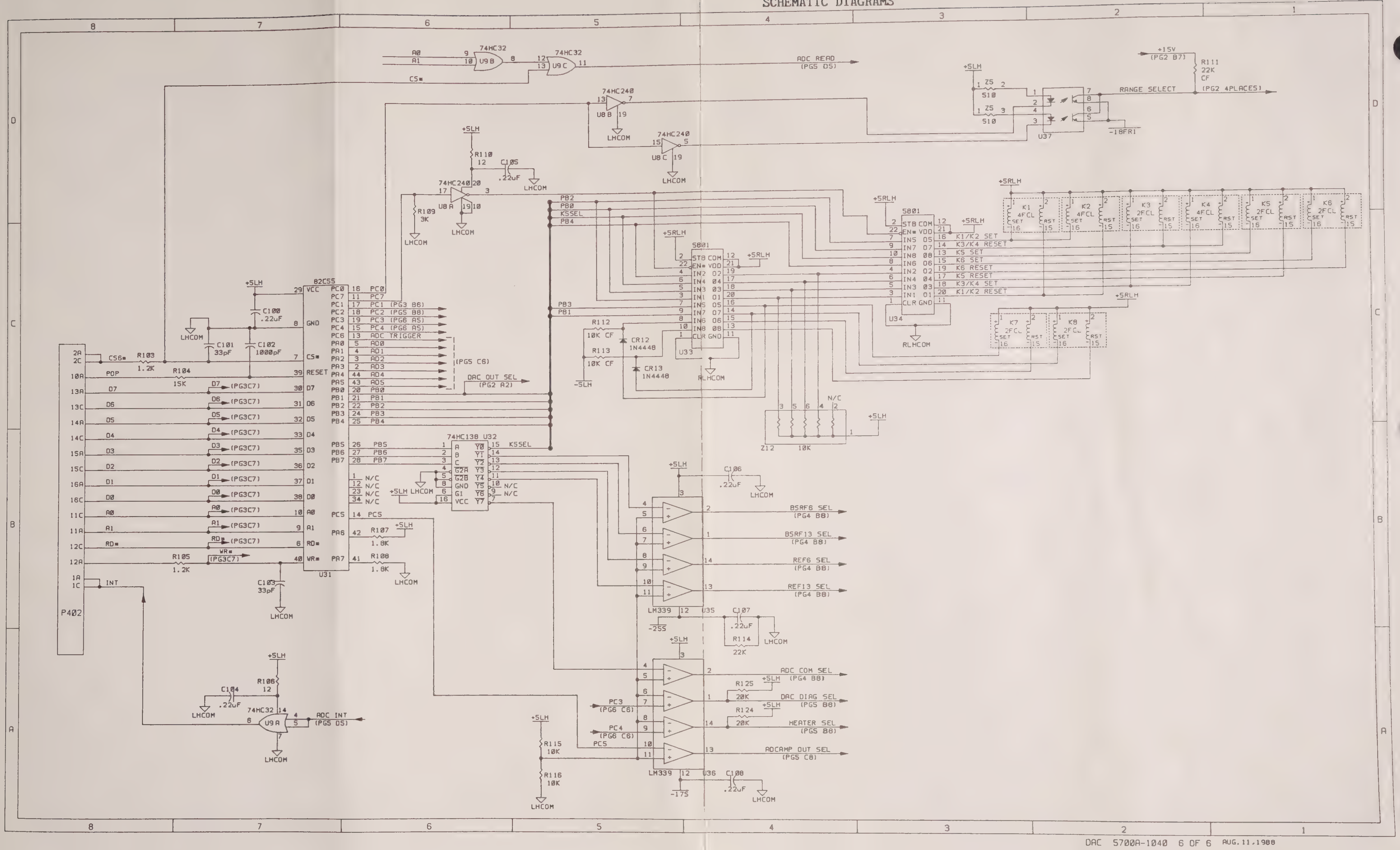

8
7
6
5
4
3
2
1
D
C
B
A
74HC32
U9B
U9C
A0
A1
CS=
ADC READ
(PG5 D5)
74HC240
U8B
U8C
U8A
LHCOM
+5LH
R110
12
C105
.22uF
R109
3K
+15V
(PG2 B7)
R111
22K
CF
RANGE SELECT
(PG2 4PLACES)
Z5
510
U37
-18FR1
+SRLH
K1 4FCL
K2 4FCL
K3 2FCL
K4 4FCL
K5 2FCL
K6 2FCL
K7 2FCL
K8 2FCL
SET
RST
5801
U34
U33
RLHCOM
K1/K2 SET
K3/K4 RESET
K5 SET
K6 SET
K6 RESET
K5 RESET
K3/K4 SET
K1/K2 RESET
PB2
PB0
K5SEL
PB4
PB3
PB1
R112
10K CF
R113
10K CF
CR12
1N4448
CR13
1N4448
-5LH
Z12
10K
N/C
82C55
U31
VCC
GND
CS=
RESET
C100
.22uF
C101
33pF
C102
1000pF
R103
1.2K
R104
15K
R105
1.2K
CS6=
POP
D7
D6
D5
D4
D3
D2
D1
D0
RD=
WR=
INT
(PG3C7)
PC0
PC7
PC1 (PG3 B6)
PC2 (PG5 B8)
PC3 (PG6 A5)
PC4 (PG6 A5)
ADC TRIGGER
AD0
AD1
AD2
AD3
AD4
AD5
(PG5 C6)
DAC OUT SEL
(PG2 A2)
PCS
PA6
PA7
R107
1.8K
R108
1.8K
C103
33pF
P402
2A
2C
10A
13A
13C
14A
14C
15A
15C
16A
16C
11C
11A
12C
12A
1A
1C
74HC138 U32
N/C
LM339
U35
U36
C106
.22uF
C107
.22uF
R114
22K
-255
-175
C108
.22uF
BSRF6 SEL
(PG4 B8)
BSRF13 SEL
(PG4 B8)
REF6 SEL
(PG4 B8)
REF13 SEL
(PG4 B8)
ADC COM SEL
(PG4 B8)
R125
20K
DAC DIAG SEL
(PG5 B8)
R124
20K
HEATER SEL
(PG5 B8)
ADCAMP OUT SEL
(PG5 C8)
PC3
(PG6 C6)
PC4
(PG6 C6)
R115
10K
R116
10K
R106
12
C104
.22uF
74HC32
U9A
ADC INT
(PG5 D5)
DAC 5700A-1040 6 OF 6 AUG.11.1988

Figure 7-11. A11 DAC PCA (cont)

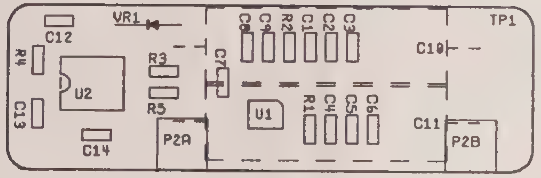
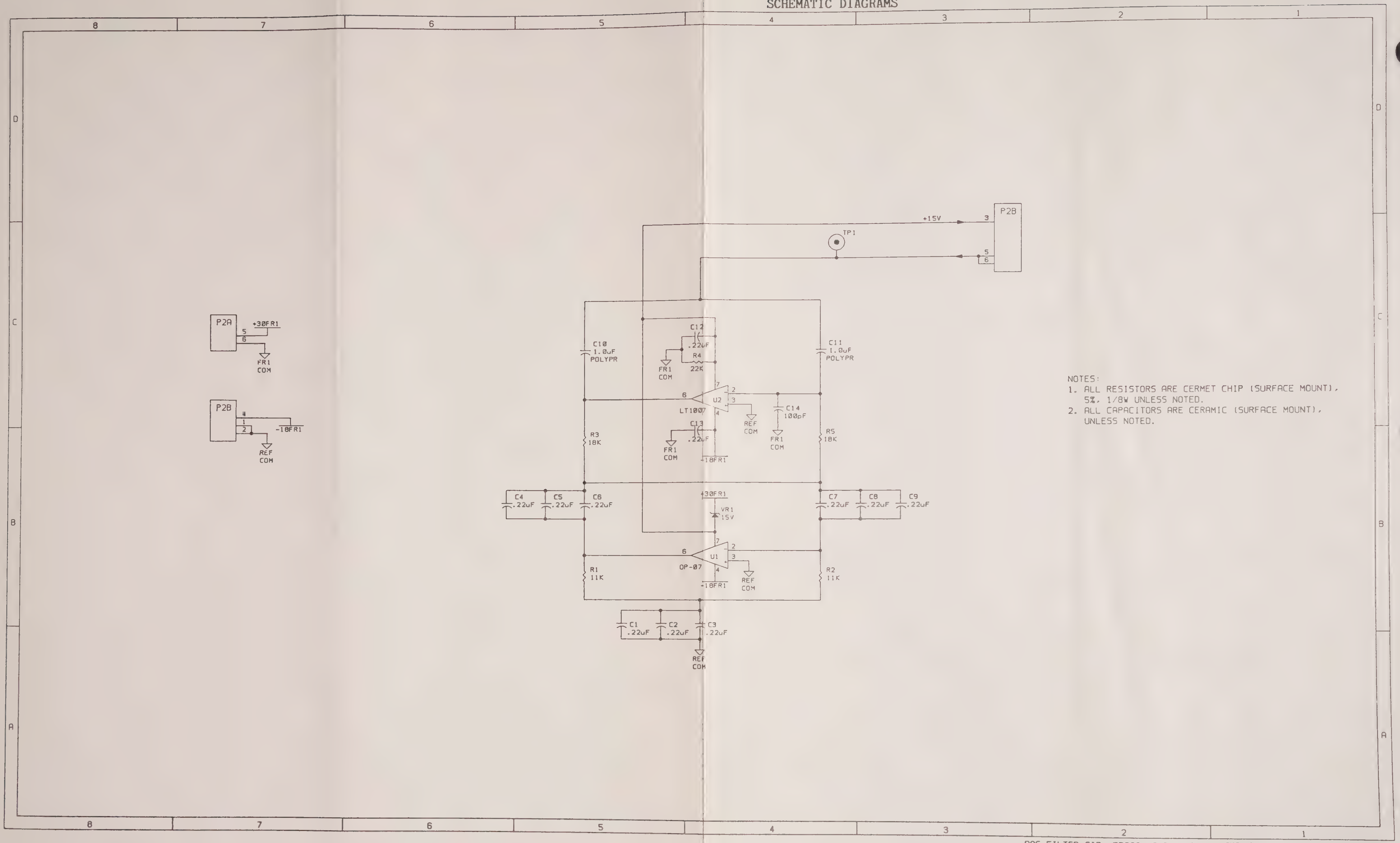

C12
VR1
C8
C9
R2
C1
C2
C3
TP1
R4
R3
C7
C10
U2
R5
C13
U1
R1
C4
C5
C6
C11
C14
P2A
P2B

Figure 7-12. A11A1 DAC Filter SIP PCA


8
7
6
5
4
3
2
1
D
C
B
A
P2A
+30FR1
5
6
FR1
COM
P2B
4
1
2
-18FR1
REF
COM
P2B
+15V
3
TP1
5
6
C10
1.0uF
POLYPR
C12
.22uF
R4
22K
FR1
COM
C11
1.0uF
POLYPR
6
U2
LT1007
2
3
7
4
C14
100pF
REF
COM
FR1
COM
C13
.22uF
FR1
COM
-18FR1
R3
18K
R5
18K
C4
.22uF
C5
.22uF
C6
.22uF
+30FR1
VR1
15V
C7
.22uF
C8
.22uF
C9
.22uF
6
U1
OP-07
2
3
7
4
REF
COM
-18FR1
R1
11K
R2
11K
C1
.22uF
C2
.22uF
C3
.22uF
REF
COM
DAC FILTER SIP 5700A-1043 1 OF 1 AUG.12.1988

NOTES:
1. ALL RESISTORS ARE CERMET CHIP (SURFACE MOUNT), 5%, 1/8W UNLESS NOTED.
2. ALL CAPACITORS ARE CERAMIC (SURFACE MOUNT), UNLESS NOTED.

Figure 7-12. A11A1 DAC Filter SIP PCA (cont)

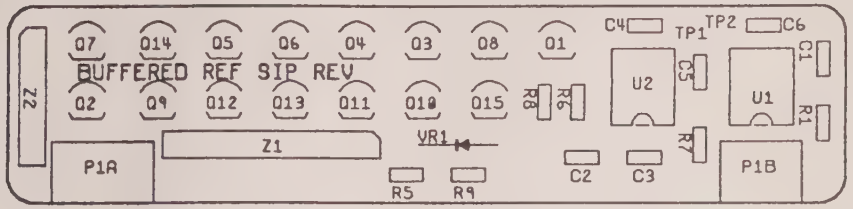
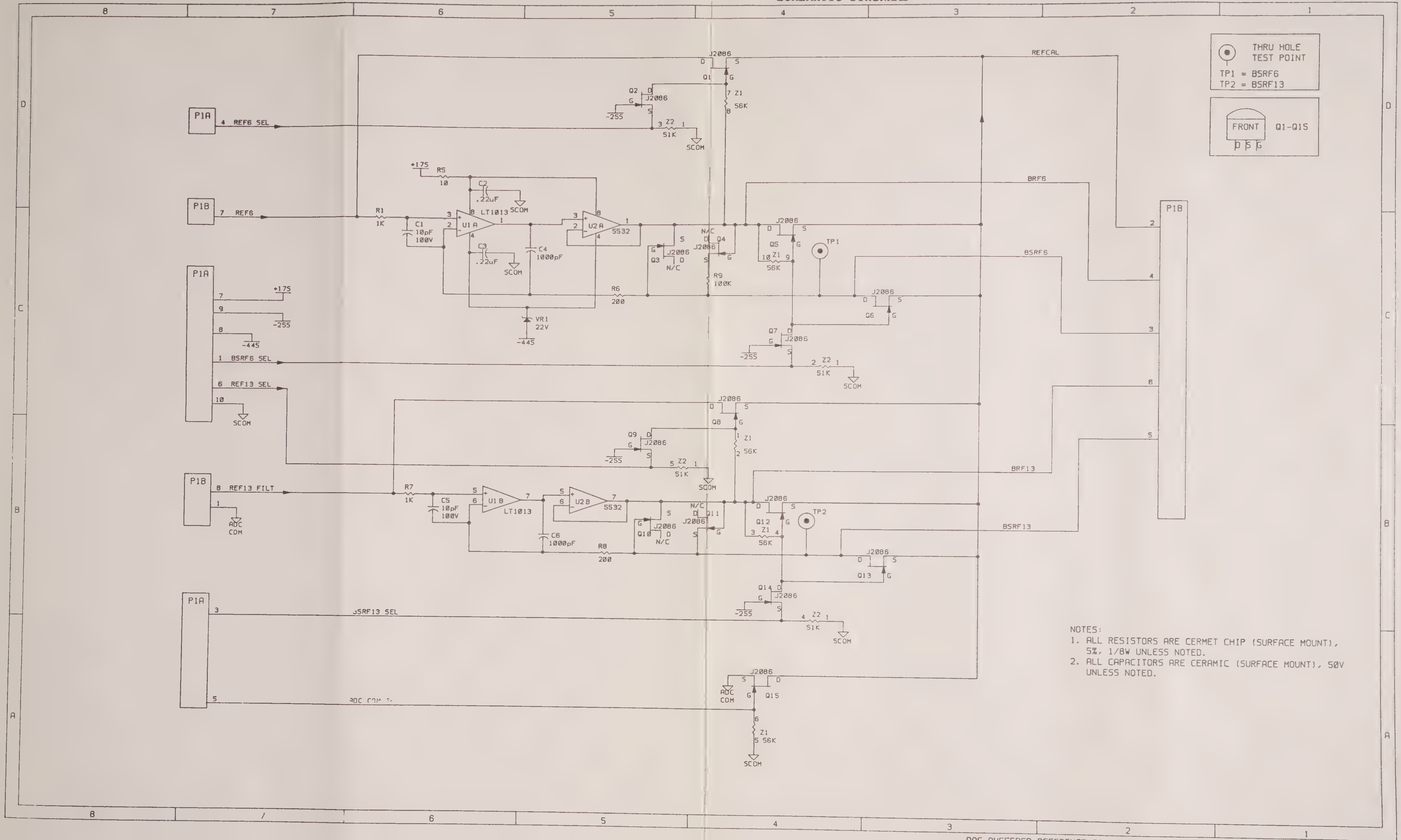

Q7
Q14
Q5
Q6
Q4
Q3
Q8
Q1
C4
TP1
TP2
C6
C1
BUFFERED REF SIP REV
C5
U2
U1
Z2
Q2
Q9
Q12
Q13
Q11
Q10
Q15
R8
R6
R1
Z1
VR1
R7
P1A
R5
R9
C2
C3
P1B

Figure 7-13. A11A2 DAC Buffered Reference SIP PCA


THRU HOLE TEST POINT
TP1 = BSRF6
TP2 = BSRF13
FRONT
Q1-Q15
D S G
P1A
4 REF6 SEL
P1B
7 REF6
P1A
7 +175
9 -255
8 -445
1 BSRF6 SEL
6 REF13 SEL
10 SCOM
P1B
8 REF13 FILT
1 ADC COM
P1A
3 BSRF13 SEL
5 ADC COM
J2086
Q1
Q2
Z1 56K
Z2 51K
-255
SCOM
+175
R5 10
C2 .22uF
R1 1K
C1 10pF 100V
U1A LT1013
C3 .22uF
C4 1000pF
U2A 5532
VR1 22V
-445
R6 200
Q3
Q4
N/C
R9 100K
Q5
TP1
Q6
Q7
REFCAL
BRF6
BSRF6
Q8
Q9
R7 1K
C5 10pF 100V
U1B LT1013
U2B 5532
C6 1000pF
R8 200
Q10
Q11
Q12
TP2
Q13
Q14
Q15
BRF13
BSRF13
P1B
2
4
3
6
5
DAC BUFFERED REFERENCE SIP 5700A-1044 1 OF 1 AUG.12,1988

NOTES:
1. ALL RESISTORS ARE CERMET CHIP (SURFACE MOUNT), 5%, 1/8W UNLESS NOTED.
2. ALL CAPACITORS ARE CERAMIC (SURFACE MOUNT), 50V UNLESS NOTED.

Figure 7-13. A11A2 DAC Buffered Reference SIP PCA (cont)

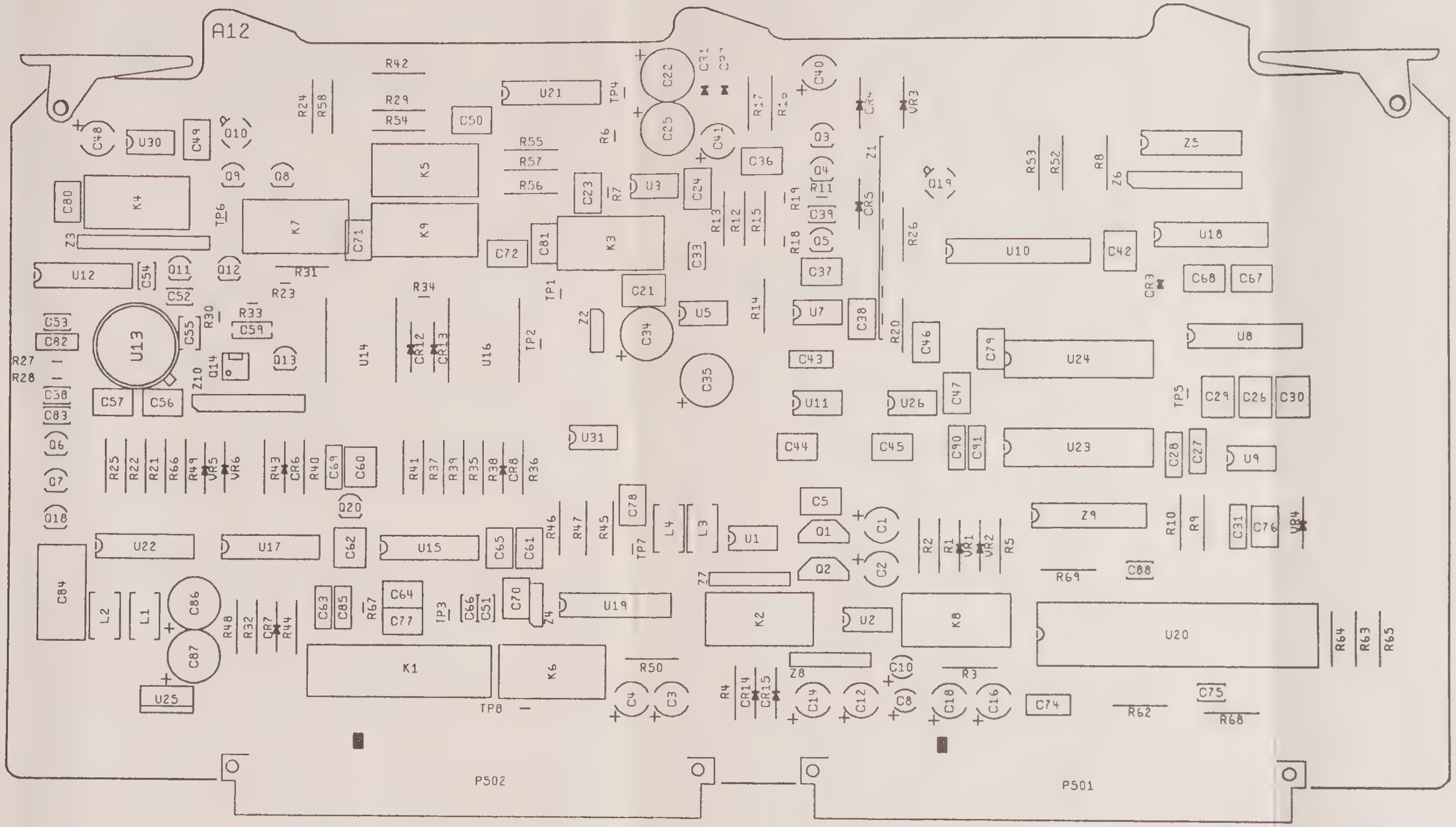

A12
R42
R29
R54
U21
TP4
C22
C25
C40
VR3
R24
R58
C50
R55
R57
R56
R6
C41
Z5
C48
U30
C49
Q10
Q9
Q8
K5
C23
R7
U3
C24
C36
Q3
Q4
R11
R19
C39
Q5
CR5
Z1
Q19
R53
R52
R8
Z6
C80
K4
TP6
K7
C71
K9
C72
C81
K3
R13
R12
R15
R18
R26
U10
C42
U18
Z3
U12
C54
Q11
Q12
R31
R23
C33
C21
C37
CR3
C68
C67
C52
R34
TP1
U5
R14
U7
C38
C53
C82
U13
C55
R30
R33
C59
U14
CR12
CR13
U16
TP2
Z2
C34
R20
C46
C79
U24
U8
R27
R28
Z10
Q14
Q13
C43
C35
C58
C83
C57
C56
U11
U26
C47
TP5
C29
C26
C30
U31
Q6
R25
R22
R21
R66
R49
VR5
VR6
R43
CR6
R40
C69
C60
R41
R37
R39
R35
R38
CR8
R36
C44
C45
C90
C91
U23
C28
C27
U9
Q7
Q20
C78
C5
Z9
Q18
R46
R47
R45
L4
L3
C1
R10
R9
C31
C76
VR4
U22
U17
C62
U15
C65
C61
TP7
U1
Q1
R2
R1
VR1
VR2
R5
Q2
C2
R69
C88
C84
Z7
L2
L1
C86
R48
R32
CR7
R44
C63
C85
R67
C64
C77
TP3
C66
C51
C70
Z4
U19
K2
U2
K8
U20
R64
R63
R65
C87
R50
Z8
C10
R3
K1
K6
R4
CR14
CR15
C14
C12
C8
C18
C16
C74
R62
C75
R68
U25
TP8
C4
C3
P502
P501

Figure 7-14. A12 Oscillator Control PCA (cont)

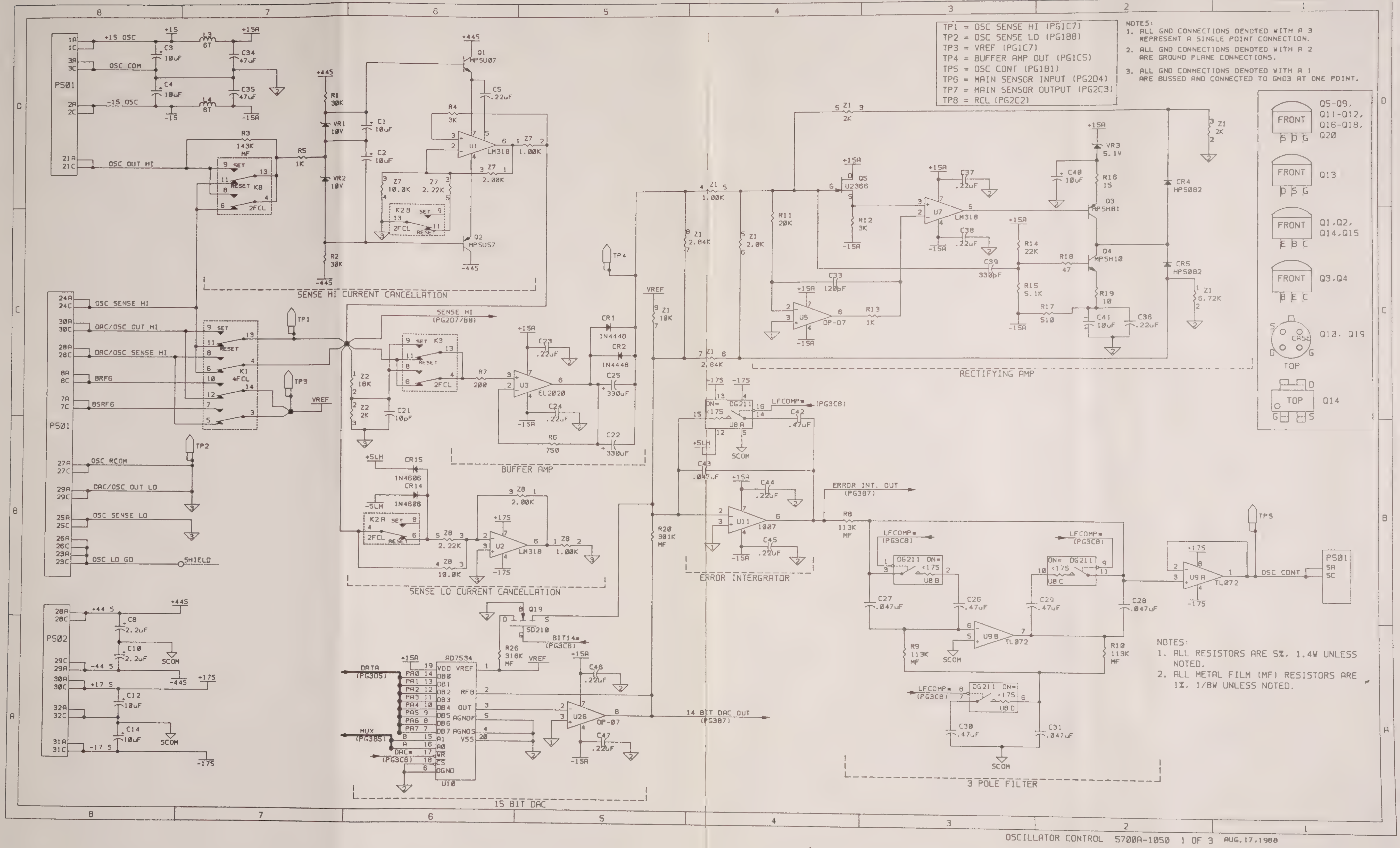

TP1 = OSC SENSE HI (PG1C7)
TP2 = OSC SENSE LO (PG1B8)
TP3 = VREF (PG1C7)
TP4 = BUFFER AMP OUT (PG1C5)
TP5 = OSC CONT (PG1B1)
TP6 = MAIN SENSOR INPUT (PG2D4)
TP7 = MAIN SENSOR OUTPUT (PG2C3)
TP8 = RCL (PG2C2)
NOTES:
1. ALL GND CONNECTIONS DENOTED WITH A 3 REPRESENT A SINGLE POINT CONNECTION.
2. ALL GND CONNECTIONS DENOTED WITH A 2 ARE GROUND PLANE CONNECTIONS.
3. ALL GND CONNECTIONS DENOTED WITH A 1 ARE BUSSED AND CONNECTED TO GND3 AT ONE POINT.
SENSE HI CURRENT CANCELLATION
BUFFER AMP
SENSE LO CURRENT CANCELLATION
15 BIT DAC
RECTIFYING AMP
ERROR INTERGRATOR
3 POLE FILTER
ERROR INT. OUT (PG3B7)
14 BIT DAC OUT (PG3B7)
OSC CONT
PS01
PS02
Q5-Q9, Q11-Q12, Q16-Q18, Q20
Q13
Q1,Q2, Q14,Q15
Q3,Q4
Q10, Q19
Q14
NOTES:
1. ALL RESISTORS ARE 5%, 1.4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.
OSCILLATOR CONTROL 5700A-1050 1 OF 3 AUG.17,1988

Figure 7-14. A12 Oscillator Control PCA (cont)

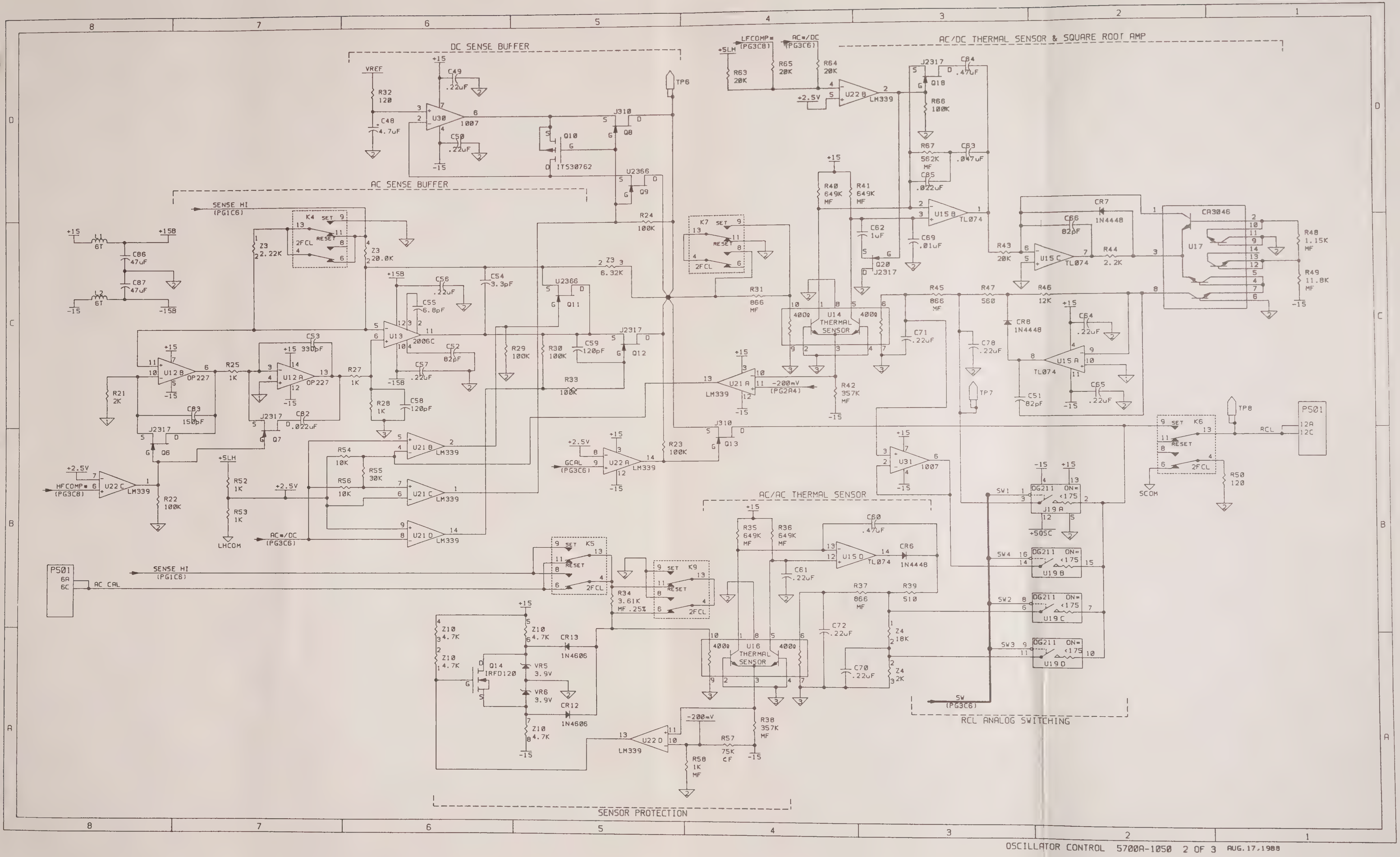
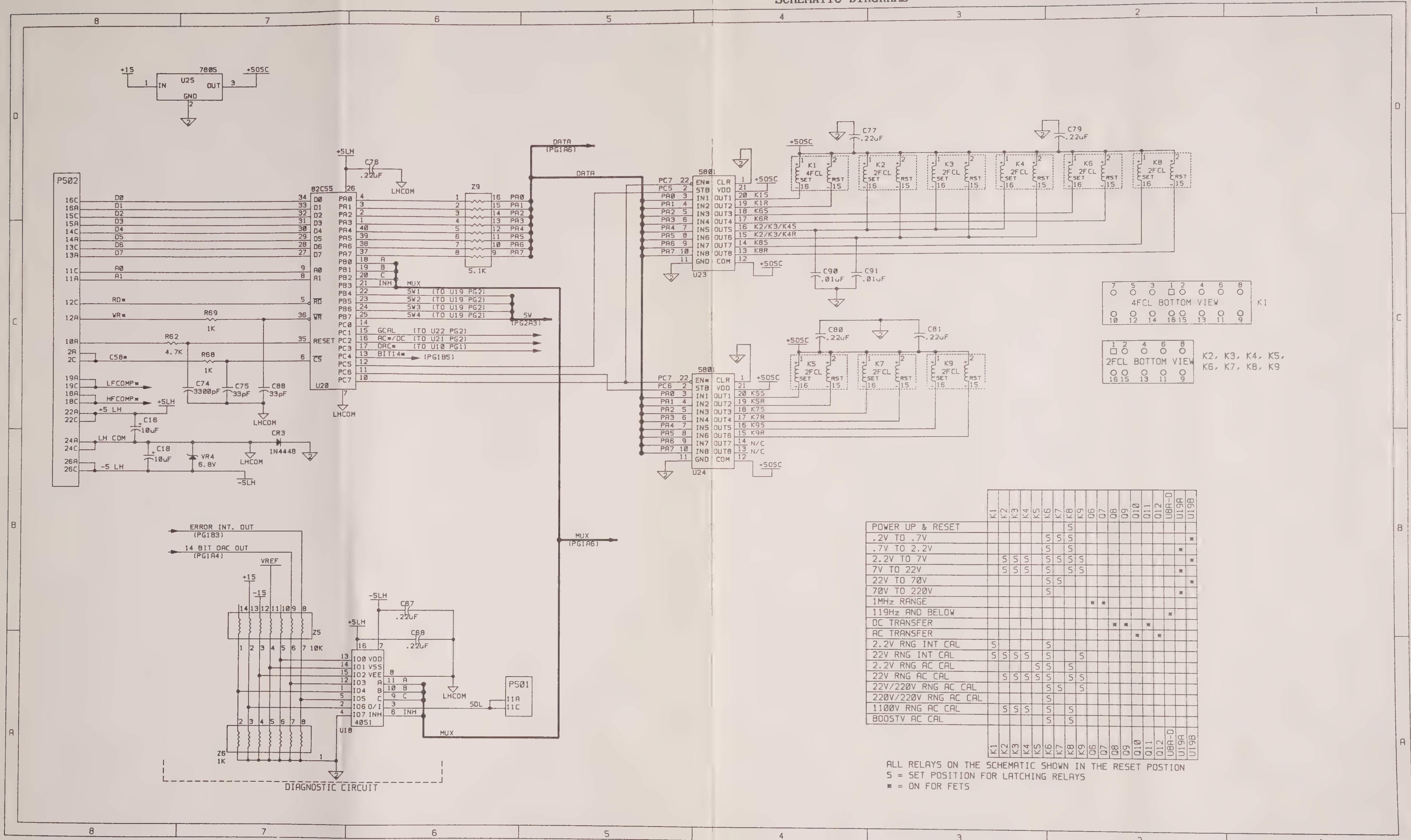

DC SENSE BUFFER
AC SENSE BUFFER
AC/DC THERMAL SENSOR & SQUARE ROOT AMP
AC/AC THERMAL SENSOR
SENSOR PROTECTION
RCL ANALOG SWITCHING
VREF
R32 120
C48 4.7uF
U30 1007
C49 .22uF
C50 .22uF
Q10
IT530762
J310 Q8
U2366 Q9
TP6
TP7
TP8
SENSE HI (PG1C6)
K4 SET RESET 2FCL
Z3 2.22K
Z3 20.0K
Z3 6.32K
R24 100K
+15 +15B -15 -15B
L1 6T
L2 6T
C86 47uF
C87 47uF
U12B OP227
U12A OP227
U13 2006C
R21 2K
R25 1K
R27 1K
C53 330pF
C83 150pF
C82 .022uF
J2317 Q6
J2317 Q7
C56 .22uF
C55 6.8pF
C54 3.3pF
C52 82pF
C57 .22uF
C58 120pF
R28 1K
R29 100K
R30 100K
C59 120pF
J2317 Q12
U2366 Q11
R33 100K
HFCOMP* (PG3C8)
U22C LM339
R22 100K
+5LH
R52 1K
R53 1K
LHCOM
R54 10K
R55 30K
R56 10K
U21B LM339
U21C LM339
U21D LM339
AC*/DC (PG3C6)
+2.5V
GCAL (PG3C6)
U22A LM339
R23 100K
J310 Q13
LFCOMP* (PG3C8)
AC*/DC (PG3C6)
R63 20K
R65 20K
R64 20K
U22B LM339
J2317 Q18
C84 .47uF
R66 100K
R67 562K MF
C83 .047uF
C85 .022uF
R40 649K MF
R41 649K MF
U15B TL074
C62 1uF
C69 .01uF
Q20 J2317
K7 SET RESET 2FCL
R31 866 MF
U14 THERMAL SENSOR 400Ω 400Ω
C71 .22uF
U21A LM339
-200mV (PG2A4)
R42 357K MF
CR7 1N4448
C66 82pF
U15C TL074
R43 20K
R44 2.2K
CA3046 U17
R48 1.15K MF
R49 11.8K MF
R45 866 MF
R47 560
R46 12K
CR8 1N4448
C64 .22uF
U15A TL074
C78 .22uF
C51 82pF
C65 .22uF
PS01 12A 12C
K6 SET RESET 2FCL
RCL
R50 120
SCOM
U31 1007
SW1 DG211 ON=<175 U19A
+5OSC
SW4 DG211 ON=<175 U19B
SW2 DG211 ON=<175 U19C
SW3 DG211 ON=<175 U19D
SW (PG3C6)
PS01 6A 6C
AC CAL
K5 SET RESET 2FCL
K9 SET RESET 2FCL
R34 3.61K MF .25%
R35 649K MF
R36 649K MF
C60 .47uF
U15D TL074
CR6 1N4448
C61 .22uF
R37 866 MF
R39 510
C72 .22uF
Z4 18K
Z4 2K
C70 .22uF
U16 THERMAL SENSOR 400Ω 400Ω
Z10 4.7K
Q14 IRFD120
VR5 3.9V
VR6 3.9V
CR13 1N4606
CR12 1N4606
U22D LM339
R38 357K MF
R57 75K CF
R58 1K MF
-200mV
A B C D
1 2 3 4 5 6 7 8
OSCILLATOR CONTROL 5700A-1050 2 OF 3 AUG.17,1988

Figure 7-14. A12 Oscillator Control PCA (cont


8
7
6
5
4
3
2
1
D
C
B
A
+15
7805
U25
IN
OUT
GND
+5OSC
P502
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
RD*
WR*
R69
1K
R62
4.7K
R68
1K
CS8*
LFCOMP*
HFCOMP*
+5LH
+5 LH
C16
10uF
LH COM
C18
10uF
VR4
6.8V
-5 LH
-5LH
CR3
1N4448
C74
3300pF
C75
33pF
C88
33pF
LHCOM
82C55
U20
RESET
C76
.22uF
Z9
5.1K
DATA
(PG1A6)
MUX
SW1 (TO U19 PG2)
SW2 (TO U19 PG2)
SW3 (TO U19 PG2)
SW4 (TO U19 PG2)
SV
(PG2A3)
GCAL (TO U22 PG2)
AC*/DC (TO U21 PG2)
DAC* (TO U10 PG1)
BIT14* (PG1B5)
5801
U23
U24
EN*
STB
CLR
VDD
GND
COM
K1S
K1R
K6S
K6R
K2/K3/K4S
K2/K3/K4R
K8S
K8R
K5S
K5R
K7S
K7R
K9S
K9R
N/C
C77
.22uF
C79
.22uF
C80
.22uF
C81
.22uF
C90
.01uF
C91
.01uF
K1
4FCL
K2
K3
K4
K5
K6
K7
K8
K9
2FCL
SET
RST
4FCL BOTTOM VIEW
2FCL BOTTOM VIEW
K2, K3, K4, K5, K6, K7, K8, K9
ERROR INT. OUT
(PG1B3)
14 BIT DAC OUT
(PG1A4)
VREF
+15
-15
Z5
10K
Z6
1K
-5LH
C67
.22uF
C68
.22uF
4051
U18
P501
11A
11C
SDL
INH
MUX
(PG1A6)
DIAGNOSTIC CIRCUIT

	K1	K2	K3	K4	K5	K6	K7	K8	K9	Q6	Q7	Q8	Q9	Q10	Q11	Q12	U8A-D	U19A	U19B
POWER UP & RESET								S											
.2V TO .7V						S	S	S											*
.7V TO 2.2V						S		S										*	
2.2V TO 7V		S	S	S		S	S	S	S										*
7V TO 22V		S	S	S		S		S	S									*	
22V TO 70V						S	S												*
70V TO 220V						S												*	
1MHz RANGE										*	*								
119Hz AND BELOW																	*		
DC TRANSFER												*	*		*				
AC TRANSFER														*		*			
2.2V RNG INT CAL	S					S													
22V RNG INT CAL	S	S	S	S		S			S										
2.2V RNG AC CAL					S	S		S											
22V RNG AC CAL		S	S	S	S	S		S	S										
22V/220V RNG AC CAL						S	S		S										
220V/220V RNG AC CAL						S													
1100V RNG AC CAL		S	S	S		S		S											
BOOSTV AC CAL						S		S											

ALL RELAYS ON THE SCHEMATIC SHOWN IN THE RESET POSTION
S = SET POSITION FOR LATCHING RELAYS
* = ON FOR FETS

OSCILLATOR CONTROL 5700A-1050 3 OF 3 JUL.12.1988

Figure 7-14. A12 Oscillator Control PCA (cont)

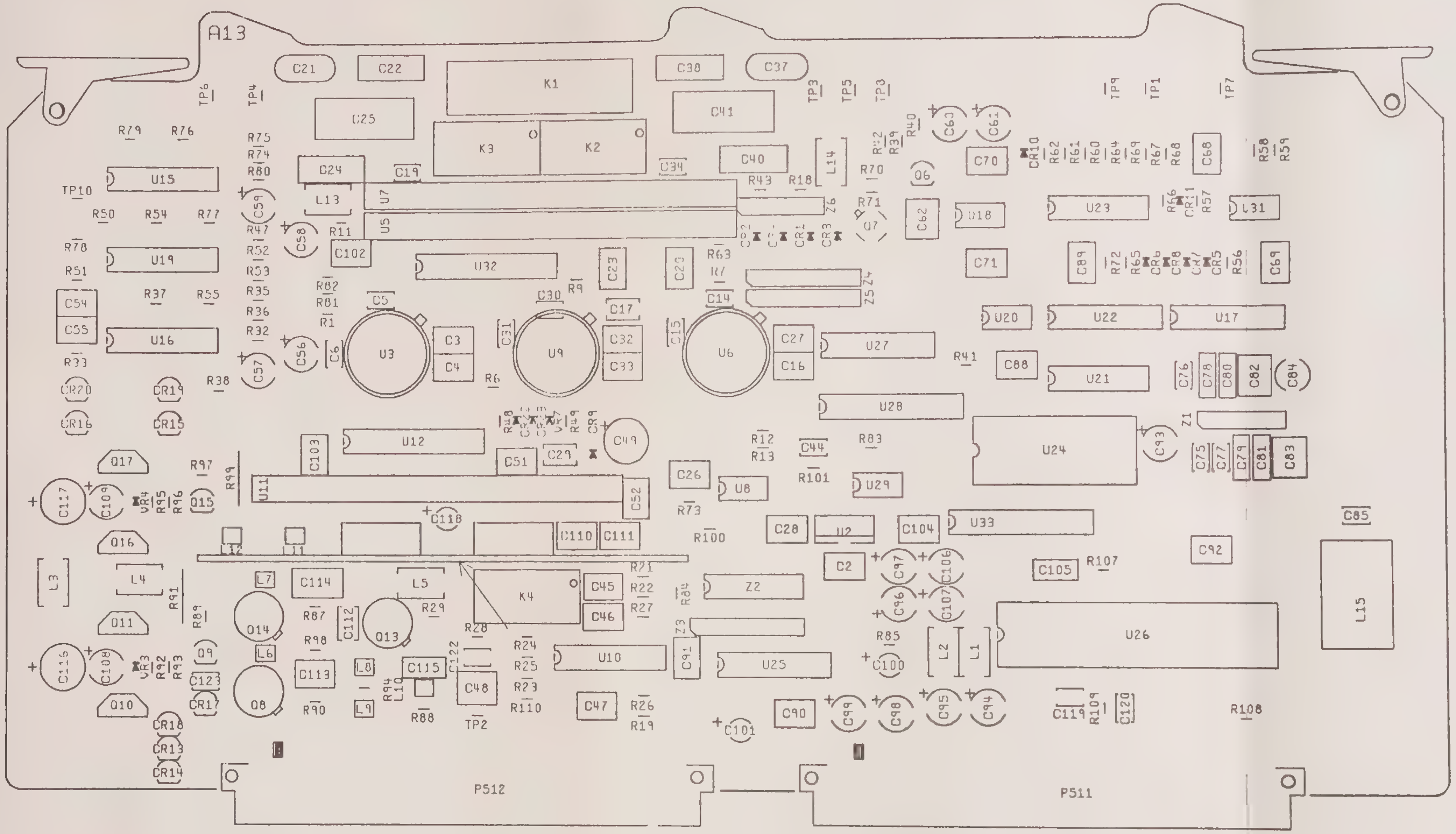

A13
C21
C22
K1
C38
C37
TP6
TP4
C25
TP3
TP5
TP3
TP9
TP1
TP7
K3
K2
C41
C40
R79
R76
R75
R74
R80
C24
C19
C34
R43
R18
L14
R70
C63
C61
C70
CR10
R62
R61
R60
R64
R69
R67
R68
C68
R58
R59
TP10
U15
U7
L13
Q6
R71
Q7
C62
U18
U23
R46
CR11
R57
L31
R50
R54
R77
C59
R47
C58
R11
U5
R52
C102
U32
C23
C20
R63
C71
C89
R72
R65
R56
C69
R78
U19
R51
R53
R35
R82
R81
R1
R9
R7
C30
C5
C17
C14
Z4
Z5
U20
U22
U17
C54
C55
R37
R55
R36
R32
U16
U3
C3
C4
C32
C33
U9
C31
C15
U6
C27
C16
U27
R41
C88
U21
C76
C78
C80
C82
C84
R33
R38
C56
C6
C57
R6
CR20
CR19
CR16
CR15
U28
Z1
U12
C49
C103
C51
C29
R12
R13
C44
R83
U24
C93
C75
C77
C79
C81
C83
Q17
R97
R99
U11
C52
C26
U8
R101
U29
C117
C109
VR4
R95
R96
Q15
C118
R73
R100
C28
U2
C104
U33
C85
Q16
C110
C111
R71
L12
L11
C2
C97
C106
C105
R107
C92
L3
L4
L7
C114
L5
K4
C45
R22
R84
Z2
L15
R91
R89
Q11
Q14
R87
C112
Q13
R29
C46
R27
C96
C107
U26
R98
R28
Z3
C116
C108
VR3
R92
R93
Q9
L6
C122
R24
U10
C91
R85
C100
L2
L1
U25
C123
C113
L8
R94
L10
C115
R25
C48
R23
Q10
CR17
Q8
R90
L9
R88
R110
C47
R26
C90
C99
C98
C95
C94
C119
R109
C120
R108
CR18
CR13
TP2
R19
C101
CR14
P512
P511

Figure 7-15. A13 Oscillator Output PCA

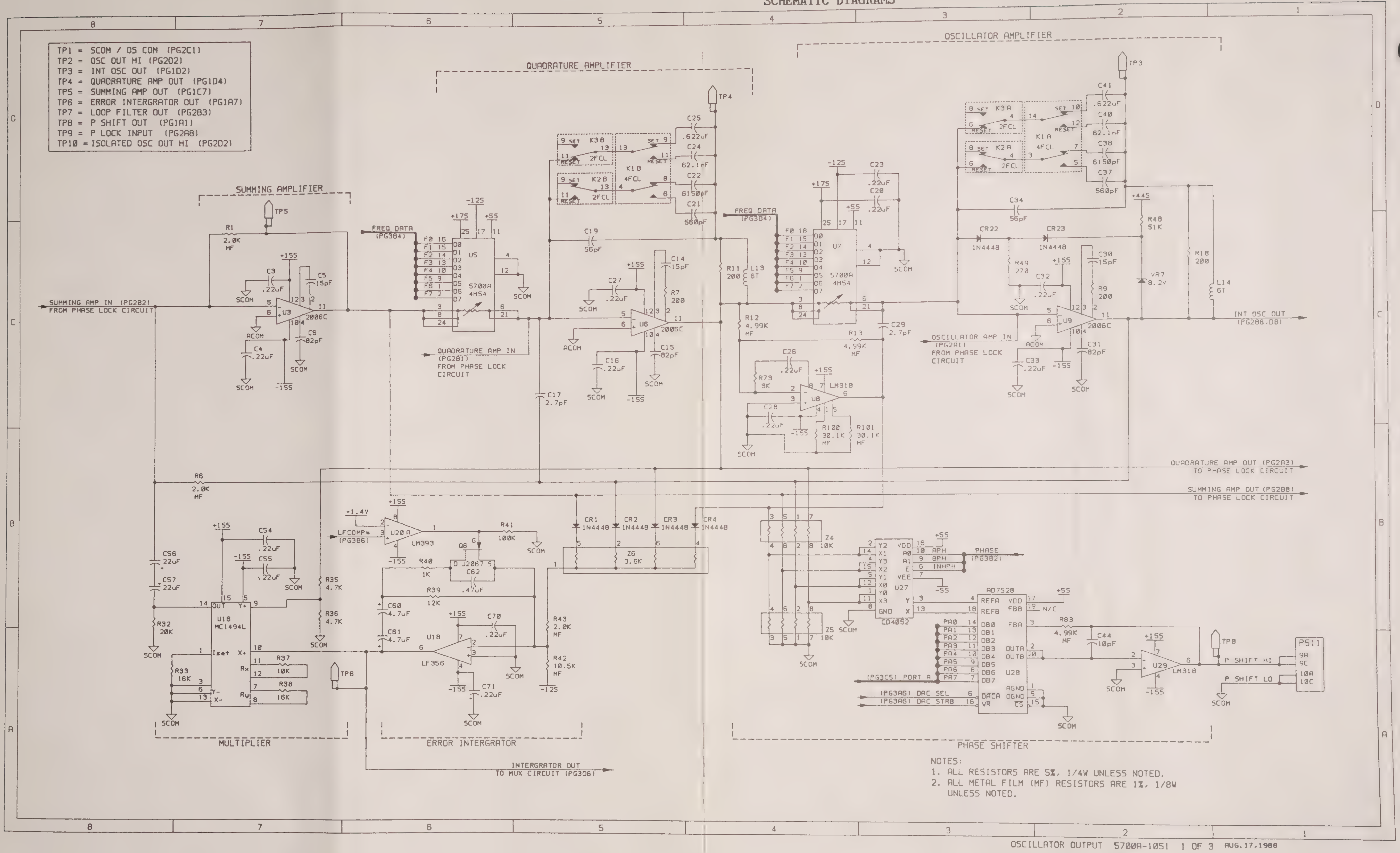

TP1 = SCOM / OS COM (PG2C1)
TP2 = OSC OUT HI (PG2D2)
TP3 = INT OSC OUT (PG1D2)
TP4 = QUADRATURE AMP OUT (PG1D4)
TP5 = SUMMING AMP OUT (PG1C7)
TP6 = ERROR INTERGRATOR OUT (PG1A7)
TP7 = LOOP FILTER OUT (PG2B3)
TP8 = P SHIFT OUT (PG1A1)
TP9 = P LOCK INPUT (PG2A8)
TP10 = ISOLATED OSC OUT HI (PG2D2)
SUMMING AMPLIFIER
QUADRATURE AMPLIFIER
OSCILLATOR AMPLIFIER
SUMMING AMP IN (PG2B2) FROM PHASE LOCK CIRCUIT
FREQ DATA (PG3B4)
QUADRATURE AMP IN (PG2B1) FROM PHASE LOCK CIRCUIT
OSCILLATOR AMP IN (PG2A1) FROM PHASE LOCK CIRCUIT
INT OSC OUT (PG2B8,D8)
QUADRATURE AMP OUT (PG2A3) TO PHASE LOCK CIRCUIT
SUMMING AMP OUT (PG2B8) TO PHASE LOCK CIRCUIT
LFCOMP* (PG3B6)
PHASE (PG3B2)
(PG3C5) PORT A
(PG3A6) DAC SEL
(PG3A6) DAC STRB
P SHIFT HI
P SHIFT LO
MULTIPLIER
ERROR INTERGRATOR
PHASE SHIFTER
INTERGRATOR OUT TO MUX CIRCUIT (PG3D6)
U3 2006C
U5 5700A 4H54
U6 2006C
U7 5700A 4H54
U8 LM318
U9 2006C
U16 MC1494L
U18 LF356
U20 A LM393
U27 CD4052
U28 AD7528
U29 LM318
NOTES:
1. ALL RESISTORS ARE 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.
OSCILLATOR OUTPUT 5700A-1051 1 OF 3 AUG.17,1988

Figure 7-15. A13 Oscillator Output PCA (cont)

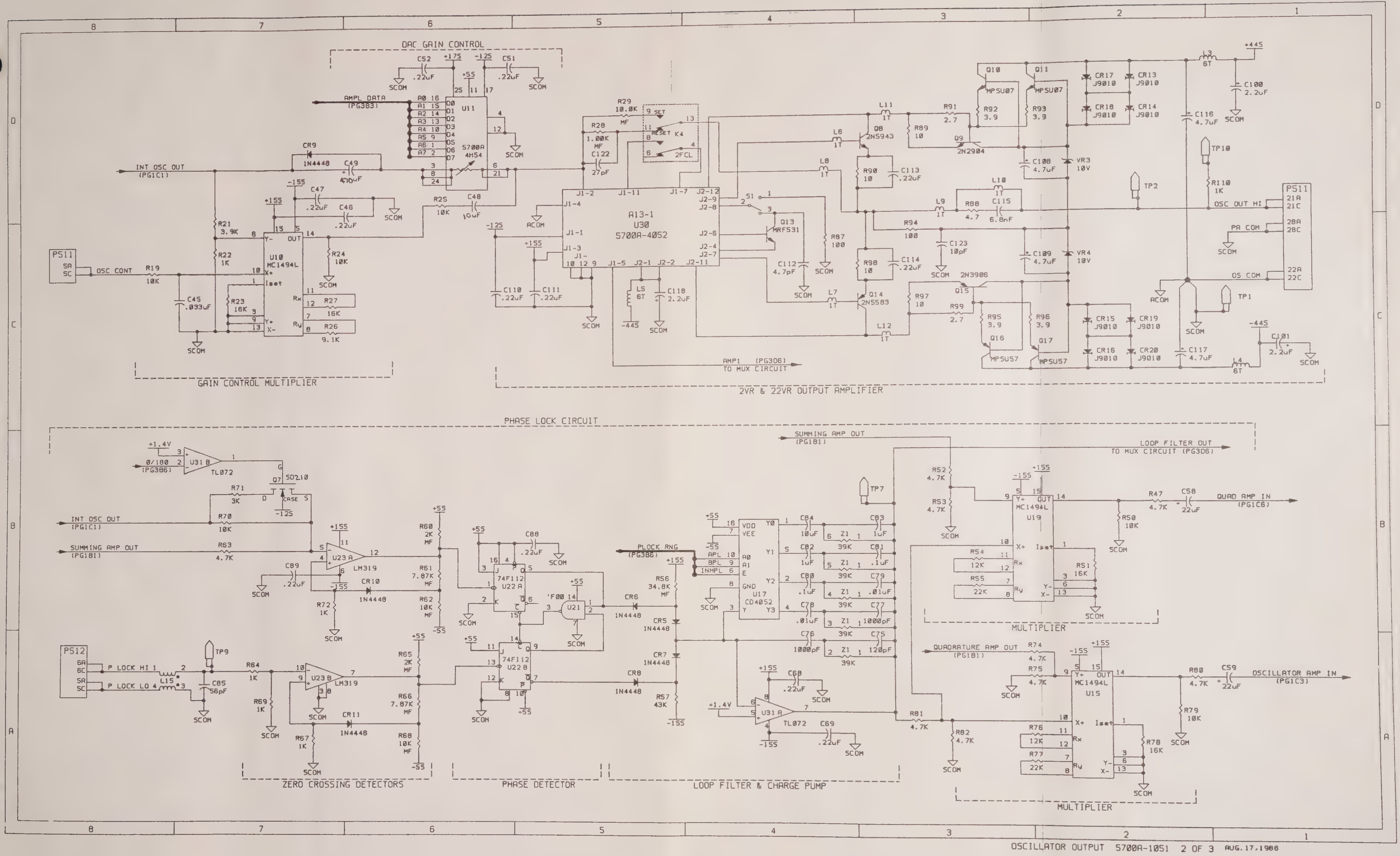
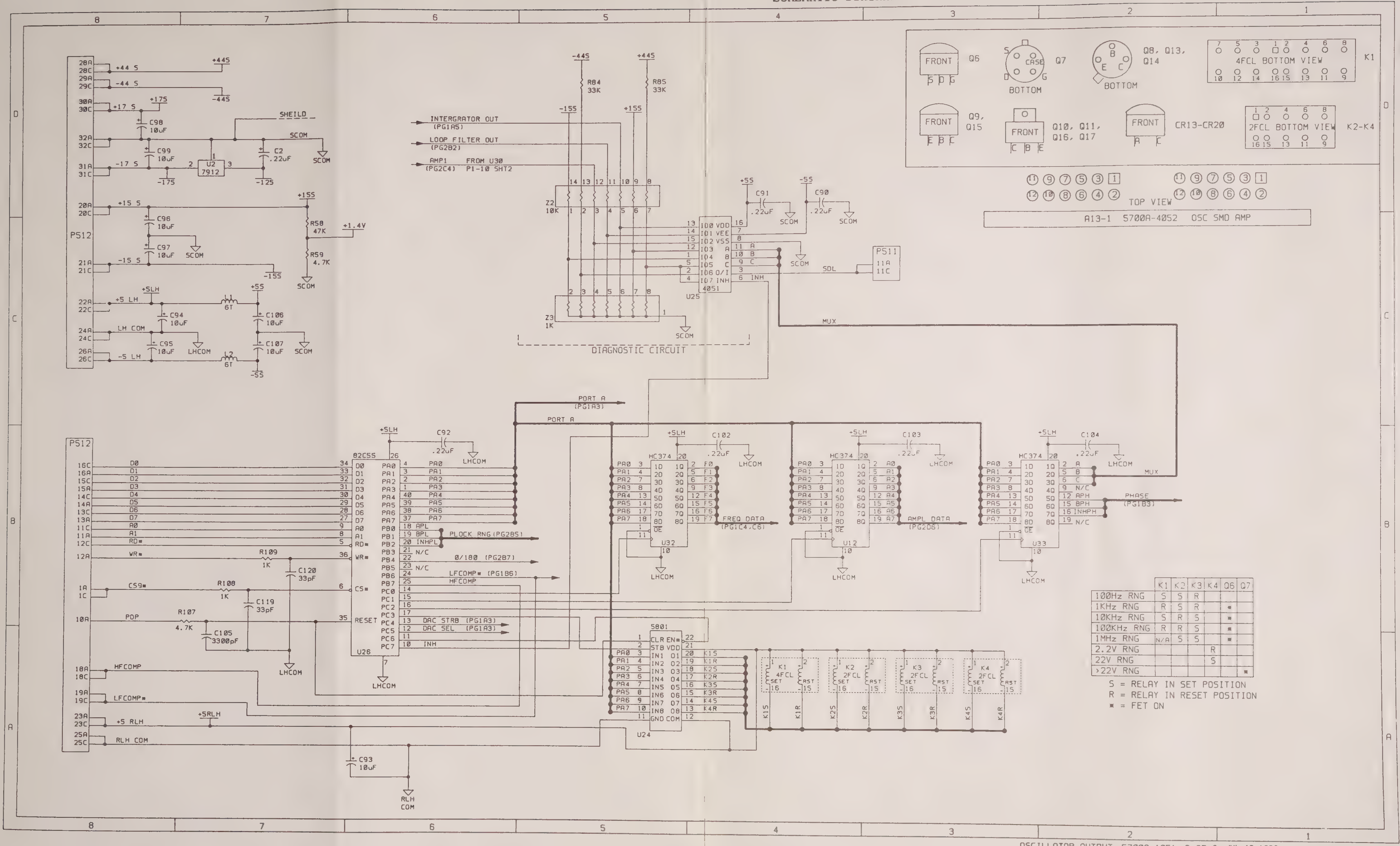

DAC GAIN CONTROL
AMPL DATA (PG3B3)
U11 5700A 4H54
INT OSC OUT (PG1C1)
CR9 1N4448
C49 470uF
C48 10uF
R25 10K
P511 5A 5C
OSC CONT
R19 10K
C45 .033uF
R21 3.9K
R22 1K
R23 18K
U10 MC1494L
R24 10K
R27 16K
R26 9.1K
GAIN CONTROL MULTIPLIER
R29 10.0K MF
R28 1.00K MF
C122 27pF
K4 2FCL
A13-1 U30 5700A-4052
AMP1 (PG3D6) TO MUX CIRCUIT
2VR & 22VR OUTPUT AMPLIFIER
Q8 2N5943
Q9 2N2904
Q10 MPSU07
Q11 MPSU07
Q13 MRF531
Q14 2N5583
Q15 2N3906
Q16 MPSU57
Q17 MPSU57
CR13–CR20 J9010
VR3 10V
VR4 10V
TP1
TP2
TP10
R110 1K
P511 21A 21C 28A 28C 22A 22C
OSC OUT HI
PA COM
OS COM
+44S
-44S
L3 6T
L4 6T
C100 2.2uF
C101 2.2uF
C116 4.7uF
C117 4.7uF
PHASE LOCK CIRCUIT
SUMMING AMP OUT (PG1B1)
LOOP FILTER OUT TO MUX CIRCUIT (PG3C6)
+1.4V
0/180 (PG3B6)
U31 B TL072
Q7 SD210
R71 3K
R70 10K
R63 4.7K
U23 A LM319
U23 B LM319
CR10 1N4448
CR11 1N4448
P512 6A 6C 5A 5C
P LOCK HI
P LOCK LO
L15
C85 56pF
TP9
R64 1K
ZERO CROSSING DETECTORS
74F112 U22 A
74F112 U22 B
'F00 U21
PHASE DETECTOR
PLOCK RNG (PG3B6)
U17 CD4052
CR5 1N4448
CR6 1N4448
CR7 1N4448
CR8 1N4448
R56 34.8K MF
R57 43K
U31 A TL072
LOOP FILTER & CHARGE PUMP
TP7
U19 MC1494L
U15 MC1494L
QUAD AMP IN (PG1C6)
QUADRATURE AMP OUT (PG1B1)
OSCILLATOR AMP IN (PG1C3)
R47 4.7K
C58 22uF
R80 4.7K
C59 22uF
MULTIPLIER
MULTIPLIER
OSCILLATOR OUTPUT 5700A-1051 2 OF 3 AUG.17.1988

Figure 7-15. A13 Oscillator Output PCA (cont)


P512
+44 S
-44 S
+17 S
-17 S
+15 S
-15 S
+5 LH
LH COM
-5 LH
SHEILD
SCOM
U2 7912
C2 .22uF
C98 10uF
C99 10uF
C96 10uF
C97 10uF
R58 47K
R59 4.7K
+1.4V
C94 10uF
C95 10uF
C106 10uF
C107 10uF
LHCOM
6T
INTERGRATOR OUT (PG1A5)
LOOP FILTER OUT (PG2B2)
AMP1 (PG2C4) FROM U30 P1-10 SHT2
R84 33K
R85 33K
Z2 10K
Z3 1K
DIAGNOSTIC CIRCUIT
U25 4051
C91 .22uF
C90 .22uF
P511 11A 11C
SDL
MUX
FRONT Q6
Q7 CASE BOTTOM
Q8, Q13, Q14 BOTTOM
4FCL BOTTOM VIEW K1
Q9, Q15
Q10, Q11, Q16, Q17
CR13-CR20
2FCL BOTTOM VIEW K2-K4
TOP VIEW
A13-1 5700A-4052 OSC SMD AMP
PORT A (PG1A3)
PORT A
82C55 U26
C92 .22uF
PLOCK RNG (PG2B5)
0/180 (PG2B7)
LFCOMP* (PG1B6)
HFCOMP
DAC STRB (PG1A3)
DAC SEL (PG1A3)
INH
R109 1K
C120 33pF
R108 1K
C119 33pF
R107 4.7K
C105 3300pF
HC374 U32
C102 .22uF
FREQ DATA (PG1C4,C6)
HC374 U12
C103 .22uF
AMPL DATA (PG2D6)
HC374 U33
C104 .22uF
PHASE (PS1B3)
5801 U24
K1 4FCL
K2 2FCL
K3 2FCL
K4 2FCL
+5 RLH
RLH COM
+SRLH
C93 10uF
RLH COM

	K1	K2	K3	K4	Q6	Q7
100Hz RNG	S	S	R			
1KHz RNG	R	S	R		*	
10KHz RNG	S	R	S		*	
100KHz RNG	R	R	S		*	
1MHz RNG	N/A	S	S		*	
2.2V RNG				R		
22V RNG				S		
>22V RNG						*

S = RELAY IN SET POSITION
R = RELAY IN RESET POSITION
* = FET ON

OSCILLATOR OUTPUT 5700A-1051 3 OF 3 JUL.12,1988

Figure 7-15. A13 Oscillator Output PCA (cont)

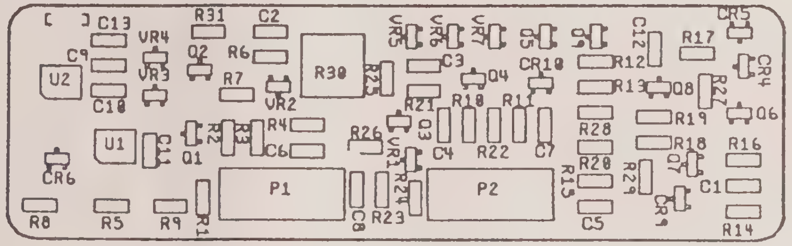
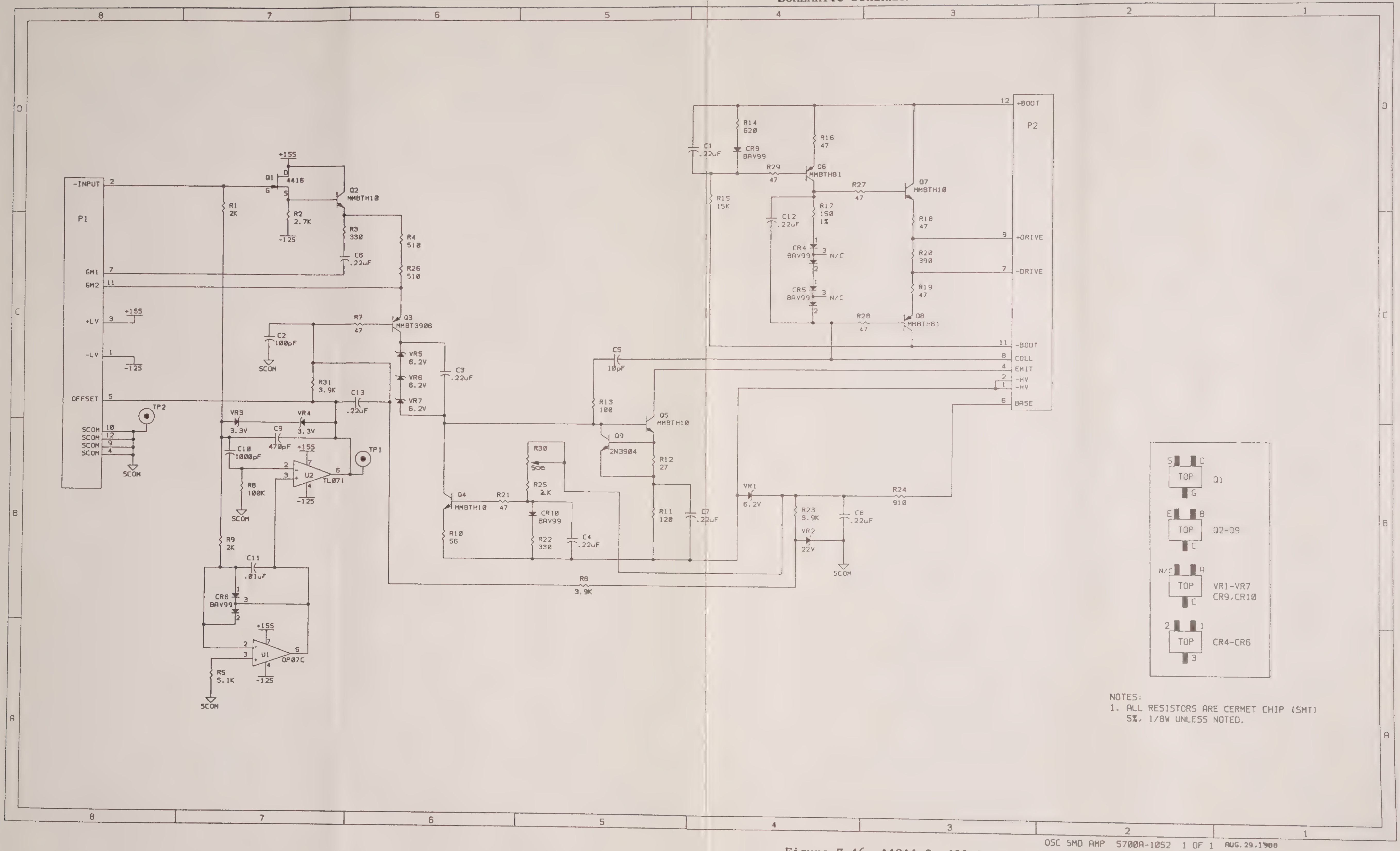

C13
R31
C2
VR4
C9
Q2
R6
R30
R25
VR5
VR6
VR7
Q5
Q9
C12
R17
CR5
U2
VR3
R7
VR2
C3
Q4
CR10
R12
R13
Q8
R27
CR4
C10
R21
R10
R11
Q6
R19
U1
C11
Q1
R2
R3
R4
C6
R26
Q3
R28
R18
R16
VR1
C4
R22
C7
R20
Q7
CR6
P1
P2
R24
R15
R29
C1
CR9
R8
R5
R9
R1
C8
R23
C5
R14

Figure 7-16. A13A1 Oscillator Wideband SMD PCA (cont)


P1
-INPUT 2
GM1 7
GM2 11
+LV 3
-LV 1
OFFSET 5
SCOM 10
SCOM 12
SCOM 9
SCOM 4
+15S
-12S
TP1
TP2
Q1 4416
Q2 MMBTH10
Q3 MMBT3906
Q4 MMBTH10
Q5 MMBTH10
Q6 MMBTH81
Q7 MMBTH10
Q8 MMBTH81
Q9 2N3904
R1 2K
R2 2.7K
R3 330
R4 510
R5 5.1K
R6 3.9K
R7 47
R8 100K
R9 2K
R10 56
R11 120
R12 27
R13 100
R14 620
R15 15K
R16 47
R17 150 1%
R18 47
R19 47
R20 390
R21 47
R22 330
R23 3.9K
R24 910
R25 2K
R26 510
R27 47
R28 47
R29 47
R30 500
R31 3.9K
C1 .22uF
C2 100pF
C3 .22uF
C4 .22uF
C5 10pF
C6 .22uF
C7 .22uF
C8 .22uF
C9 470pF
C10 1000pF
C11 .01uF
C12 .22uF
C13 .22uF
CR4 BAV99
CR5 BAV99
CR6 BAV99
CR9 BAV99
CR10 BAV99
N/C
VR1 6.2V
VR2 22V
VR3 3.3V
VR4 3.3V
VR5 6.2V
VR6 6.2V
VR7 6.2V
U1 OP07C
U2 TL071
SCOM
P2
12 +BOOT
9 +DRIVE
7 -DRIVE
11 -BOOT
8 COLL
4 EMIT
2 -HV
1 -HV
6 BASE
S D TOP G Q1
E B TOP C Q2-Q9
N/C A TOP C VR1-VR7 CR9,CR10
2 1 TOP 3 CR4-CR6
OSC SMD AMP 5700A-1052 1 OF 1 AUG.29.1988

NOTES:
1. ALL RESISTORS ARE CERMET CHIP (SMT) 5%, 1/8W UNLESS NOTED.

Figure 7-16. A13A1 Oscillator Wideband SMD PCA (cont)

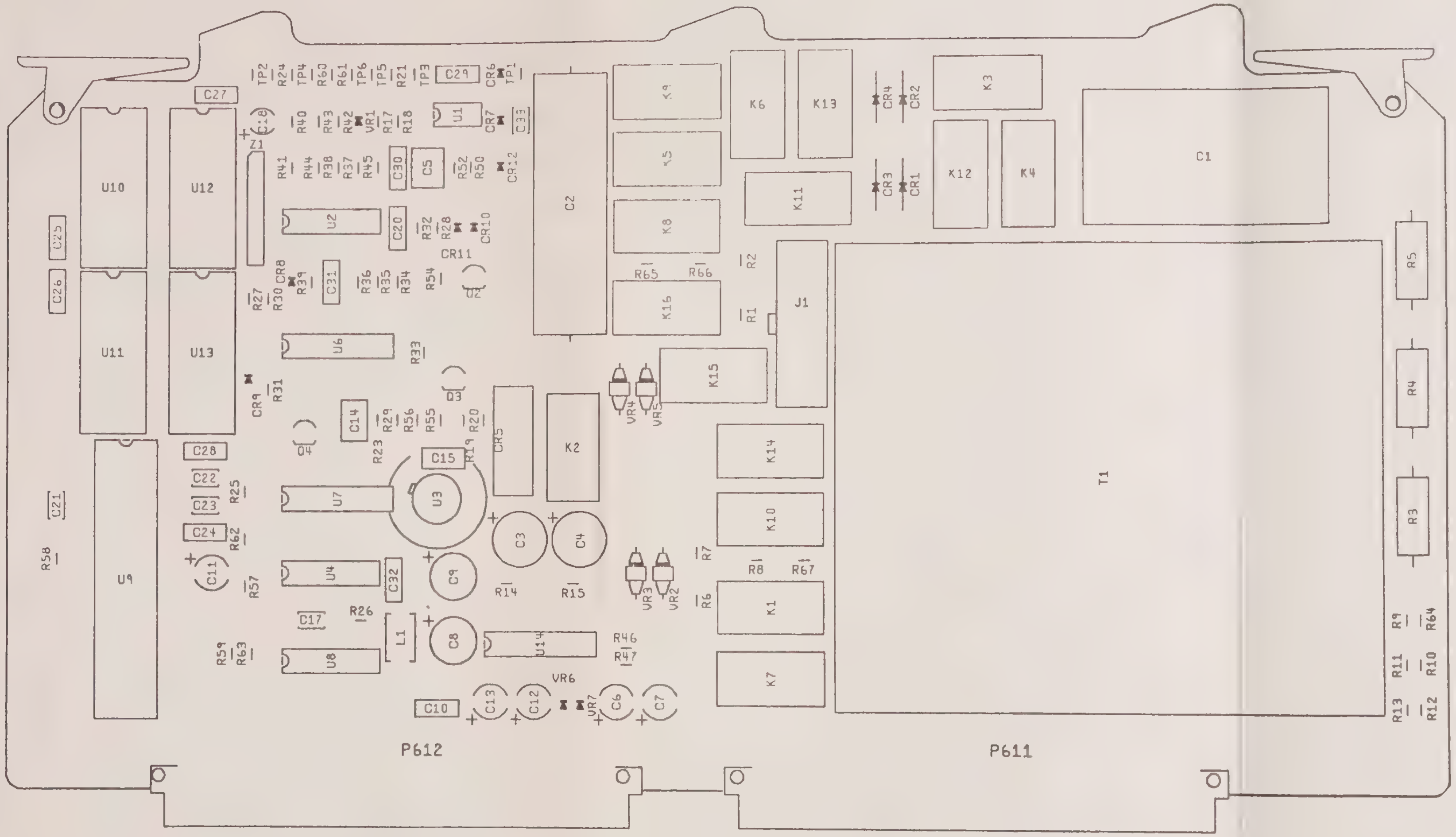
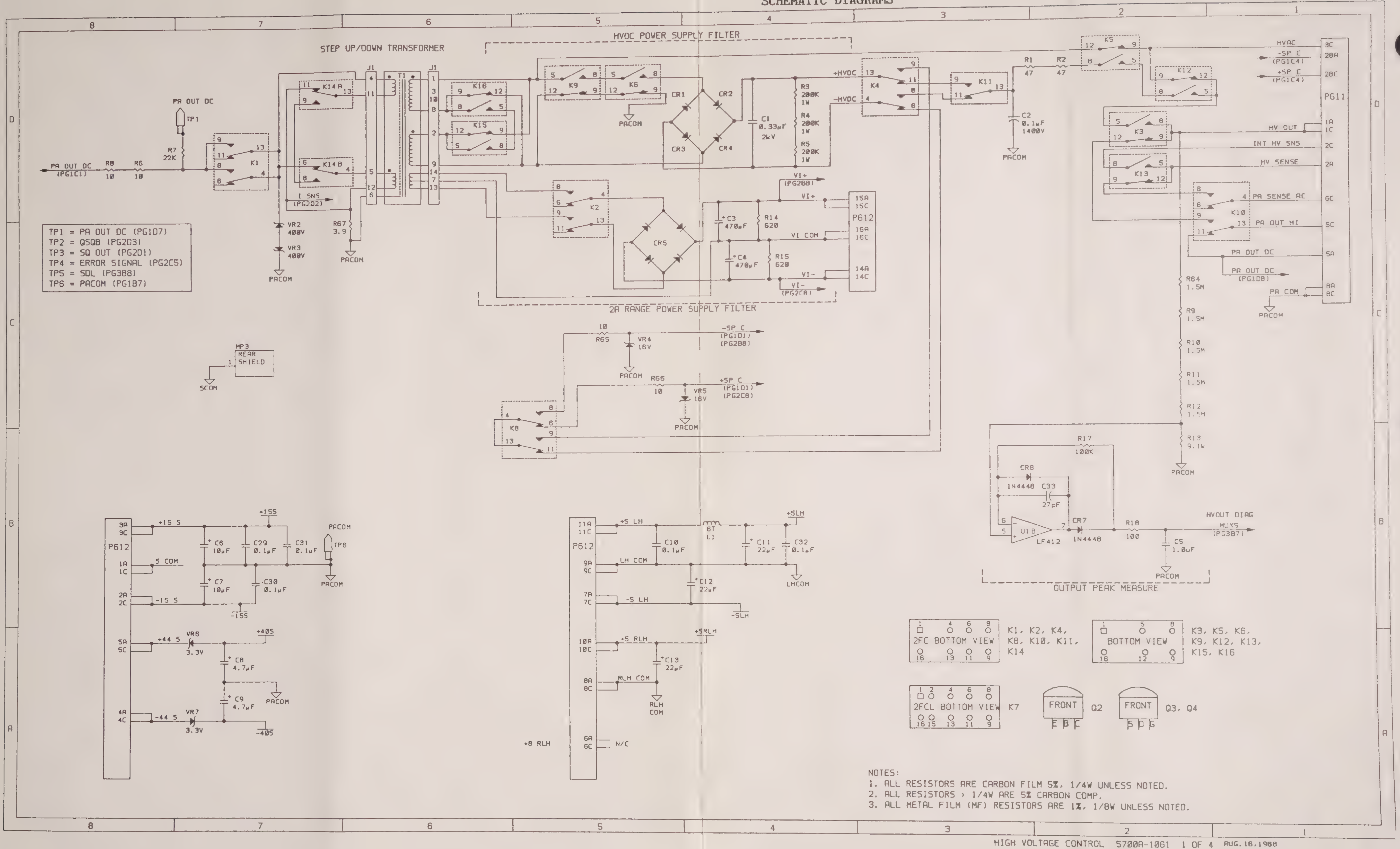

TP2
R24
TP4
R60
R61
TP6
TP5
R21
TP3
C29
CR6
TP1
C27
C18
R40
R43
R42
VR1
R17
R18
U1
CR7
C33
Z1
R41
R44
R38
R37
R45
C30
C5
R52
R50
CR12
U10
U12
C2
K9
K5
K8
K6
K13
CR4
CR2
CR3
CR1
K3
K12
K4
K11
C1
C25
U2
C20
R32
R28
CR10
CR11
C26
R27
R30
CR8
R39
C31
R36
R35
R34
R54
Q2
R65
R66
R2
K16
R1
J1
R5
U11
U13
U6
R33
CR9
R31
Q3
VR4
VR5
K15
R4
C14
R29
R56
R55
R20
Q4
R23
R19
CR5
K2
K14
C28
C15
C22
R25
U7
U3
C23
C3
C4
K10
T1
R3
C21
C24
R62
R7
R58
C11
U9
R57
U4
C32
C9
R14
R15
VR3
VR2
R8
R67
R6
K1
C17
R26
L1
C8
U14
R46
R47
R59
R63
U8
R9
R64
R11
R10
K7
VR6
C10
C13
C12
VR7
C6
C7
R13
R12
P612
P611

Figure 7-17. A14 High Voltage Control PCA

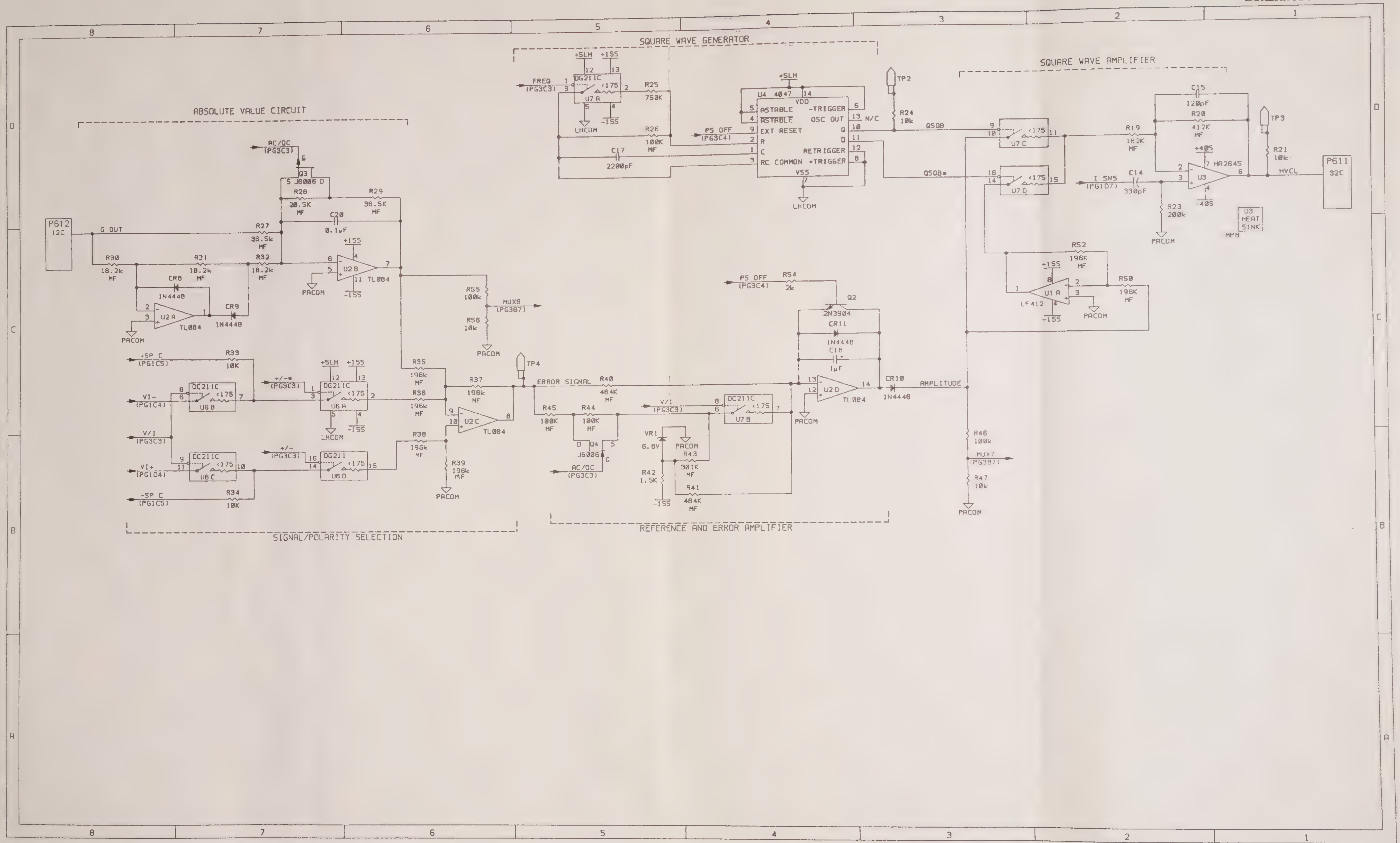

8
7
6
5
4
3
2
1
D
C
B
A
STEP UP/DOWN TRANSFORMER
HVDC POWER SUPPLY FILTER
PA OUT DC
TP1
R7
22K
PA OUT DC
(PG1C1)
R8
10
R6
10
K1
K14A
K14B
J1
T1
I SNS
(PG2D2)
R67
3.9
VR2
400V
VR3
400V
PACOM
K16
K15
K9
K6
CR1
CR2
CR3
CR4
C1
0.33μF
2kV
R3
200K
1W
R4
200K
1W
R5
200K
1W
+HVDC
-HVDC
K4
K11
R1
47
R2
47
C2
0.1μF
1400V
K5
K12
K3
K13
K10
HVAC
-SP C
(PG1C4)
+SP C
(PG1C4)
HV OUT
INT HV SNS
HV SENSE
PA SENSE AC
PA OUT HI
PA OUT DC
PA OUT DC
(PG1D8)
PA COM
P611
K2
CR5
C3
470μF
R14
620
C4
470μF
R15
620
VI+
(PG2B8)
VI COM
VI-
(PG2C8)
P612
2A RANGE POWER SUPPLY FILTER
R65
10
VR4
16V
-SP C
(PG1D1)
(PG2B8)
R66
10
VR5
16V
+SP C
(PG1D1)
(PG2C8)
K8
MP3
REAR
SHIELD
SCOM
R64
1.5M
R9
1.5M
R10
1.5M
R11
1.5M
R12
1.5M
R13
9.1k
R17
100K
CR6
1N4448
C33
27pF
U1B
LF412
CR7
1N4448
R18
100
C5
1.0μF
HVOUT DIAG
MUXS
(PG3B7)
OUTPUT PEAK MEASURE
P612
+15 S
+15S
C6
10μF
C29
0.1μF
C31
0.1μF
TP6
S COM
C7
10μF
C30
0.1μF
-15 S
-15S
+44 S
VR6
3.3V
+40S
C8
4.7μF
C9
4.7μF
-44 S
VR7
3.3V
-40S
+5 LH
C10
0.1μF
L1
6T
C11
22μF
C32
0.1μF
+5LH
LH COM
LHCOM
C12
22μF
-5 LH
-5LH
+5 RLH
+5RLH
C13
22μF
RLH COM
RLH
COM
+8 RLH
N/C
2FC BOTTOM VIEW
K1, K2, K4, K8, K10, K11, K14
BOTTOM VIEW
K3, K5, K6, K9, K12, K13, K15, K16
2FCL BOTTOM VIEW
K7
FRONT
Q2
FRONT
Q3, Q4

TP1 = PA OUT DC (PG1D7)
TP2 = QSQB (PG2D3)
TP3 = SQ OUT (PG2D1)
TP4 = ERROR SIGNAL (PG2C5)
TP5 = SDL (PG3B8)
TP6 = PACOM (PG1B7)

NOTES:
1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL RESISTORS › 1/4W ARE 5% CARBON COMP.
3. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

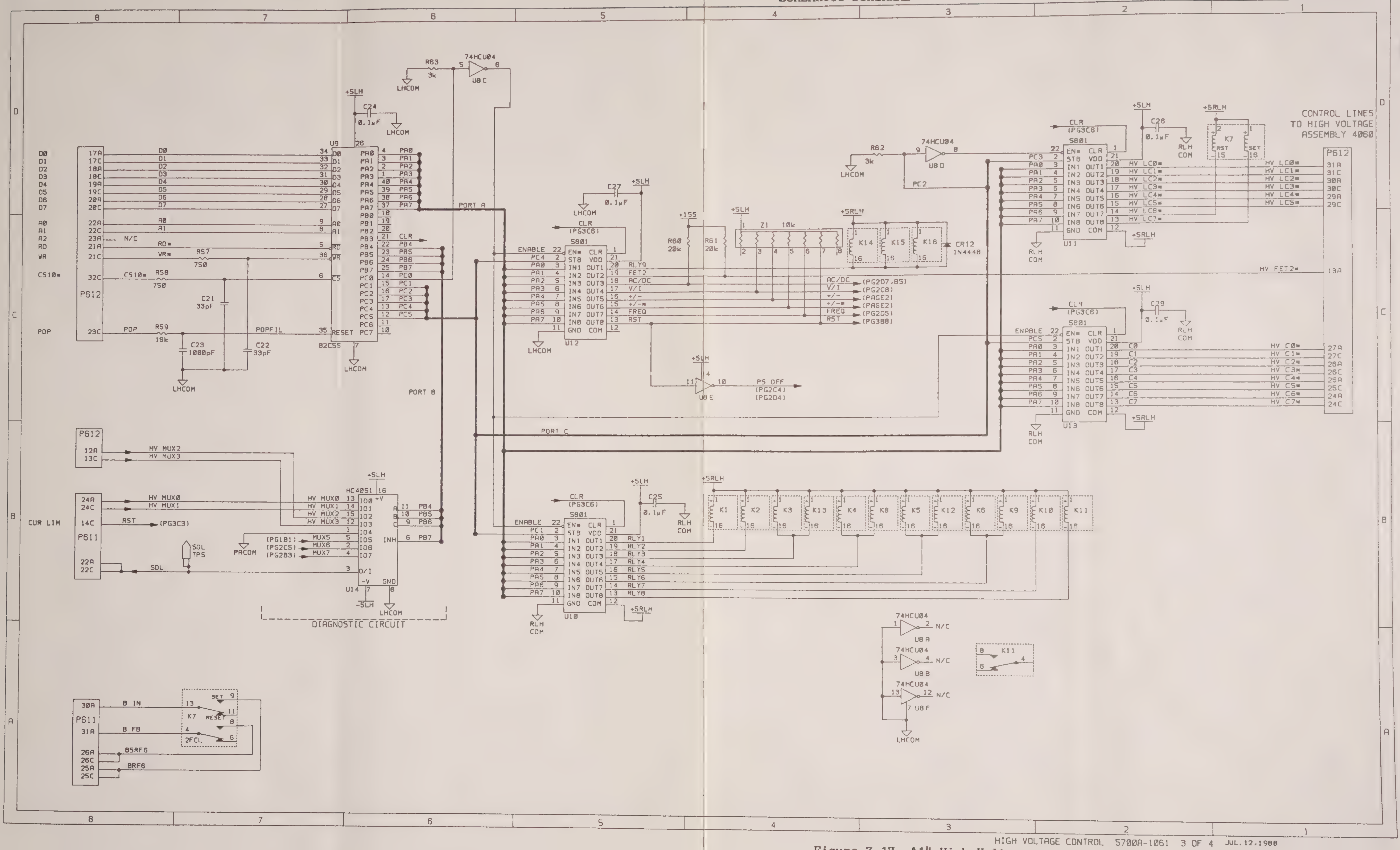
HIGH VOLTAGE CONTROL 5700A-1061 1 OF 4 AUG.16.1988

Figure 7-17. A14 High Voltage Control PCA (cont)


ABSOLUTE VALUE CIRCUIT
SQUARE WAVE GENERATOR
SQUARE WAVE AMPLIFIER
SIGNAL/POLARITY SELECTION
REFERENCE AND ERROR AMPLIFIER
P612 12C
G OUT
AC/DC (PG3C3)
Q3 J6006
R27 36.5k MF
R28 20.5K MF
R29 36.5K MF
C20 0.1µF
R30 18.2k MF
R31 18.2k MF
R32 18.2k MF
CR8 1N4448
CR9 1N4448
U2A TL084
U2B TL084
+15S
-15S
PACOM
R55 100k
R56 10k
MUX6 (PG3B7)
+SP C (PG1C5)
R33 10K
VI- (PG1C4)
V/I (PG3C3)
VI+ (PG1D4)
-SP C (PG1C5)
R34 10K
DG211C U6B
DG211C U6C
DG211C U6A
DG211 U6D
+/-= (PG3C3)
+/- (PG3C3)
+5LH
LHCOM
R35 196k MF
R36 196k MF
R37 196k MF
R38 196k MF
R39 196k MF
U2C TL084
TP4
ERROR SIGNAL
R40 464K MF
R45 100K MF
R44 100K MF
Q4 J6006
VR1 6.8V
R42 1.5K
R43 301K MF
R41 464K MF
DG211C U7B
U2D TL084
CR10 1N4448
AMPLITUDE
PS OFF (PG3C4)
R54 2k
Q2 2N3904
CR11 1N4448
C18 1µF
R46 100k
MUX7 (PG3B7)
R47 10k
FREQ (PG3C3)
DG211C U7A
R25 750K
R26 100K MF
C17 2200pF
U4 4047
VDD
ASTABLE
ASTABLE
EXT RESET
R
C
RC COMMON
-TRIGGER
OSC OUT
Q
Q̄
RETRIGGER
+TRIGGER
VSS
N/C
TP2
R24 10k
QSOB
QSOB=
U7C
U7D
C15 120pF
R20 412K MF
R19 162K MF
+40S
-40S
U3 HA2645
TP3
R21 10k
HVCL
P611 32C
I SNS (PG1D7)
C14 330pF
R23 200k
U3 HEAT SINK MP8
R52 196K MF
R50 196K MF
U1A LF412
8
7
6
5
4
3
2
1
D
C
B
A

HIGH VOLTAGE CONTROL 5700A-1061 2 OF 4 AUG.16.1988

Figure 7-17. A14 High Voltage Control PCA (cont)



P612
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
RD
WR
CS10*
POP
N/C
RD*
WR*
R57 750
R58 750
R59 16k
C21 33pF
C22 33pF
C23 1000pF
POPFIL
LHCOM
U9
82C55
RESET
PORT A
PORT B
PORT C
74HCU04
R63 3k
U8 C
+5LH
C24 0.1µF
C27 0.1µF
CLR (PG3C6)
ENABLE
5801
U12
RLY9
FET2
AC/DC
V/I
+/-
+/-*
FREQ
RST
(PG2D7,B5)
(PG2C8)
(PAGE2)
(PG2D5)
(PG3B8)
+15S
R60 20k
R61 20k
Z1 10k
+5RLH
K14
K15
K16
CR12 1N4448
U8 E
PS OFF (PG2C4) (PG2D4)
R62 3k
U8 D
PC2
U11
RLH COM
C26 0.1µF
K7
RST
SET
CONTROL LINES TO HIGH VOLTAGE ASSEMBLY 4060
HV LC0*
HV LC1*
HV LC2*
HV LC3*
HV LC4*
HV LC5*
HV LC6*
HV LC7*
HV FET2*
U13
C28 0.1µF
HV C0*
HV C1*
HV C2*
HV C3*
HV C4*
HV C5*
HV C6*
HV C7*
HV MUX0
HV MUX1
HV MUX2
HV MUX3
CUR LIM
P611
RST (PG3C3)
SOL TP5
SOL
HC4051
U14
MUX5
MUX6
MUX7
(PG1B1)
(PG2C5)
(PG2B3)
PACOM
INH
-5LH
DIAGNOSTIC CIRCUIT
C25 0.1µF
U10
RLY1
RLY2
RLY3
RLY4
RLY5
RLY6
RLY7
RLY8
K1
K2
K3
K13
K4
K8
K5
K12
K6
K9
K10
K11
U8 A
U8 B
U8 F
N/C
B IN
B FB
BSRF6
BRF6
2FCL
HIGH VOLTAGE CONTROL 5700A-1061 3 OF 4 JUL.12,1988

Figure 7-17. A14 High Voltage Control PCA (cont)

	HIGH VOLTAGE A15 ASSEMBLY														HIGH VOLTAGE CONTROL A14 ASSEMBLY																							
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K14	Q10	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	Q3	Q4	U6A	U6B	U6C	U6D	U7A	U7B
DORMANT	R	R	R											*							R												*					
AC 220V RANGE	R	R	R											*							R			*									*					
DC 220V RANGE	R	R	R											*							R												*					
AC 1100V RANGE	R	R	R	*		*								*	*		*				R						*	1	1	1			*					
DC +1100V RANGE	S	R	S		*	*	*						*	*	*		*		*	*	R		*		*	*	*						*					
DC -1100V RANGE	S	R	S		*	*	*						*	*	*		*	*	*	*	R	*	*			*	*									*		
AC 2.2A RANGE	R	R	R								*	*			*	*			*		R					*					*	*		*	*	*		*
DC +2.2A RANGE	R	R	R								*	*			*	*			*		R					*								*	*	*		*
DC -2.2A RANGE	R	R	R								*	*			*	*			*		R					*							*	*	*			*
OFFSET CAL HR7 RNET	S	R	S		*		*		*				*	*							R												*					
GAIN CAL HR7 RNET	R	S	S					*						*							R												*					
AC 220V AC FREQ CHAR	R	R	R								*	*		*							R			*									*					
AC 1100V AC FREQ CHAR	R	R	R	*		*		*		*	*	*		*	*		*				R						*						*					
OFFSET CAL CURRENT RNET	R	R	R								*	*			*	*			*		R					*								*	*	*		*
GAIN CAL CURRENT RNET	R	R	R								*	*			*	*			*		R					*								*	*	*		*
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K14	Q10	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	Q3	Q4	U6A	U6B	U6C	U6D	U7A	U7B

R = RESET POSITION FOR LATCHING RELAYS
S = SET POSITION FOR LATCHING RELAYS
* = ENERGIZED FOR NON-LATCHING RELAYS
* = ON FOR FETS
1 = ENERGIZED DURING OPERATION BELOW 120Hz ONLY
RELAY K7 IS SET DURING CALIBRATION OF THE 1.9 OHM ON THE OHMS CAL ASSEMBLY

HIGH VOLTAGE CONTROL 5700A-1061 4 OF 4 JUL.12.1988

Figure 7-17. A14 High Voltage Control PCA (cont)

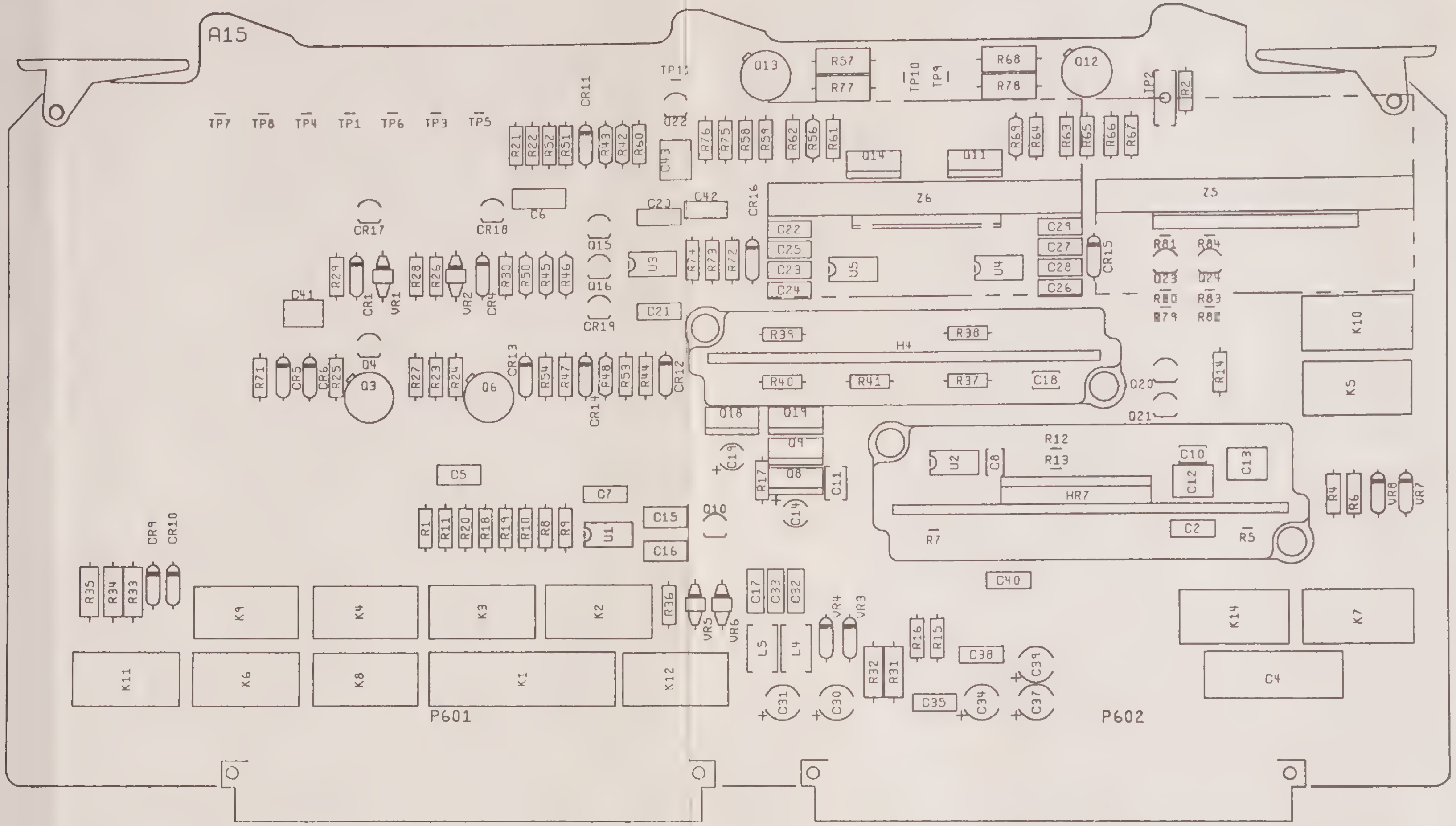
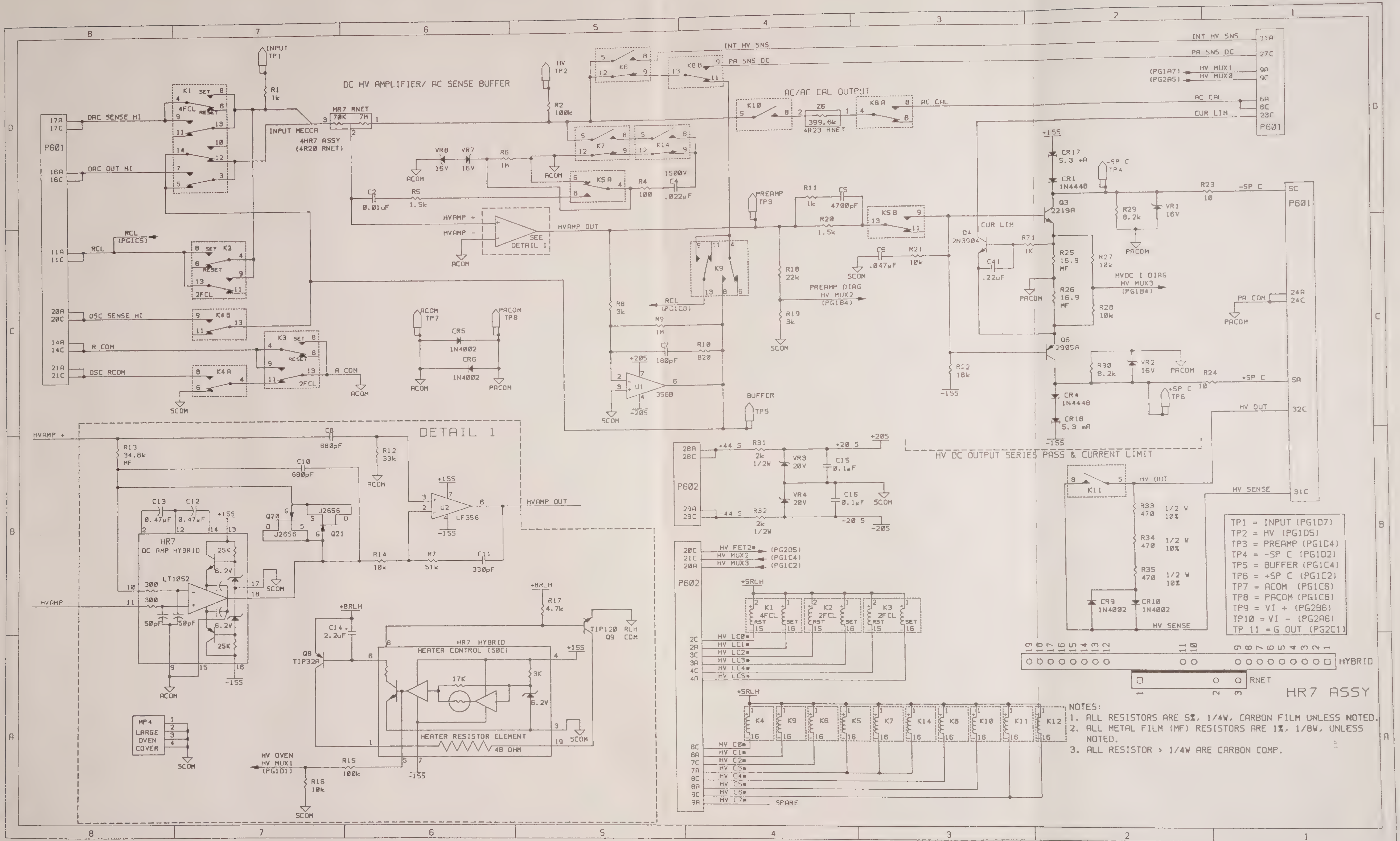

A15
TP7
TP8
TP4
TP1
TP6
TP3
TP5
CR11
TP11
Q22
Q13
R57
R77
TP10
TP9
R68
R78
Q12
TP2
R2
R21
R22
R52
R51
R43
R42
R60
C43
R76
R75
R58
R59
R62
R56
R61
Q14
Q11
R69
R64
R63
R65
R66
R67
C6
C20
C42
CR16
Z6
Z5
CR17
CR18
Q15
C22
C25
C23
C24
C29
C27
C28
C26
CR15
R81
R84
Q23
Q24
R80
R83
R79
R82
R29
CR1
VR1
R28
R26
VR2
CR4
R30
R50
R45
R46
Q16
U3
R74
R73
R72
U5
U4
C41
CR19
C21
R39
R38
H4
K10
R71
CR5
CR6
R25
Q4
Q3
R27
R23
R24
Q6
CR13
R54
R47
CR14
R48
R53
R44
CR12
R40
R41
R37
C18
Q20
R14
K5
Q21
Q18
Q19
Q9
C19
R17
Q8
C11
C14
U2
C8
R12
R13
C10
C13
C12
HR7
R4
R6
VR8
VR7
C5
C7
R1
R11
R20
R18
R19
R10
R8
R9
U1
C15
C16
Q10
R7
C2
R5
CR9
CR10
C40
R35
R34
R33
K9
K4
K3
K2
R36
VR5
VR6
C17
C33
C32
VR4
VR3
K14
K7
L5
L4
R16
R15
C38
C39
K11
K6
K8
K1
K12
R32
R31
C4
C31
C30
C35
C34
C37
P601
P602

Figure 7-18. A15 High Voltage/
High Current PCA


DC HV AMPLIFIER/ AC SENSE BUFFER
INPUT TP1
R1 1k
HV TP2
R2 100k
HR7 RNET 70K 7M
INPUT MECCA 4HR7 ASSY (4R20 RNET)
P601
17A 17C DAC SENSE HI
16A 16C DAC OUT HI
11A 11C RCL
RCL (PG1C5)
20A 20C OSC SENSE HI
14A 14C R COM
21A 21C OSC RCOM
K1 4FCL SET RESET
K2 2FCL SET RESET
K3 2FCL SET RESET
K4A
K4B
A COM
SCOM
ACOM
VR8 16V
VR7 16V
R6 1M
C2 0.01uF
R5 1.5k
HVAMP +
HVAMP -
SEE DETAIL 1
HVAMP OUT
K6
K8B
K7
K14
K5A
R4 100
1500V C4 .022uF
INT HV SNS
PA SNS DC
AC/AC CAL OUTPUT
K10
Z6 399.6k 4R23 RNET
K8A
AC CAL
CUR LIM
INT HV SNS 31A
PA SNS DC 27C
(PG1A7) HV MUX1 9A
(PG2A5) HV MUX0 9C
AC CAL 6A 6C
CUR LIM 23C
P601
ACOM TP7
PACOM TP8
CR5 1N4002
CR6 1N4002
PREAMP TP3
R11 1k
C5 4700pF
R20 1.5k
K5B
K9
R18 22k
PREAMP DIAG HV MUX2 (PG1B4)
R19 3k
C6 .047uF
R21 10k
R8 3k
RCL (PG1C8)
R9 1M
C7 180pF
R10 820
+20S
-20S
U1 3568
BUFFER TP5
+15S
CR17 5.3 mA
CR1 1N4448
Q3 2219A
Q4 2N3904
CUR LIM
R71 1K
C41 .22uF
R25 16.9 MF
R26 16.9 MF
R27 10k
R28 10k
HVDC I DIAG HV MUX3 (PG1B4)
-SP C TP4
R29 8.2k
VR1 16V
R23 10
-SP C
PACOM
Q6 2905A
R22 16k
-15S
R30 8.2k
VR2 16V
R24 10
+SP C
+SP C TP6
CR4 1N4448
CR18 5.3 mA
HV OUT
SC 24A 24C 5A 32C 31C
PA COM
HV DC OUTPUT SERIES PASS & CURRENT LIMIT
DETAIL 1
R13 34.8k MF
C8 680pF
R12 33k
C10 680pF
C13 0.47uF
C12 0.47uF
HR7 DC AMP HYBRID
LT1052
300
300
25K
6.2V
50pF
Q20 J2656
Q21 J2656
U2 LF356
R14 10k
R7 51k
C11 330pF
+8RLH
R17 4.7k
TIP120 Q9
RLH COM
C14 2.2uF
Q8 TIP32A
HR7 HYBRID HEATER CONTROL (50C)
17K
3K
6.2V
HEATER RESISTOR ELEMENT 48 OHM
HV OVEN HV MUX1 (PG1D1)
R15 100k
R16 10k
MP4 LARGE OVEN COVER
P602
28A 28C +44 S
R31 2k 1/2W
VR3 20V
C15 0.1uF
29A 29C -44 S
R32 2k 1/2W
VR4 20V
C16 0.1uF
-20S
20C HV FET2 (PG2D5)
21C HV MUX2 (PG1C4)
20A HV MUX3 (PG1C2)
+5RLH
K1 4FCL RST SET
K2 2FCL RST SET
K3 2FCL RST SET
2C HV LC0
2A HV LC1
3C HV LC2
3A HV LC3
4C HV LC4
4A HV LC5
K4 K9 K6 K5 K7 K14 K8 K10 K11 K12
6C HV C0
6A HV C1
7C HV C2
7A HV C3
8C HV C4
8A HV C5
9C HV C6
9A HV C7
SPARE
K11
HV OUT
R33 470 1/2 W 10%
R34 470 1/2 W 10%
R35 470 1/2 W 10%
CR9 1N4002
CR10 1N4002
HV SENSE
HYBRID
RNET
HR7 ASSY

TP1 = INPUT (PG1D7)
TP2 = HV (PG1D5)
TP3 = PREAMP (PG1D4)
TP4 = -SP C (PG1D2)
TP5 = BUFFER (PG1C4)
TP6 = +SP C (PG1C2)
TP7 = ACOM (PG1C6)
TP8 = PACOM (PG1C6)
TP9 = VI + (PG2B6)
TP10 = VI - (PG2A6)
TP 11 = G OUT (PG2C1)

NOTES:
1. ALL RESISTORS ARE 5%, 1/4W, CARBON FILM UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W, UNLESS NOTED.
3. ALL RESISTOR > 1/4W ARE CARBON COMP.

HIGH VOLTAGE / HIGH CURRENT 5700A-1060 1 OF 2 JUL.12.1988

Figure 7-18. A15 High Voltage/ High Current PCA (cont)

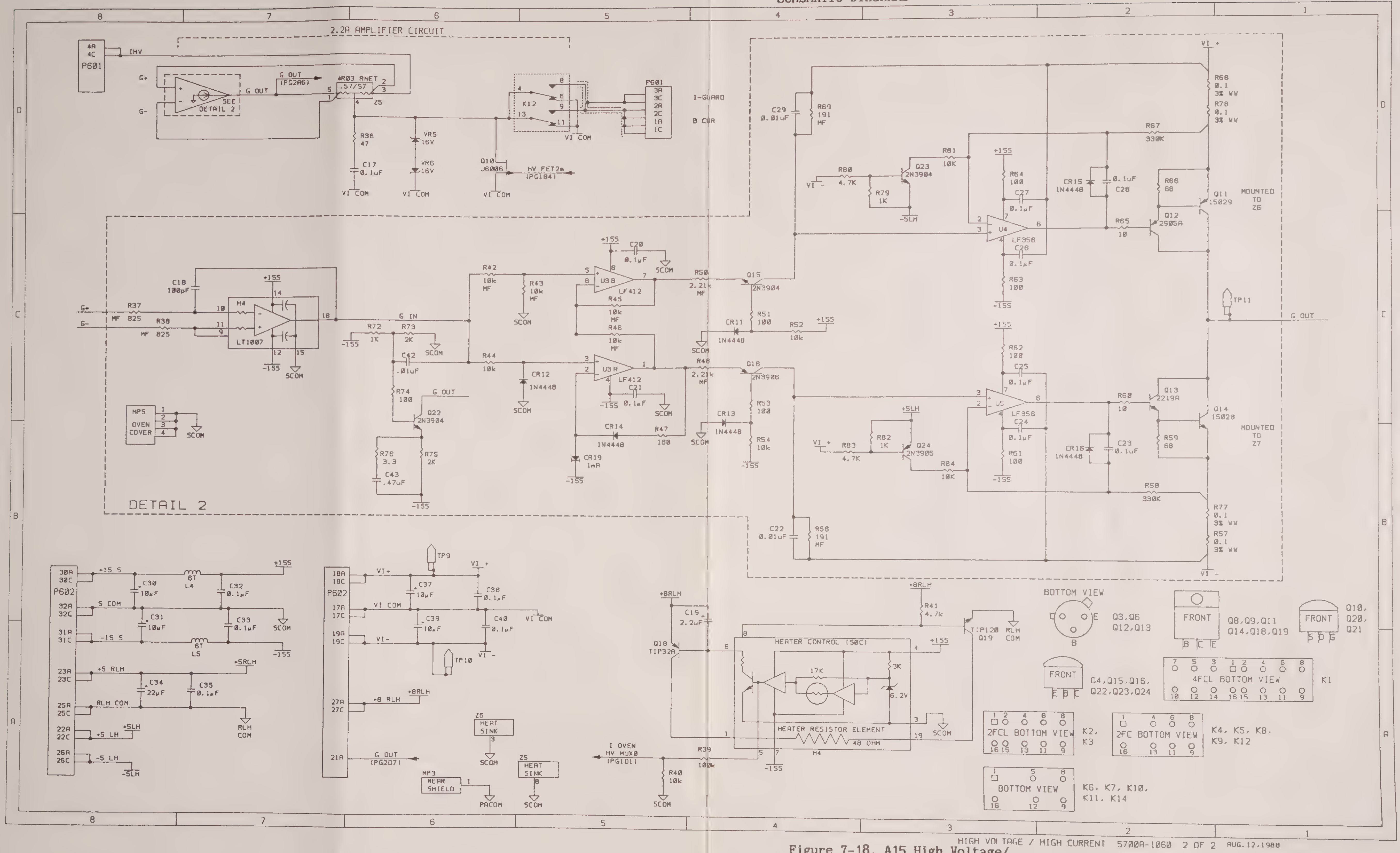

2.2A AMPLIFIER CIRCUIT
4A
4C
P601
IHV
G+
G-
SEE
DETAIL 2
G OUT
G OUT
(PG2A6)
4R03 RNET
.57/57
Z5
K12
P601
3A
3C
2A
2C
1A
1C
I-GUARD
B CUR
R36
47
C17
0.1uF
VR5
16V
VR6
16V
VI COM
Q10
J6006
HV FET2m
(PG1B4)
DETAIL 2
C18
100pF
R37
MF 825
R38
MF 825
H4
LT1007
+15S
-15S
SCOM
G IN
R72
1K
R73
2K
C42
.01uF
R74
100
G OUT
Q22
2N3904
R76
3.3
C43
.47uF
R75
2K
R42
10k
MF
R43
10k
MF
R44
10k
CR12
1N4448
C20
0.1uF
U3 B
LF412
R45
10k
MF
R46
10k
MF
U3 A
LF412
C21
0.1uF
CR14
1N4448
R47
160
CR19
1mA
R50
2.21k
MF
R48
2.21k
MF
Q15
2N3904
Q16
2N3906
R51
100
R52
10k
CR11
1N4448
R53
100
R54
10k
CR13
1N4448
MP5
OVEN
COVER
C29
0.01uF
R69
191
MF
R80
4.7K
R79
1K
Q23
2N3904
-5LH
R81
10K
R64
100
C27
0.1uF
U4
LF356
C26
0.1uF
R63
100
CR15
1N4448
C28
0.1uF
R67
330K
R66
68
R65
10
Q11
15029
Q12
2905A
MOUNTED
TO
Z6
R68
0.1
3% WW
R70
0.1
3% WW
VI +
TP11
G OUT
R62
100
C25
0.1uF
U5
LF356
C24
0.1uF
R61
100
+5LH
R83
4.7K
R82
1K
Q24
2N3906
R84
10K
CR16
1N4448
C23
0.1uF
R60
10
Q13
2219A
Q14
15028
MOUNTED
TO
Z7
R59
68
R58
330K
R77
0.1
3% WW
R57
0.1
3% WW
VI -
C22
0.01uF
R56
191
MF
P602
30A
30C
+15 S
C30
10uF
L4
6T
C32
0.1uF
32A
32C
S COM
C31
10uF
C33
0.1uF
31A
31C
-15 S
L5
6T
23A
23C
+5 RLH
+5RLH
C34
22uF
C35
0.1uF
25A
25C
RLH COM
22A
22C
+5 LH
+5LH
26A
26C
-5 LH
-5LH
P602
18A
18C
VI+
TP9
C37
10uF
C38
0.1uF
17A
17C
VI COM
C39
10uF
C40
0.1uF
19A
19C
VI-
TP10
27A
27C
+8 RLH
+8RLH
21A
G OUT
(PG2D7)
Z6
HEAT
SINK
Z5
HEAT
SINK
MP3
REAR
SHIELD
PACOM
C19
2.2uF
Q18
TIP32A
R41
4.7k
TIP120
Q19
RLH
COM
HEATER CONTROL (50C)
17K
3K
6.2V
HEATER RESISTOR ELEMENT
48 OHM
H4
I OVEN
HV MUX0
(PG1D1)
R39
100k
R40
10k
BOTTOM VIEW
Q3,Q6
Q12,Q13
FRONT
B C E
Q8,Q9,Q11
Q14,Q18,Q19
FRONT
S D G
Q10,
Q20,
Q21
FRONT
E B C
Q4,Q15,Q16,
Q22,Q23,Q24
4FCL BOTTOM VIEW
K1
2FCL BOTTOM VIEW
K2,
K3
2FC BOTTOM VIEW
K4, K5, K8,
K9, K12
BOTTOM VIEW
K6, K7, K10,
K11, K14
HIGH VOLTAGE / HIGH CURRENT 5700A-1060 2 OF 2 AUG.12,1988

Figure 7-18. A15 High Voltage/ High Current PCA (cont)

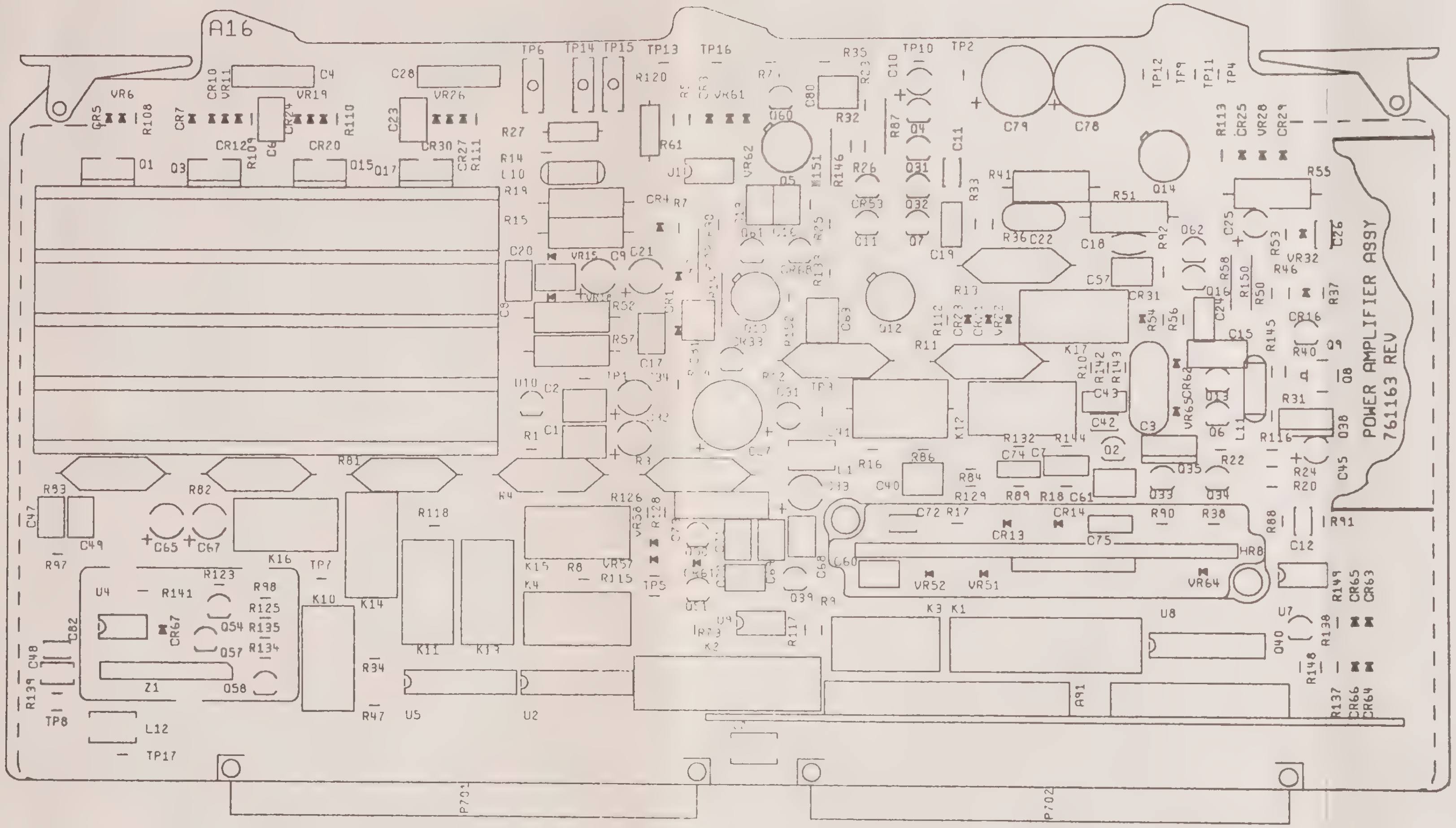
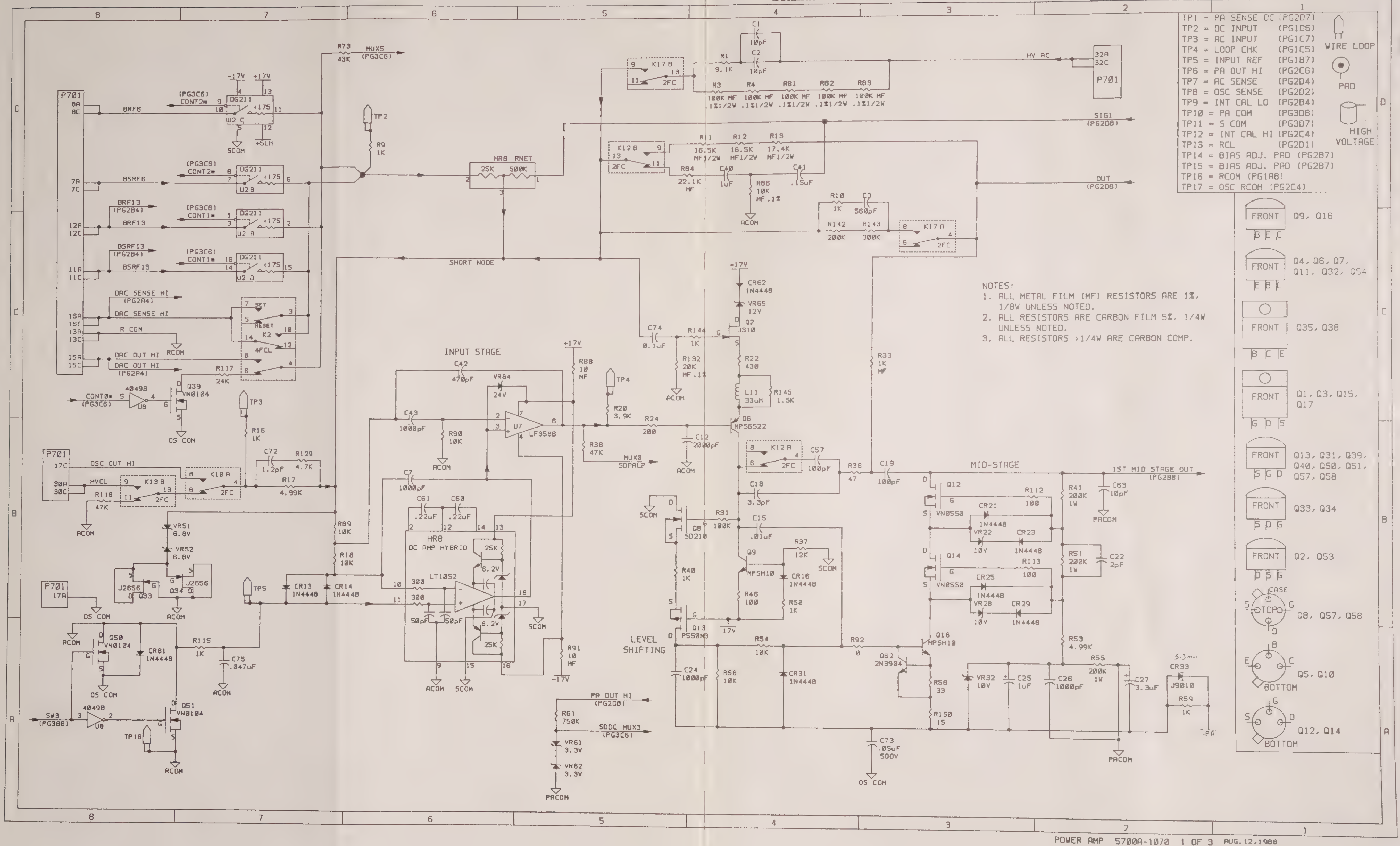

A16
TP6
TP14
TP15
TP13
TP16
R35
TP10
TP2
C4
C28
VR6
VR19
VR76
CR5
R108
CR7
CR10
VR11
CR24
R110
C23
R120
R27
R61
R32
R87
C10
C79
C78
TP12
TP9
TP11
TP4
R113
CR25
VR28
CR29
CR12
CR20
CR30
CR27
R111
Q1
Q3
Q15
Q17
R14
L10
R19
R15
VR62
Q5
R151
R146
R26
Q31
C11
Q60
C80
R41
Q14
R55
CR4
R7
CR53
Q32
R33
R51
C20
VR15
C9
C21
C11
Q7
R36
C22
C18
R92
Q62
C75
R53
VR32
R46
C26
R52
R57
C19
R17
C57
CR31
R58
R150
R50
Q16
R37
CR16
C17
Q12
R11
R112
K17
R145
R56
C24
C15
R40
Q9
Q8
U10
C2
C1
TP1
R62
Q33
TP3
R107
R142
R143
C43
CR65
R31
Q38
C42
C3
Q6
L11
R116
R132
R144
C74
C7
Q2
R22
R24
R20
C45
K12
R81
R93
R82
R4
R3
R126
L1
R16
R86
C40
R84
Q35
Q33
Q34
R129
R89
R18
C61
C47
C49
C65
C67
R118
R128
C72
R17
CR14
R90
R38
R88
R91
C12
CR13
C75
HR8
R97
K16
TP7
K15
R8
VR57
R115
TP5
C60
VR52
VR51
VR64
R149
CR65
CR63
U4
R141
R123
R98
R125
K10
K14
K4
Q39
R9
K3
K1
U8
U7
CR67
Q54
R135
C82
Q57
R134
K11
K13
R117
K2
Q40
R138
C48
R139
Z1
Q58
R34
R148
R47
U5
U2
A91
R137
CR66
CR64
TP8
L12
TP17
P701
P702
POWER AMPLIFIER ASSY
761163 REV

Figure 7-19. A16 Power Amplifier PCA



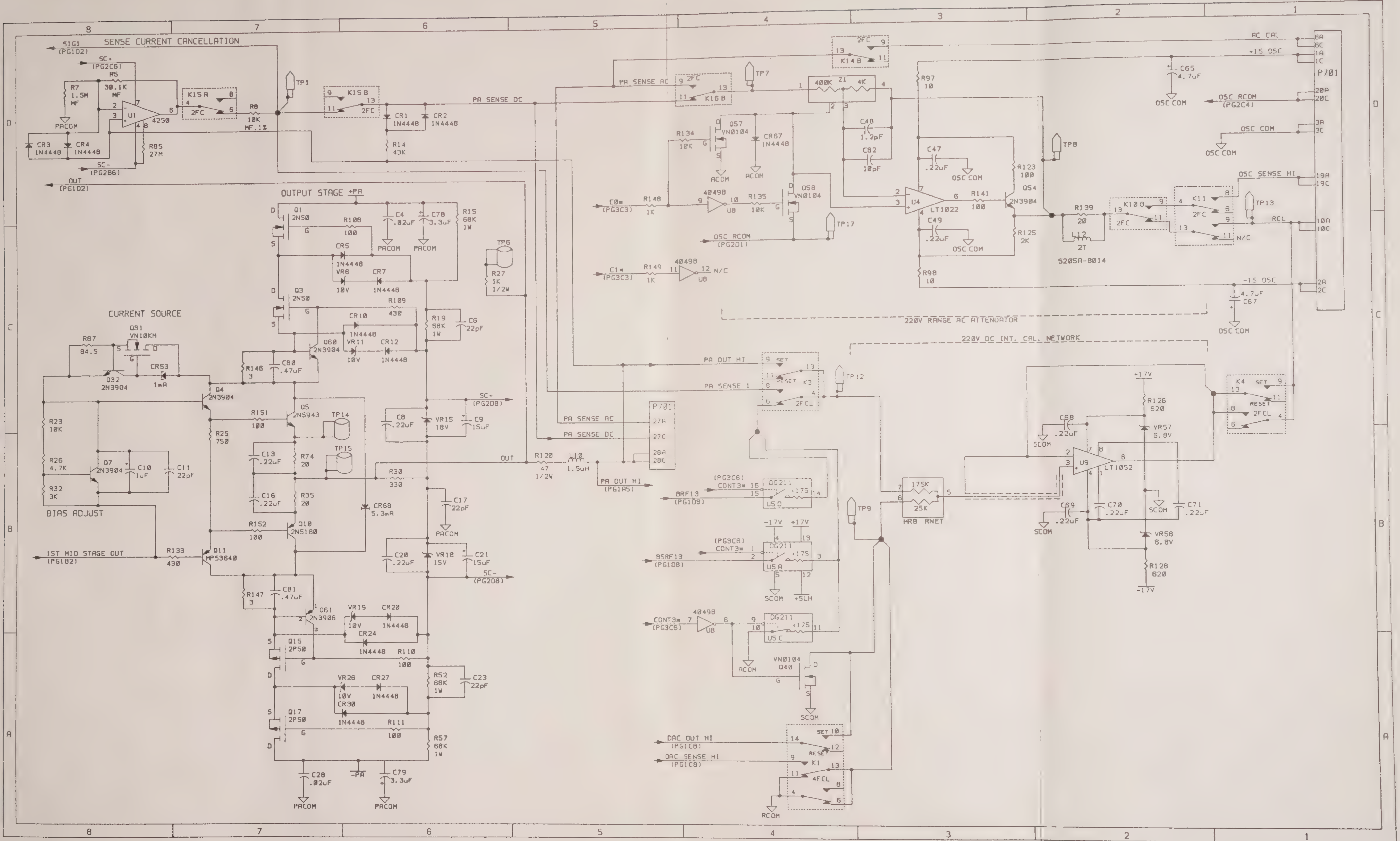
P701
8A
8C
BRF6
(PG3C6)
CONT2=
-17V
+17V
DG211
U2 C
<175
SCOM
+5LH
R73
43K
MUX5
(PG3C6)
TP2
R9
1K
7A
7C
BSRF6
U2 B
HR8 RNET
25K
500K
BRF13
(PG2B4)
CONT1=
U2 A
12A
12C
BSRF13
11A
11C
U2 D
SHORT NODE
DAC SENSE HI
(PG2A4)
R COM
RCOM
SET
RESET
K2
4FCL
16A
16C
13A
13C
15A
15C
DAC OUT HI
R117
24K
40498
U8
CONT0=
Q39
VN0104
OS COM
TP3
R16
1K
17C
OSC OUT HI
HVCL
K13 B
2FC
30A
30C
R118
47K
ACOM
K10 A
C72
1.2pF
R129
4.7K
R17
4.99K
VR51
6.8V
VR52
6.8V
J2656
Q33
Q34
17A
TP5
Q50
VN0104
CR61
1N4448
R115
1K
C75
.047uF
SW3
(PG3B6)
Q51
TP16
R89
10K
R18
10K
CR13
1N4448
CR14
INPUT STAGE
C42
470pF
VR64
24V
U7
LF356B
C43
1000pF
R90
10K
C7
1000pF
C61
.22uF
C60
HR8
DC AMP HYBRID
LT1052
300
50pF
6.2V
-17V
R88
10
MF
TP4
R20
3.9K
R24
200
R38
47K
MUX0
SDPALP
R91
PA OUT HI
(PG2D8)
R61
750K
SDDC MUX3
VR61
3.3V
VR62
PACOM
K17 B
R1
9.1K
C1
10pF
C2
R3
R4
R81
R82
R83
100K MF
.1%1/2W
HV AC
32A
32C
SIG1
(PG2D8)
K12 B
R11
16.5K
MF1/2W
R12
R13
17.4K
R84
22.1K
C40
1uF
R86
10K
MF .1%
C41
.15uF
OUT
R10
C3
560pF
R142
200K
R143
300K
K17 A
C74
0.1uF
R144
R132
20K
MF .1%
+17V
CR62
1N4448
VR65
12V
Q2
J310
R22
430
L11
33uH
R145
1.5K
Q6
MPS6522
C12
2000pF
K12 A
C57
100pF
R36
47
C19
R33
1K
MF
C18
3.3pF
C15
.01uF
R31
100K
Q8
SD210
Q9
MPSH10
R37
12K
CR16
R46
100
R50
R40
Q13
P550N3
LEVEL SHIFTING
C24
1000pF
R54
R56
CR31
C73
.05uF
500V
R92
0
Q62
2N3904
Q16
R58
33
R150
15
MID-STAGE
Q12
VN0550
R112
CR21
VR22
10V
CR23
Q14
R113
CR25
VR28
CR29
R41
200K
1W
C63
10pF
1ST MID STAGE OUT
(PG2B8)
R51
C22
2pF
R53
4.99K
R55
VR32
C25
C26
C27
3.3uF
CR33
J9010
R59
-PA
WIRE LOOP
PAD
HIGH VOLTAGE
FRONT
Q9, Q16
Q4, Q6, Q7, Q11, Q32, Q54
Q35, Q38
Q1, Q3, Q15, Q17
Q13, Q31, Q39, Q40, Q50, Q51, Q57, Q58
Q33, Q34
Q2, Q53
CASE
TOP
Q8, Q57, Q58
BOTTOM
Q5, Q10
Q12, Q14
8
7
6
5
4
3
2
1
D
C
B
A

TP1 = PA SENSE DC (PG2D7)
TP2 = DC INPUT (PG1D6)
TP3 = AC INPUT (PG1C7)
TP4 = LOOP CHK (PG1C5)
TP5 = INPUT REF (PG1B7)
TP6 = PA OUT HI (PG2C6)
TP7 = AC SENSE (PG2D4)
TP8 = OSC SENSE (PG2D2)
TP9 = INT CAL LO (PG2B4)
TP10 = PA COM (PG3D8)
TP11 = S COM (PG3D7)
TP12 = INT CAL HI (PG2C4)
TP13 = RCL (PG2D1)
TP14 = BIAS ADJ. PAD (PG2B7)
TP15 = BIAS ADJ. PAD (PG2B7)
TP16 = RCOM (PG1A8)
TP17 = OSC RCOM (PG2C4)

NOTES:
1. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.
2. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
3. ALL RESISTORS >1/4W ARE CARBON COMP.

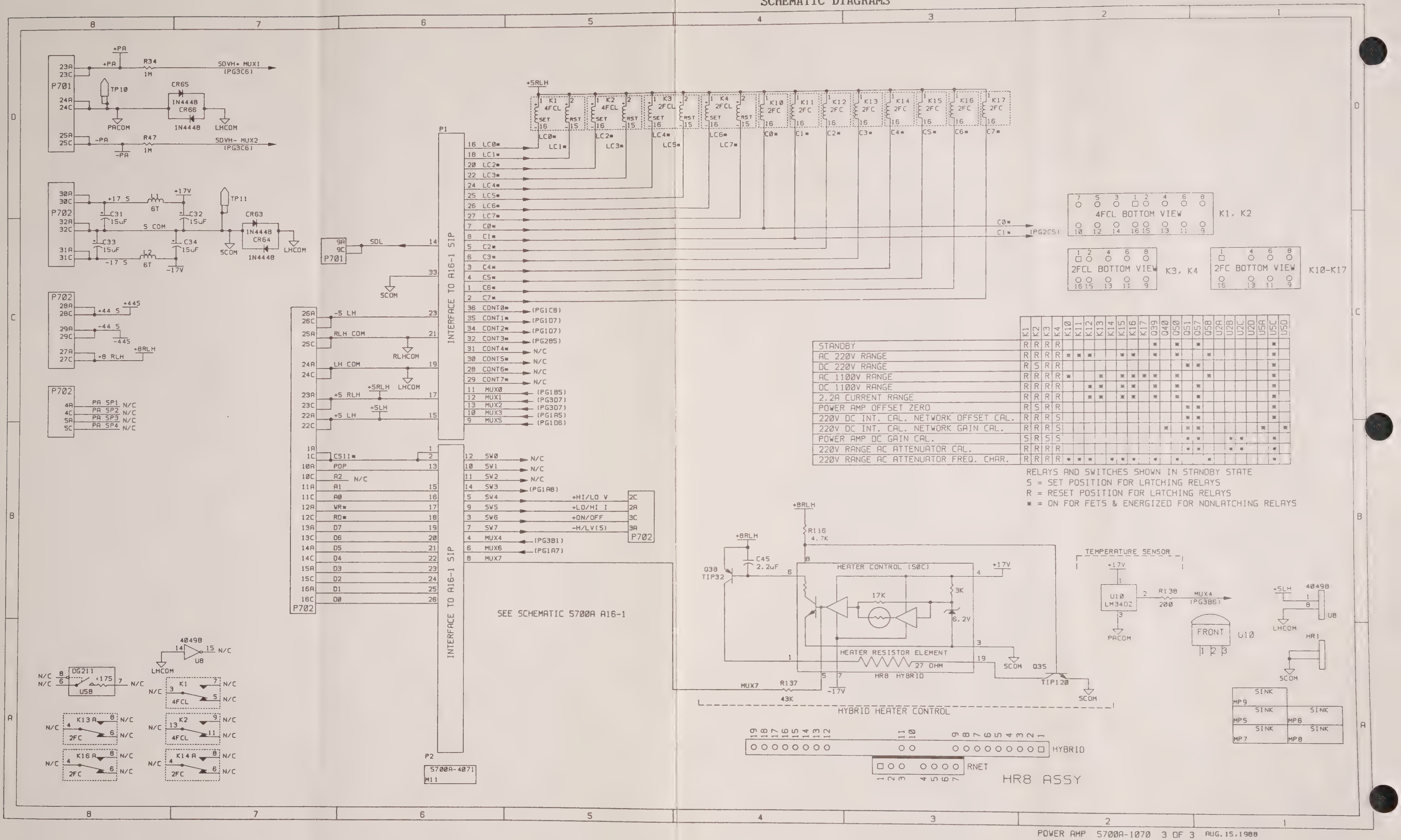
POWER AMP 5700A-1070 1 OF 3 AUG.12.1988

Figure 7-19. A16 Power Amplifier PCA (cont)


SENSE CURRENT CANCELLATION
SIG1 (PG1D2)
SC+ (PG2C6)
R5 30.1K MF
R7 1.5M MF
U1 4250
K15 A 2FC
R8 10K MF,1%
TP1
K15 B 2FC
PA SENSE DC
CR1 1N4448
CR2 1N4448
R14 43K
CR3 1N4448
CR4 1N4448
R85 27M
PACOM
SC- (PG2B6)
OUT (PG1D2)
OUTPUT STAGE
+PA
Q1 2N50
R108 100
C4 .02uF
C78 3.3uF
R15 68K 1W
CR5 1N4448
VR6 10V
CR7 1N4448
Q3 2N50
R109 430
CR10 1N4448
VR11 10V
CR12 1N4448
Q60 2N3904
R19 68K 1W
C6 22pF
TP6
R27 1K 1/2W
CURRENT SOURCE
Q31 VN10KM
R87 84.5
CR53 1mA
Q32 2N3904
Q4 2N3904
R146 3
C80 .47uF
R23 10K
R26 4.7K
R32 3K
Q7 2N3904
C10 1uF
C11 22pF
BIAS ADJUST
R25 750
R151 100
Q5 2N5943
TP14
TP15
C13 .22uF
R74 20
C16 .22uF
R35 20
C8 .22uF
VR15 18V
C9 15uF
SC+ (PG2D8)
OUT
R120 47 1/2W
L10 1.5uH
R30 330
C17 22pF
CR68 5.3mA
R152 100
Q10 2N5160
1ST MID STAGE OUT (PG1B2)
R133 430
Q11 MPS3640
C20 .22uF
VR18 15V
C21 15uF
SC- (PG2D8)
R147 3
C81 .47uF
Q61 2N3906
VR19 10V
CR20 1N4448
CR24 1N4448
Q15 2P50
R110 100
R52 68K 1W
C23 22pF
VR26 10V
CR27 1N4448
CR30 1N4448
Q17 2P50
R111 100
R57 68K 1W
C28 .02uF
-PA
C79 3.3uF
PA OUT HI (PG1A5)
PA SENSE AC
PA SENSE DC
P701 27A 27C 28A 28C
PA SENSE AC
K16 B 2FC
TP7
Z1 400K 4K
Q57 VN0104
R134 10K
CR67 1N4448
ACOM
C48 1.2pF
C82 10pF
C0= (PG3C3)
R148 1K
40498 U8
R135 10K
Q58 VN0104
OSC RCOM (PG2D1)
TP17
C1= (PG3C3)
R149 1K
N/C
K14 B 2FC
R97 10
C47 .22uF
OSC COM
U4 LT1022
R141 100
Q54 2N3904
C49 .22uF
R123 100
R125 2K
TP8
R98 10
R139 20
L12 2T
5205A-8014
K10 B 2FC
K11 2FC
TP13
RCL
N/C
AC CAL
+15 OSC
C65 4.7uF
OSC RCOM (PG2C4)
OSC COM
OSC SENSE HI
-15 OSC
C67 4.7uF
P701 6A 6C 1A 1C 20A 20C 3A 3C 19A 19C 10A 10C 2A 2C
220V RANGE AC ATTENUATOR
220V DC INT. CAL. NETWORK
PA OUT HI
PA SENSE 1
K3 SET RESET 2FCL
TP12
K4 SET RESET 2FCL
+17V
R126 620
VR57 6.8V
C68 .22uF
SCOM
U9 LT1052
C69 .22uF
C70 .22uF
C71 .22uF
VR58 6.8V
R128 620
-17V
175K 25K HR8 RNET
TP9
BRF13 (PG1D8)
(PG3C6) CONT3=
DG211 U5 D
BSRF13 (PG1D8)
U5 A
+5LH
CONT3= (PG3C6)
U5 C
VN0104 Q40
DAC OUT HI (PG1C8)
DAC SENSE HI (PG1C8)
K1 SET RESET 4FCL
RCOM
8 7 6 5 4 3 2 1
D C B A

POWER AMP 5700A-1070 2 OF 3 AUG.12.1988

Figure 7-19. A16 Power Amplifier PCA (cont)


P701
23A
23C
24A
24C
25A
25C
+PA
R34
1M
SDVH+ MUX1
(PG3C6)
TP10
CR65
1N4448
CR66
1N4448
PACOM
LHCOM
-PA
R47
1M
SDVH- MUX2
(PG3C6)
P702
30A
30C
32A
32C
31A
31C
+17 S
6T
+17V
C31
15uF
C32
15uF
S COM
C33
15uF
C34
15uF
-17 S
L2
6T
-17V
TP11
CR63
1N4448
CR64
1N4448
SCOM
LHCOM
28A
28C
+44 S
+445
29A
29C
-44 S
-445
27A
27C
+8 RLH
+8RLH
PA SP1 N/C
PA SP2 N/C
PA SP3 N/C
PA SP4 N/C
4A
4C
5A
5C
SDL
9A
9C
P701
SCOM
-5 LH
RLH COM
RLHCOM
LH COM
LHCOM
+5 RLH
+5RLH
+5 LH
+5LH
26A
26C
25A
25C
24A
24C
23A
23C
22A
22C
1A
1C
10A
10C
11A
11C
12A
12C
13A
13C
14A
14C
15A
15C
16A
16C
CS11
POP
A2 N/C
A1
A0
WR
RD
D7
D6
D5
D4
D3
D2
D1
D0
P702
P1
INTERFACE TO A16-1 SIP
16 LC0
18 LC1
20 LC2
22 LC3
24 LC4
25 LC5
26 LC6
27 LC7
7 C0
8 C1
5 C2
6 C3
3 C4
4 C5
1 C6
2 C7
36 CONT0 (PG1C8)
35 CONT1 (PG1D7)
34 CONT2 (PG1D7)
32 CONT3 (PG2B5)
31 CONT4 N/C
30 CONT5 N/C
28 CONT6 N/C
29 CONT7 N/C
11 MUX0 (PG1B5)
12 MUX1 (PG3D7)
13 MUX2 (PG3D7)
10 MUX3 (PG1A5)
9 MUX5 (PG1D6)
+5RLH
K1 4FCL SET RST
K2 4FCL SET RST
K3 2FCL SET RST
K4 2FCL SET RST
K10 2FC
K11 2FC
K12 2FC
K13 2FC
K14 2FC
K15 2FC
K16 2FC
K17 2FC
C0 → C1 → (PG2C5)
4FCL BOTTOM VIEW K1, K2
2FCL BOTTOM VIEW K3, K4
2FC BOTTOM VIEW K10-K17
INTERFACE TO A16-1 SIP
12 SW0 N/C
10 SW1 N/C
11 SW2 N/C
14 SW3 (PG1A8)
5 SW4 +HI/LO V 2C
3 SW5 +LO/HI I 2A
9 SW6 +ON/OFF 3C
7 SW7 -H/LV(S) 3A
P702
4 MUX4 (PG3B1)
6 MUX6 (PG1A7)
8 MUX7
SEE SCHEMATIC 5700A A16-1
P2
5700A-4071
M11
40498
U8
N/C
LHCOM
DG211
U58
K1 4FCL
K2 4FCL
K13 A 2FC
K14 A 2FC
K16 A 2FC
+8RLH
R116
4.7K
+8RLH
C45
2.2uF
Q38
TIP32
HEATER CONTROL (50C)
17K
3K
6.2V
+17V
HEATER RESISTOR ELEMENT
27 OHM
HR8 HYBRID
MUX7
R137
43K
-17V
SCOM
Q35
TIP120
SCOM
HYBRID HEATER CONTROL
TEMPERATURE SENSOR
+17V
U10
LM34DZ
R138
200
MUX4
(PG3B6)
PACOM
FRONT
U10
+5LH
40498
U8
LHCOM
HR1
SCOM
SINK
MP9
MP5
MP6
MP7
MP8
HYBRID
RNET
HR8 ASSY

	K1	K2	K3	K4	K10	K11	K12	K13	K14	K15	K16	K17	Q39	Q40	Q50	Q51	Q57	Q58	U2A	U2B	U2C	U2D	U5A	U5C	U5D
STANDBY	R	R	R	R									*		*		*							*	
AC 220V RANGE	R	R	R	R	*	*	*			*	*		*		*			*						*	
DC 220V RANGE	R	S	R	R												*	*							*	
AC 1100V RANGE	R	R	R	R	*			*		*	*	*	*		*			*						*	
DC 1100V RANGE	R	R	R	R			*	*		*	*		*		*		*							*	
2.2A CURRENT RANGE	R	R	R	R			*	*		*	*		*		*		*							*	
POWER AMP OFFSET ZERO	R	S	R	R												*	*							*	
220V DC INT. CAL. NETWORK OFFSET CAL.	R	R	R	S												*	*							*	
220V DC INT. CAL. NETWORK GAIN CAL.	R	R	R	S										*		*	*						*		*
POWER AMP DC GAIN CAL.	S	R	S	S												*	*			*	*			*	
220V RANGE AC ATTENUATOR CAL.	R	R	R	R												*	*			*	*			*	
220V RANGE AC ATTENUATOR FREQ. CHAR.	R	R	R	R	*	*	*		*	*	*		*		*			*						*	

RELAYS AND SWITCHES SHOWN IN STANDBY STATE
S = SET POSITION FOR LATCHING RELAYS
R = RESET POSITION FOR LATCHING RELAYS
* = ON FOR FETS & ENERGIZED FOR NONLATCHING RELAYS

POWER AMP 5700A-1070 3 OF 3 AUG.15.1988

Figure 7-19. A16 Power Amplifier PCA (cont)

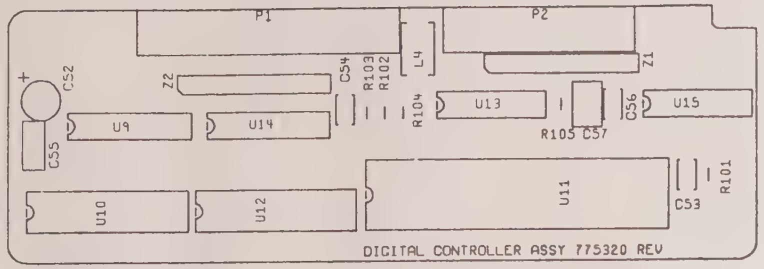
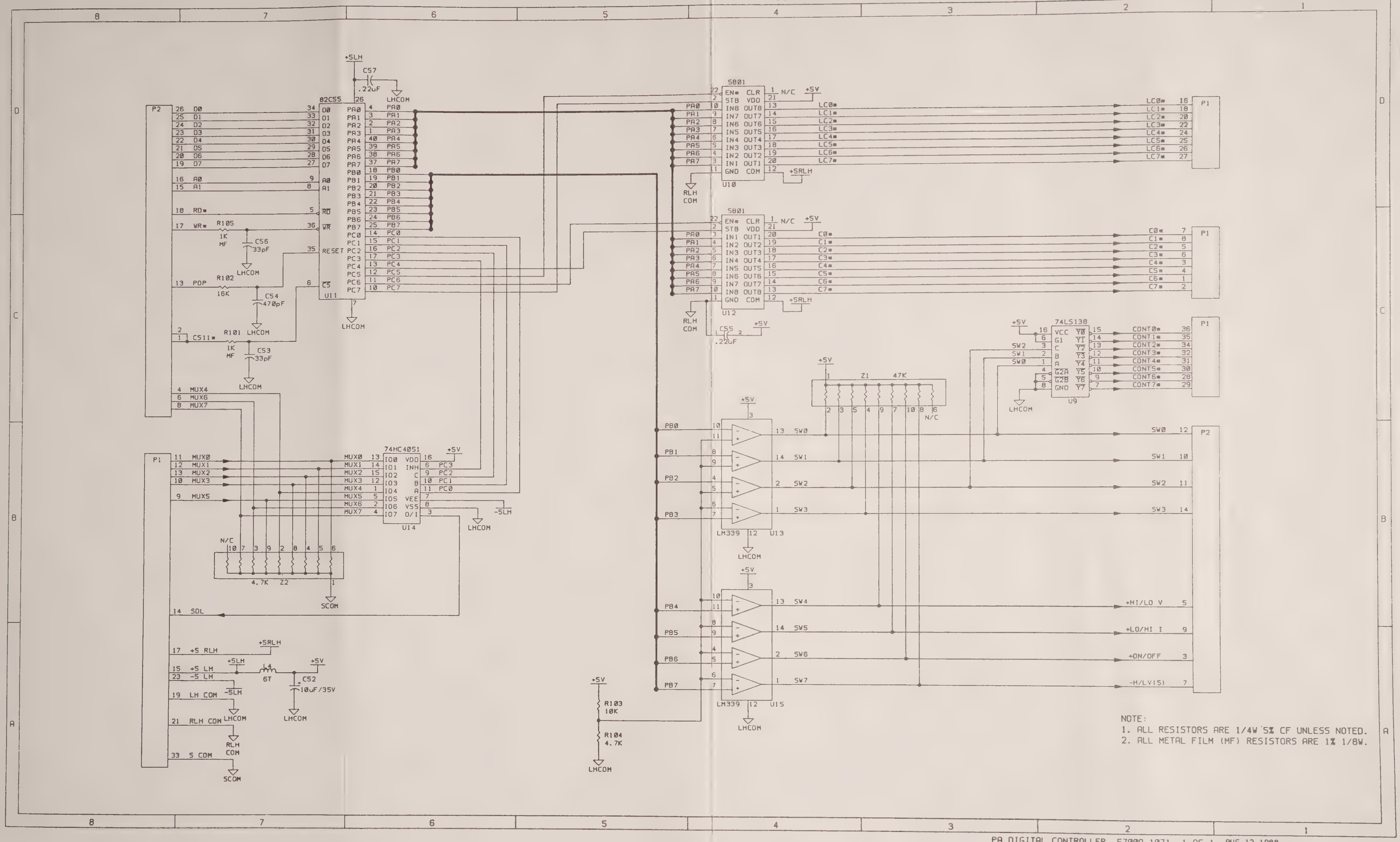

P1
P2
L4
Z1
Z2
C52
+
C54
R103
R102
R104
U13
U15
C56
R105
C57
U9
U14
C55
U10
U12
U11
C53
R101
DIGITAL CONTROLLER ASSY 775320 REV

Figure 7-20. A16A1 Power Amplifier
Digital Control SIP PCA (cont)


82C55
U11
5801
U10
U12
74LS138
U9
74HC4051
U14
LM339
U13
U15
Z1 47K
Z2 4.7K
P1
P2
R105 1K MF
C56 33pF
R102 16K
C54 470pF
R101 1K MF
C53 33pF
C57 .22uF
C55 .22uF
L4 6T
C52 10uF/35V
R103 10K
R104 4.7K
+SLH
+SRLH
+5V
-5LH
LHCOM
RLH COM
SCOM
MUX0
MUX1
MUX2
MUX3
MUX4
MUX5
MUX6
MUX7
SDL
CS11■
RD■
WR■
POP
+5 RLH
+5 LH
-5 LH
LH COM
RLH COM
S COM
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
+HI/LO V
+LO/HI I
+ON/OFF
-H/LV(S)
CONT0■
CONT1■
CONT2■
CONT3■
CONT4■
CONT5■
CONT6■
CONT7■
LC0■
LC1■
LC2■
LC3■
LC4■
LC5■
LC6■
LC7■
C0■
C1■
C2■
C3■
C4■
C5■
C6■
C7■
N/C

NOTE:
1. ALL RESISTORS ARE 1/4W 5% CF UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1% 1/8W.

PA DIGITAL CONTROLLER 5700A-1071 1 OF 1 AUG.12,1988

Figure 7-20. A16A1 Power Amplifier Digital Control SIP PCA (cont)

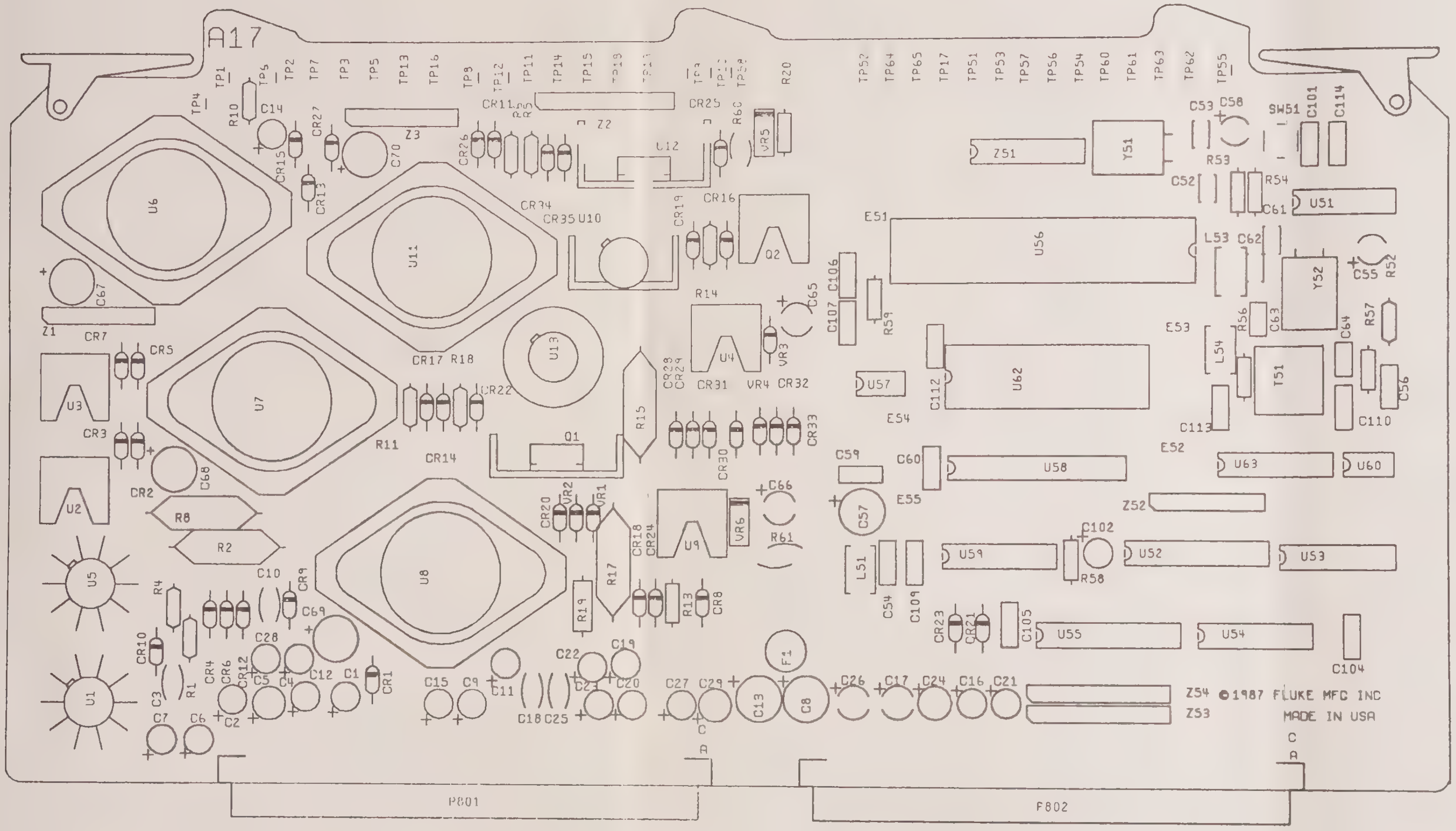

A17
TP1
TP6
TP2
TP7
TP3
TP5
TP13
TP16
TP8
TP12
TP11
TP14
TP15
TP18
TP4
R10
C14
CR27
Z3
C70
CR15
CR13
U6
CR26
CR11
Z2
U12
CR25
VR5
R20
CR34
CR35
U10
CR19
CR16
Q2
U11
C67
Z1
CR7
CR5
U3
CR3
U7
R11
CR17
R18
U13
R14
U4
CR28
CR29
CR31
VR4
CR32
VR3
C65
CR22
CR14
Q1
R15
CR30
CR33
C68
CR2
U2
R8
R2
U5
R4
C10
CR9
C69
CR10
CR4
CR6
CR12
R1
C3
U1
C7
C6
C2
C28
C5
C4
C12
C1
CR1
U8
CR20
VR2
VR1
CR18
CR24
R17
R19
U9
VR6
C66
R61
R13
CR8
C15
C9
C11
C18
C25
C22
C23
C19
C20
C27
C29
C13
C8
F1
C26
C17
C24
C16
C21
TP52
TP64
TP65
TP17
TP51
TP53
TP57
TP56
TP54
TP60
TP61
TP63
TP62
TP55
Z51
Y51
C53
C58
SW51
C101
C114
R53
C52
R54
C61
U51
E51
U56
C106
C107
R59
L53
C62
Y52
C55
R52
E53
L54
R56
C63
C64
R57
T51
C56
U57
C112
U62
E54
C113
C110
E52
C59
C60
U58
U63
U60
C57
E55
Z52
C102
L51
C54
C109
U59
R58
U52
U53
CR23
CR21
C105
U55
U54
C104
Z54
Z53
©1987 FLUKE MFG INC
MADE IN USA
C
A
P801
P802

Figure 7-21. A17 Regulator/Guard Crossing PCA

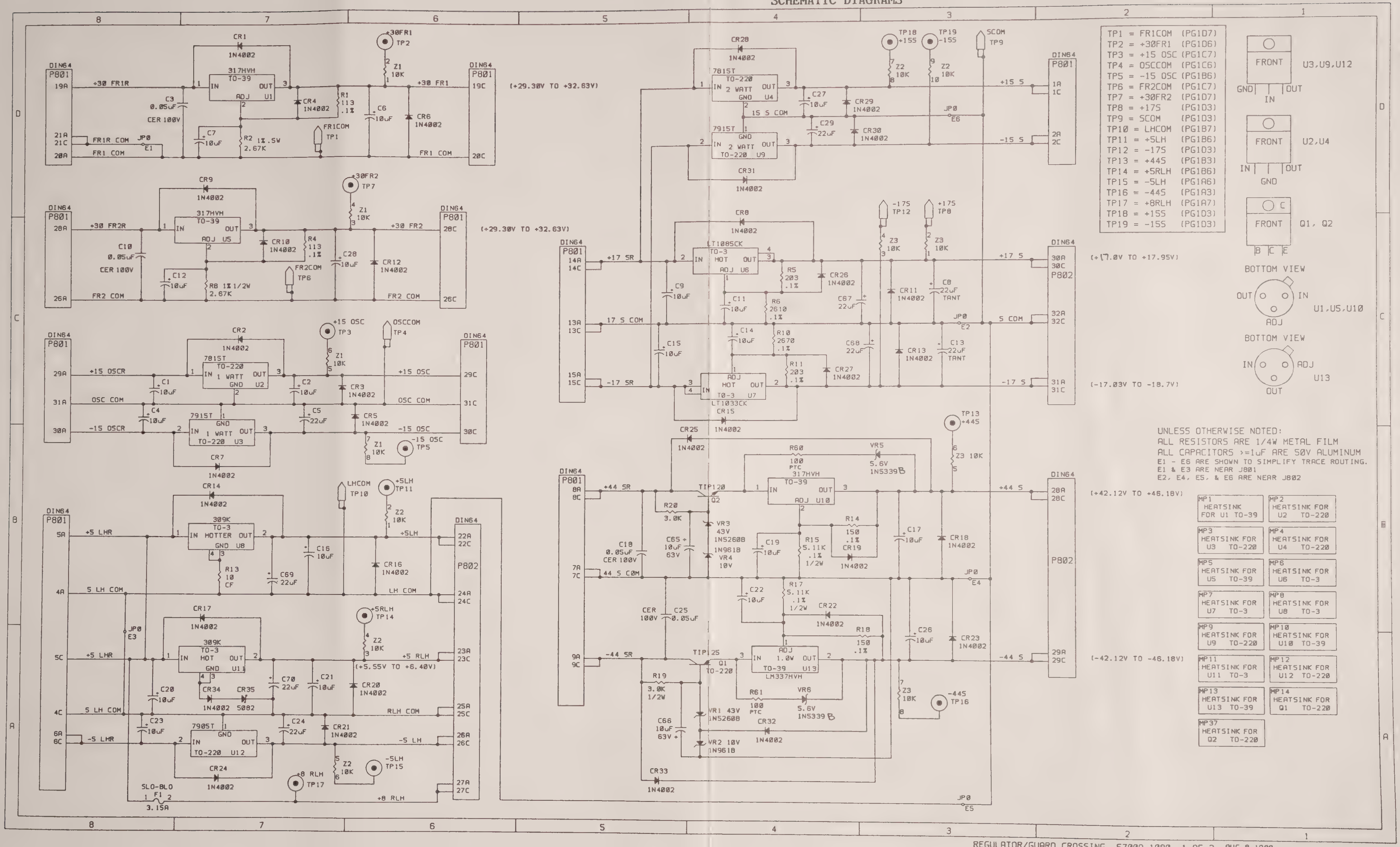
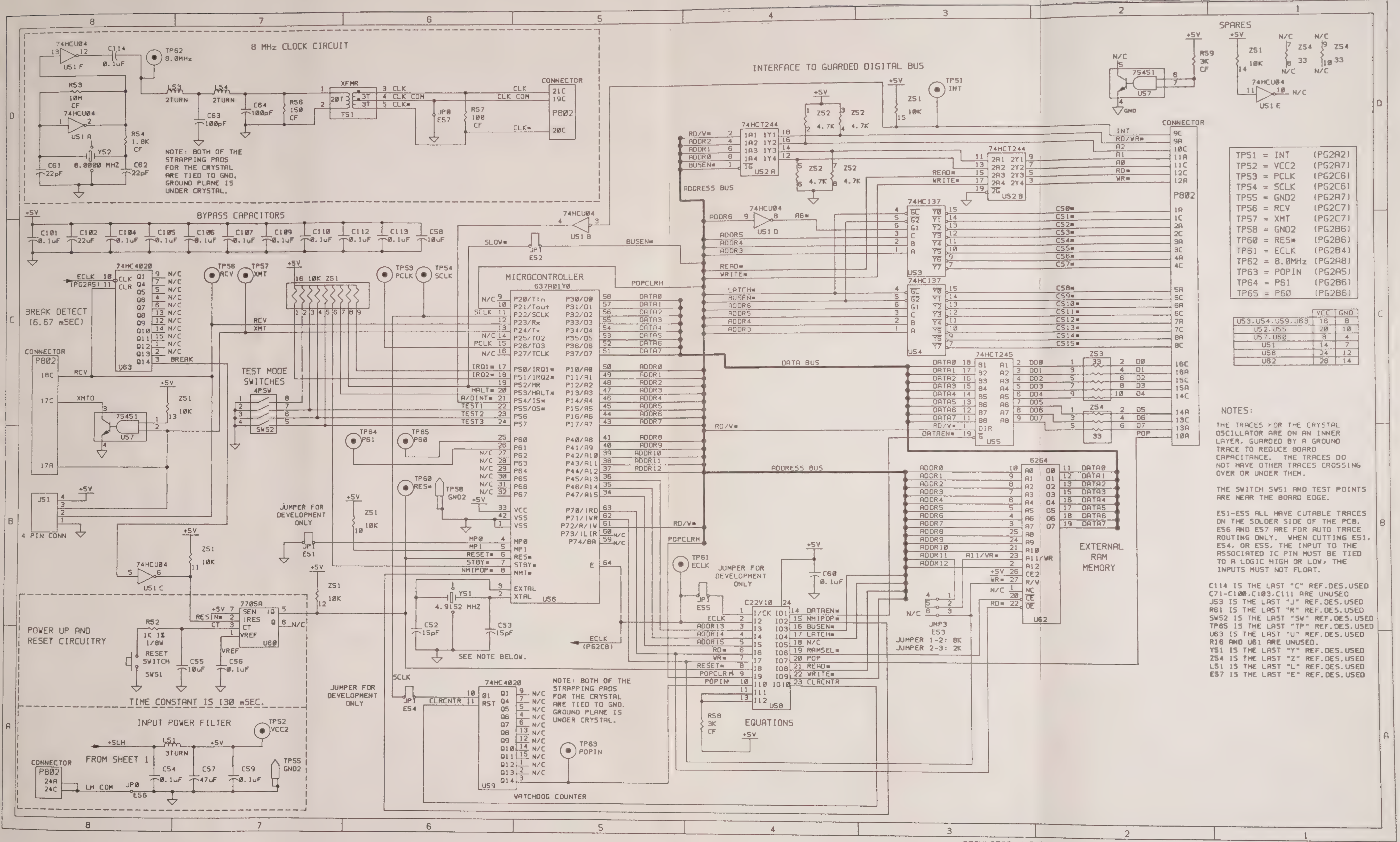

TP1 = FR1COM (PG1D7)
TP2 = +30FR1 (PG1D6)
TP3 = +15 OSC (PG1C7)
TP4 = OSCCOM (PG1C6)
TP5 = -15 OSC (PG1B6)
TP6 = FR2COM (PG1C7)
TP7 = +30FR2 (PG1D7)
TP8 = +17S (PG1D3)
TP9 = SCOM (PG1D3)
TP10 = LHCOM (PG1B7)
TP11 = +5LH (PG1B6)
TP12 = -17S (PG1D3)
TP13 = +44S (PG1B3)
TP14 = +5RLH (PG1B6)
TP15 = -5LH (PG1A6)
TP16 = -44S (PG1A3)
TP17 = +8RLH (PG1A7)
TP18 = +15S (PG1D3)
TP19 = -15S (PG1D3)
FRONT U3,U9,U12 GND IN OUT
FRONT U2,U4 IN GND OUT
FRONT Q1, Q2 B C E
BOTTOM VIEW OUT IN ADJ U1,U5,U10
BOTTOM VIEW IN ADJ OUT U13
UNLESS OTHERWISE NOTED:
ALL RESISTORS ARE 1/4W METAL FILM
ALL CAPACITORS >=1uF ARE 50V ALUMINUM
E1 - E6 ARE SHOWN TO SIMPLIFY TRACE ROUTING.
E1 & E3 ARE NEAR J801
E2, E4, E5, & E6 ARE NEAR J802
MP1 HEATSINK FOR U1 TO-39
MP2 HEATSINK FOR U2 TO-220
MP3 HEATSINK FOR U3 TO-220
MP4 HEATSINK FOR U4 TO-220
MP5 HEATSINK FOR U5 TO-39
MP6 HEATSINK FOR U6 TO-3
MP7 HEATSINK FOR U7 TO-3
MP8 HEATSINK FOR U8 TO-3
MP9 HEATSINK FOR U9 TO-220
MP10 HEATSINK FOR U10 TO-39
MP11 HEATSINK FOR U11 TO-3
MP12 HEATSINK FOR U12 TO-220
MP13 HEATSINK FOR U13 TO-39
MP14 HEATSINK FOR Q1 TO-220
MP37 HEATSINK FOR Q2 TO-220
(+29.30V TO +32.63V)
(+17.0V TO +17.95V)
(-17.03V TO -18.7V)
(+42.12V TO +46.18V)
(-42.12V TO -46.18V)
(+5.55V TO +6.40V)
DIN64 P801
DIN64 P802
317HVH
7815T
7915T
LT1085CK
LT1033CK
309K
7905T
LM337HVH
TIP120
TIP125
SLO-BLO F1 3.15A
REGULATOR/GUARD CROSSING 5700A-1080 1 OF 2 AUG.8,1988

Figure 7-21. A17 Regulator/Guard Crossing PCA (cont)


8 MHz CLOCK CIRCUIT
NOTE: BOTH OF THE STRAPPING PADS FOR THE CRYSTAL ARE TIED TO GND. GROUND PLANE IS UNDER CRYSTAL.
BYPASS CAPACITORS
BREAK DETECT (6.67 mSEC)
TEST MODE SWITCHES
MICROCONTROLLER 637A01Y0
INTERFACE TO GUARDED DIGITAL BUS
ADDRESS BUS
DATA BUS
SPARES
EXTERNAL RAM MEMORY
JUMPER FOR DEVELOPMENT ONLY
POWER UP AND RESET CIRCUITRY
TIME CONSTANT IS 130 mSEC.
INPUT POWER FILTER
FROM SHEET 1
SEE NOTE BELOW.
NOTE: BOTH OF THE STRAPPING PADS FOR THE CRYSTAL ARE TIED TO GND. GROUND PLANE IS UNDER CRYSTAL.
WATCHDOG COUNTER
EQUATIONS
JUMPER 1-2: 8K
JUMPER 2-3: 2K
CONNECTOR P802

TP51 = INT (PG2A2)
TP52 = VCC2 (PG2A7)
TP53 = PCLK (PG2C6)
TP54 = SCLK (PG2C6)
TP55 = GND2 (PG2A7)
TP56 = RCV (PG2C7)
TP57 = XMT (PG2C7)
TP58 = GND2 (PG2B6)
TP60 = RES* (PG2B6)
TP61 = ECLK (PG2B4)
TP62 = 8.0MHz (PG2A8)
TP63 = POPIN (PG2A5)
TP64 = P61 (PG2B6)
TP65 = P60 (PG2B6)

	VCC	GND
U53,U54,U59,U63	16	8
U52,U55	20	10
U57,U60	8	4
U51	14	7
U58	24	12
U62	28	14

NOTES:

THE TRACES FOR THE CRYSTAL OSCILLATOR ARE ON AN INNER LAYER, GUARDED BY A GROUND TRACE TO REDUCE BOARD CAPACITANCE. THE TRACES DO NOT HAVE OTHER TRACES CROSSING OVER OR UNDER THEM.

THE SWITCH SW51 AND TEST POINTS ARE NEAR THE BOARD EDGE.

E51-E55 ALL HAVE CUTABLE TRACES ON THE SOLDER SIDE OF THE PCB. E56 AND E57 ARE FOR AUTO TRACE ROUTING ONLY. WHEN CUTTING E51, E54, OR E55, THE INPUT TO THE ASSOCIATED IC PIN MUST BE TIED TO A LOGIC HIGH OR LOW, THE INPUTS MUST NOT FLOAT.

C114 IS THE LAST "C" REF.DES.USED
C71-C100,C103,C111 ARE UNUSED
J53 IS THE LAST "J" REF.DES.USED
R61 IS THE LAST "R" REF.DES.USED
SW52 IS THE LAST "SW" REF.DES.USED
TP65 IS THE LAST "TP" REF.DES.USED
U63 IS THE LAST "U" REF.DES.USED
R16 AND U61 ARE UNUSED.
Y51 IS THE LAST "Y" REF.DES.USED
Z54 IS THE LAST "Z" REF.DES.USED
L51 IS THE LAST "L" REF.DES.USED
E57 IS THE LAST "E" REF.DES.USED

REGULATOR / GUARD CROSSING 5700A-1080 2 OF 2 AUG.8.1988

Figure 7-21. A17 Regulator/Guard Crossing PCA (cont)

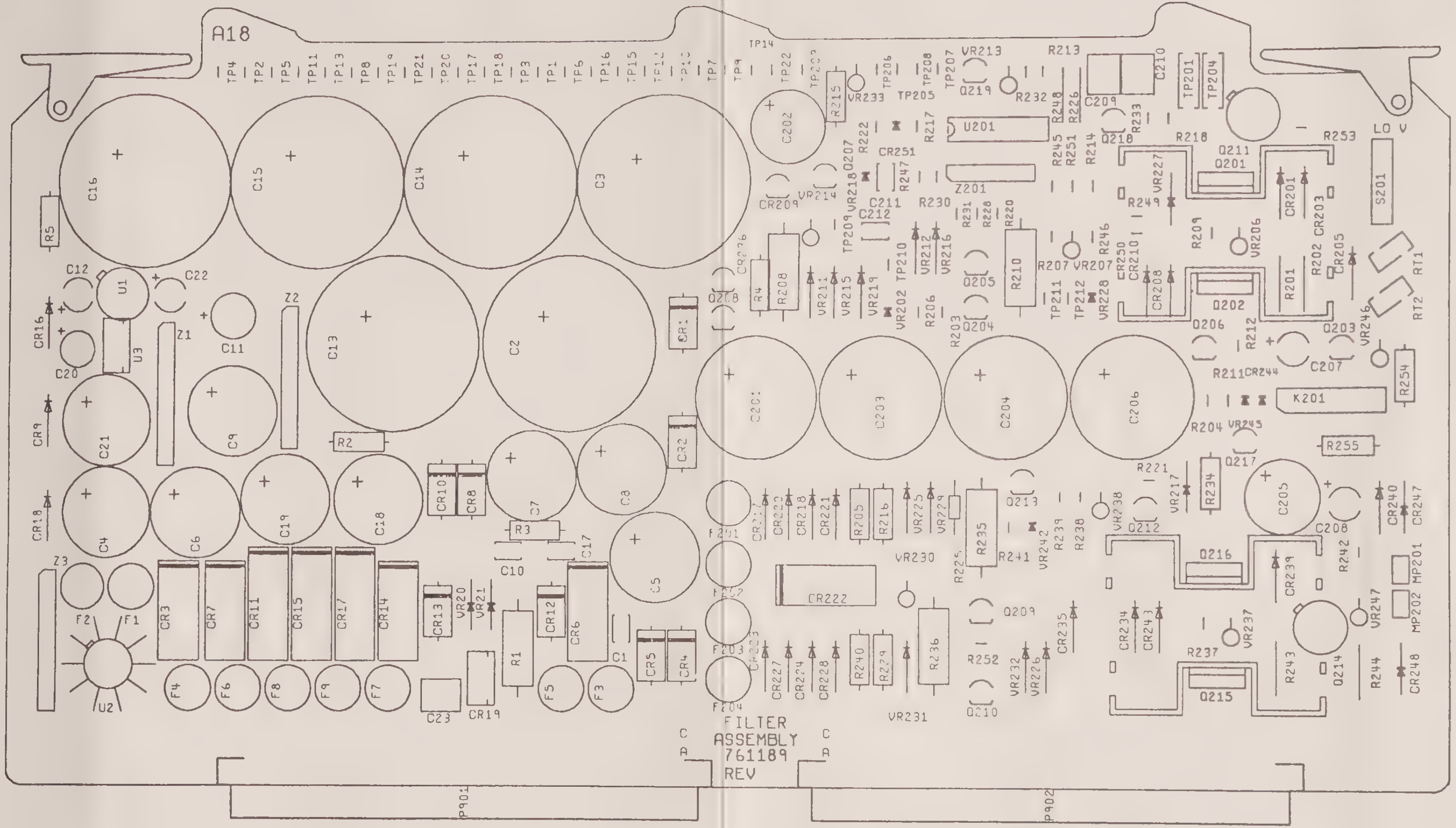
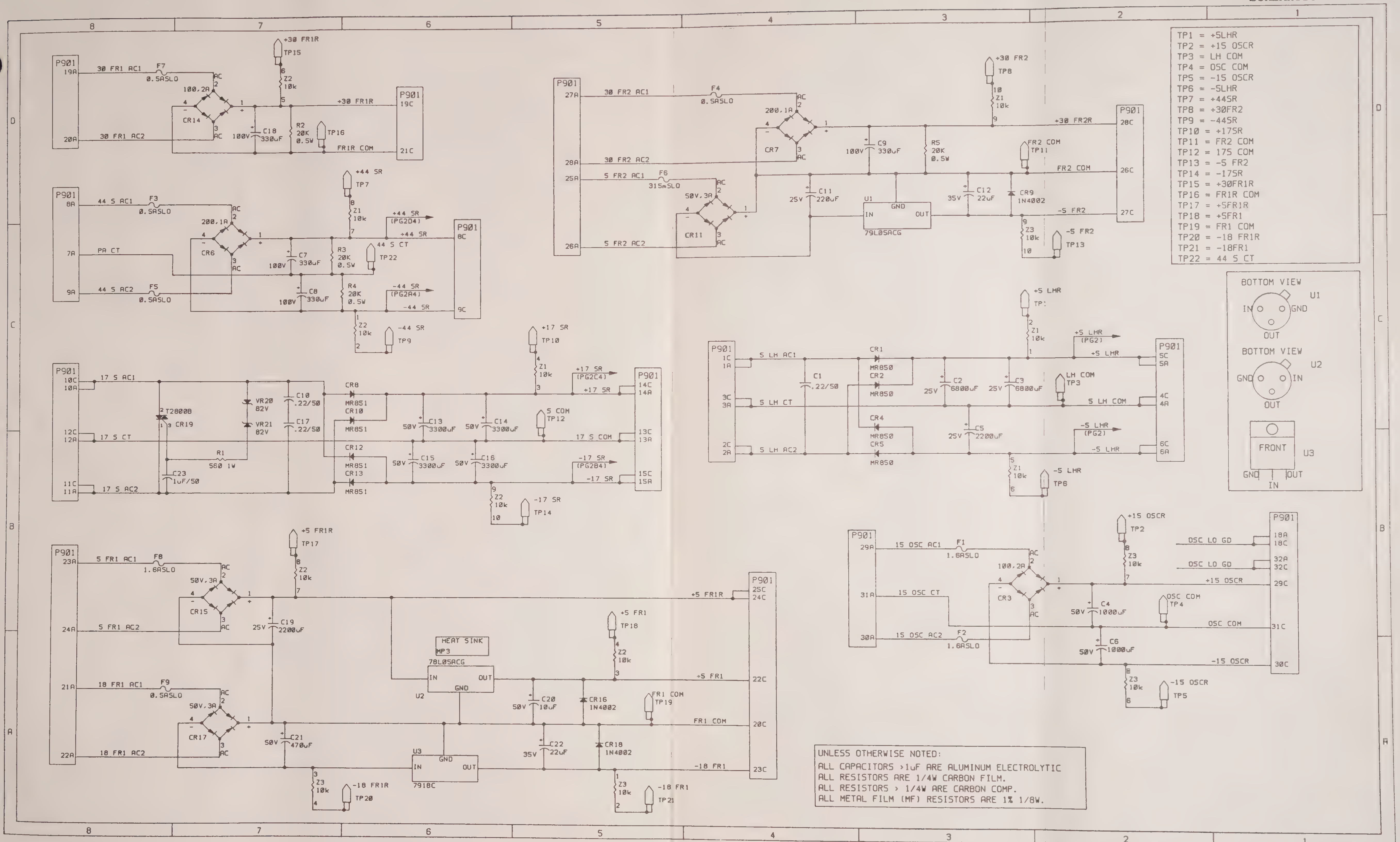

A18
TP4
TP2
TP5
TP11
TP13
TP8
TP21
TP20
TP17
TP18
TP3
TP1
TP6
TP16
TP15
TP7
TP9
TP14
TP22
C16
C15
C14
C3
C202
R5
C12
U1
C22
C11
Z2
C13
C2
CR1
CR16
C20
U3
Z1
C21
C9
R2
CR9
CR18
C4
C6
C19
C18
CR10
CR8
C7
C8
CR2
C5
R3
C17
C10
Z3
F2
F1
CR3
CR7
CR11
CR15
CR17
CR14
CR13
VR20
VR21
CR12
CR6
R1
C1
CR5
CR4
U2
F4
F6
F8
F9
F7
C23
CR19
F5
F3
F201
F202
F203
F204
FILTER
ASSEMBLY
761189
REV
C
B
P901
P902
R215
VR233
TP205
TP206
TP208
TP207
VR213
Q219
R232
R213
C209
C210
TP201
TP204
R222
CR251
R217
U201
R245
R251
R214
R233
R218
Q211
Q201
R253
LO V
Q207
VR218
R247
Z201
Q218
VR227
R249
CR201
CR203
S201
CR209
VR214
C211
C212
R230
R231
R228
R220
R246
R209
VR206
TP209
CR226
Q208
R4
R208
VR211
VR215
VR219
VR202
TP210
VR212
VR216
Q205
R206
R203
Q204
R210
R207
VR207
TP211
TP212
VR228
CR250
CR210
CR208
Q202
R201
R202
CR205
RT1
RT2
VR246
Q206
R212
C207
Q203
R211
CR244
K201
R254
C201
C203
C204
C206
R204
VR245
R255
Q217
R221
R234
VR217
C205
C208
CR240
CR247
CR220
CR218
CR221
R205
R216
VR225
VR229
R235
Q213
VR242
R239
R238
VR238
Q212
R241
VR230
R242
CR222
Q216
CR239
Q209
MP201
MP202
VR247
CR234
CR243
VR237
R237
CR235
CR227
CR224
CR228
R240
R229
R236
R252
VR232
VR226
VR231
Q210
R243
Q214
R244
CR248
Q215

Figure 7-22. A18 Filter/PA Supply PCA


8
7
6
5
4
3
2
1
D
C
B
A
P901
19A
20A
30 FR1 AC1
30 FR1 AC2
F7
0.5ASLO
100,2A
CR14
+30 FR1R
TP15
Z2
10k
C18
330uF
100V
R2
20K
0.5W
TP16
FR1R COM
19C
21C
44 S AC1
44 S AC2
F3
0.5ASLO
F5
0.5ASLO
8A
7A
9A
PA CT
200,1A
CR6
+44 SR
TP7
Z1
10k
+44 SR
(PG2D4)
44 S CT
TP22
C7
330uF
C8
330uF
R3
20K
0.5W
R4
20K
0.5W
-44 SR
(PG2A4)
8C
9C
-44 SR
TP9
17 S AC1
17 S CT
17 S AC2
10C
10A
12C
12A
11C
11A
T2800B
CR19
VR20
82V
VR21
82V
R1
560 1W
C23
1uF/50
C10
.22/50
C17
.22/50
CR8
MR851
CR10
MR851
CR12
MR851
CR13
MR851
C13
3300uF
C14
3300uF
C15
3300uF
C16
3300uF
+17 SR
TP10
+17 SR
(PG2C4)
S COM
TP12
17 S COM
-17 SR
(PG2B4)
-17 SR
TP14
14C
14A
13C
13A
15C
15A
5 FR1 AC1
5 FR1 AC2
23A
24A
F8
1.6ASLO
50V,3A
CR15
+5 FR1R
TP17
C19
2200uF
25V
+5 FR1R
25C
24C
HEAT SINK
MP3
78L05ACG
IN
OUT
GND
U2
+5 FR1
TP18
+5 FR1
22C
C20
10uF
CR16
1N4002
FR1 COM
TP19
FR1 COM
20C
18 FR1 AC1
18 FR1 AC2
21A
22A
F9
0.5ASLO
CR17
C21
470uF
U3
7918C
C22
22uF
35V
CR18
1N4002
-18 FR1
23C
Z3
10k
-18 FR1R
TP20
-18 FR1
TP21
27A
28A
25A
26A
30 FR2 AC1
30 FR2 AC2
F4
0.5ASLO
200,1A
CR7
C9
330uF
R5
20K
0.5W
+30 FR2
TP8
+30 FR2R
20C
FR2 COM
TP11
FR2 COM
26C
5 FR2 AC1
5 FR2 AC2
F6
315mSLO
50V,3A
CR11
C11
220uF
U1
79L05ACG
C12
22uF
CR9
1N4002
-5 FR2
27C
-5 FR2
TP13
+5 LHR
TP1
+5 LHR
(PG2)
+5 LHR
5C
5A
5 LH AC1
5 LH CT
5 LH AC2
1C
1A
3C
3A
2C
2A
C1
.22/50
CR1
MR850
CR2
MR850
CR4
MR850
CR5
MR850
C2
6800uF
C3
6800uF
LH COM
TP3
5 LH COM
4C
4A
C5
2200uF
-5 LHR
(PG2)
-5 LHR
6C
6A
-5 LHR
TP6
BOTTOM VIEW
U1
IN
GND
OUT
BOTTOM VIEW
U2
GND
IN
OUT
FRONT
U3
GND
IN
OUT
15 OSC AC1
15 OSC CT
15 OSC AC2
29A
31A
30A
F1
1.6ASLO
F2
1.6ASLO
100,2A
CR3
+15 OSCR
TP2
OSC LO GD
OSC LO GD
18A
18C
32A
32C
+15 OSCR
29C
C4
1000uF
C6
1000uF
OSC COM
TP4
OSC COM
31C
-15 OSCR
30C
-15 OSCR
TP5

TP1 = +5LHR
TP2 = +15 OSCR
TP3 = LH COM
TP4 = OSC COM
TP5 = -15 OSCR
TP6 = -5LHR
TP7 = +44SR
TP8 = +30FR2
TP9 = -44SR
TP10 = +175R
TP11 = FR2 COM
TP12 = 175 COM
TP13 = -5 FR2
TP14 = -175R
TP15 = +30FR1R
TP16 = FR1R COM
TP17 = +5FR1R
TP18 = +5FR1
TP19 = FR1 COM
TP20 = -18 FR1R
TP21 = -18FR1
TP22 = 44 S CT

UNLESS OTHERWISE NOTED:
ALL CAPACITORS >1uF ARE ALUMINUM ELECTROLYTIC
ALL RESISTORS ARE 1/4W CARBON FILM.
ALL RESISTORS > 1/4W ARE CARBON COMP.
ALL METAL FILM (MF) RESISTORS ARE 1% 1/8W.

FILTER / PA SUPPLY 5700A-1090 1 OF 2 AUG.12,1988

Figure 7-22. A18 Filter/PA Supply PCA (cont)

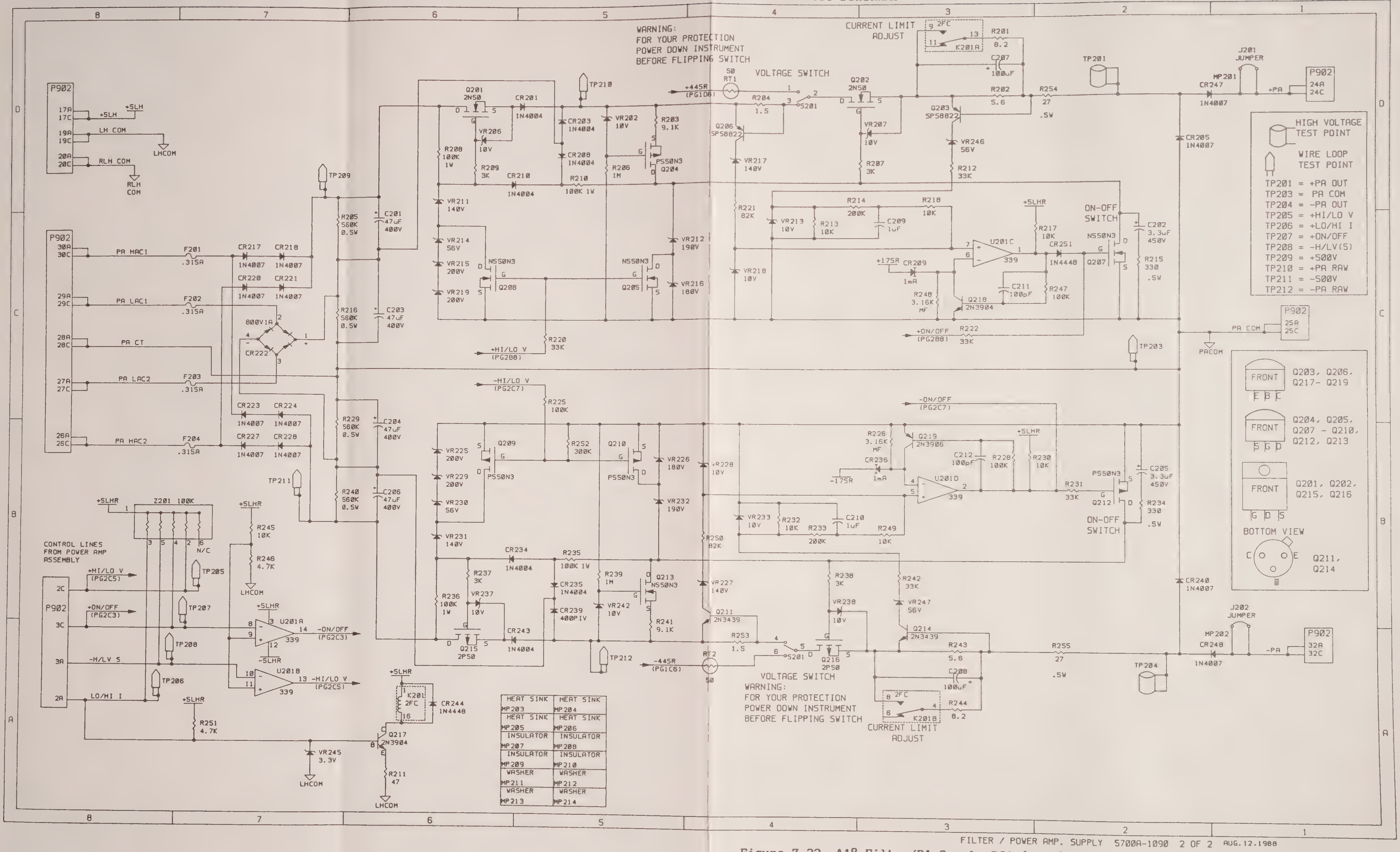

WARNING:
FOR YOUR PROTECTION
POWER DOWN INSTRUMENT
BEFORE FLIPPING SWITCH
CURRENT LIMIT
ADJUST
K201A
2FC
R201
8.2
C207
100uF
R202
5.6
R254
27
.5W
TP201
J201
JUMPER
MP201
CR247
1N4007
+PA
P902
24A
24C
TP210
+445R
(PG1D6)
50
RT1
VOLTAGE SWITCH
R204
1.5
S201
Q202
2N50
Q203
SPS8822
VR207
10V
VR246
56V
R207
3K
R212
33K
Q206
SPS8822
VR217
140V
R221
82K
VR218
10V
P902
17A
17C
+SLH
19A
19C
LH COM
LHCOM
20A
20C
RLH COM
RLH
COM
Q201
2N50
CR201
1N4004
VR206
10V
R208
100K
1W
R209
3K
CR210
1N4004
CR203
1N4004
CR208
1N4004
R210
100K 1W
VR202
10V
R206
1M
R203
9.1K
P550N3
Q204
TP209
R205
560K
0.5W
C201
47uF
400V
VR211
140V
VR214
56V
VR215
200V
VR219
200V
N550N3
Q208
N550N3
Q205
VR212
190V
VR216
180V
P902
30A
30C
PA HAC1
F201
.315A
CR217
1N4007
CR218
1N4007
CR220
1N4007
CR221
1N4007
29A
29C
PA LAC1
F202
.315A
800V1A
CR222
28A
28C
PA CT
27A
27C
PA LAC2
F203
.315A
26A
26C
PA HAC2
F204
.315A
CR223
1N4007
CR224
1N4007
CR227
1N4007
CR228
1N4007
R216
560K
0.5W
C203
47uF
400V
R220
33K
+HI/LO V
(PG2B8)
R214
200K
R218
10K
VR213
10V
R213
10K
C209
1uF
+5LHR
R217
10K
ON-OFF
SWITCH
N550N3
Q207
C202
3.3uF
450V
R215
330
.5W
U201C
339
CR251
1N4448
+17SR
CR209
1mA
R240
3.16K
MF
Q218
2N3904
C211
100pF
R247
100K
+ON/OFF
(PG2B8)
R222
33K
CR205
1N4007
P902
25A
25C
PA COM
PACOM
TP203
HIGH VOLTAGE
TEST POINT
WIRE LOOP
TEST POINT
TP201 = +PA OUT
TP203 = PA COM
TP204 = -PA OUT
TP205 = +HI/LO V
TP206 = +LO/HI I
TP207 = +ON/OFF
TP208 = -H/LV(S)
TP209 = +500V
TP210 = +PA RAW
TP211 = -500V
TP212 = -PA RAW
FRONT
E B C
Q203, Q206,
Q217- Q219
FRONT
S G D
Q204, Q205,
Q207 - Q210,
Q212, Q213
FRONT
G D S
Q201, Q202,
Q215, Q216
BOTTOM VIEW
C
E
Q211,
Q214
-HI/LO V
(PG2C7)
R225
100K
R229
560K
0.5W
C204
47uF
400V
VR225
200V
VR229
200V
VR230
56V
VR231
140V
Q209
P550N3
R252
300K
Q210
P550N3
VR226
180V
VR232
190V
VR228
10V
-ON/OFF
(PG2C7)
R226
3.16K
MF
Q219
2N3906
CR236
1mA
-17SR
C212
100pF
R228
100K
+5LHR
R230
10K
U201D
339
R231
33K
P550N3
Q212
C205
3.3uF
450V
R234
330
.5W
ON-OFF
SWITCH
VR233
10V
R232
10K
R233
200K
C210
1uF
R249
10K
R250
82K
TP211
R240
560K
0.5W
C206
47uF
400V
+5LHR
Z201 100K
N/C
CONTROL LINES
FROM POWER AMP
ASSEMBLY
+HI/LO V
(PG2C5)
TP205
P902
2C
+ON/OFF
(PG2C3)
3C
TP207
TP208
3A
-H/LV S
TP206
2A
LO/HI I
+5LHR
R245
10K
R246
4.7K
LHCOM
+5LHR
U201A
339
-5LHR
-ON/OFF
(PG2C3)
U201B
339
-HI/LO V
(PG2C5)
+5LHR
R251
4.7K
VR245
3.3V
LHCOM
+5LHR
K201
2FC
CR244
1N4448
Q217
2N3904
R211
47
LHCOM
CR234
1N4004
R235
100K 1W
R237
3K
VR237
10V
R236
100K
1W
Q215
2P50
CR243
1N4004
CR235
1N4004
CR239
400PIV
R239
1M
VR242
10V
Q213
N550N3
R241
9.1K
TP212
VR227
140V
Q211
2N3439
R253
1.5
-445R
(PG1C6)
RT2
50
S201
R238
3K
VR238
10V
Q216
2P50
R242
33K
VR247
56V
Q214
2N3439
R243
5.6
C208
100uF
R244
8.2
K201B
2FC
CURRENT LIMIT
ADJUST
VOLTAGE SWITCH
WARNING:
FOR YOUR PROTECTION
POWER DOWN INSTRUMENT
BEFORE FLIPPING SWITCH
R255
27
.5W
TP204
CR240
1N4007
J202
JUMPER
MP202
CR248
1N4007
-PA
P902
32A
32C
HEAT SINK MP203
HEAT SINK MP204
HEAT SINK MP205
HEAT SINK MP206
INSULATOR MP207
INSULATOR MP208
INSULATOR MP209
INSULATOR MP210
WASHER MP211
WASHER MP212
WASHER MP213
WASHER MP214
8
7
6
5
4
3
2
1
D
C
B
A
FILTER / POWER AMP. SUPPLY S700A-1090 2 OF 2 AUG.12,1988

Figure 7-22. A18 Filter/PA Supply PCA (cont)

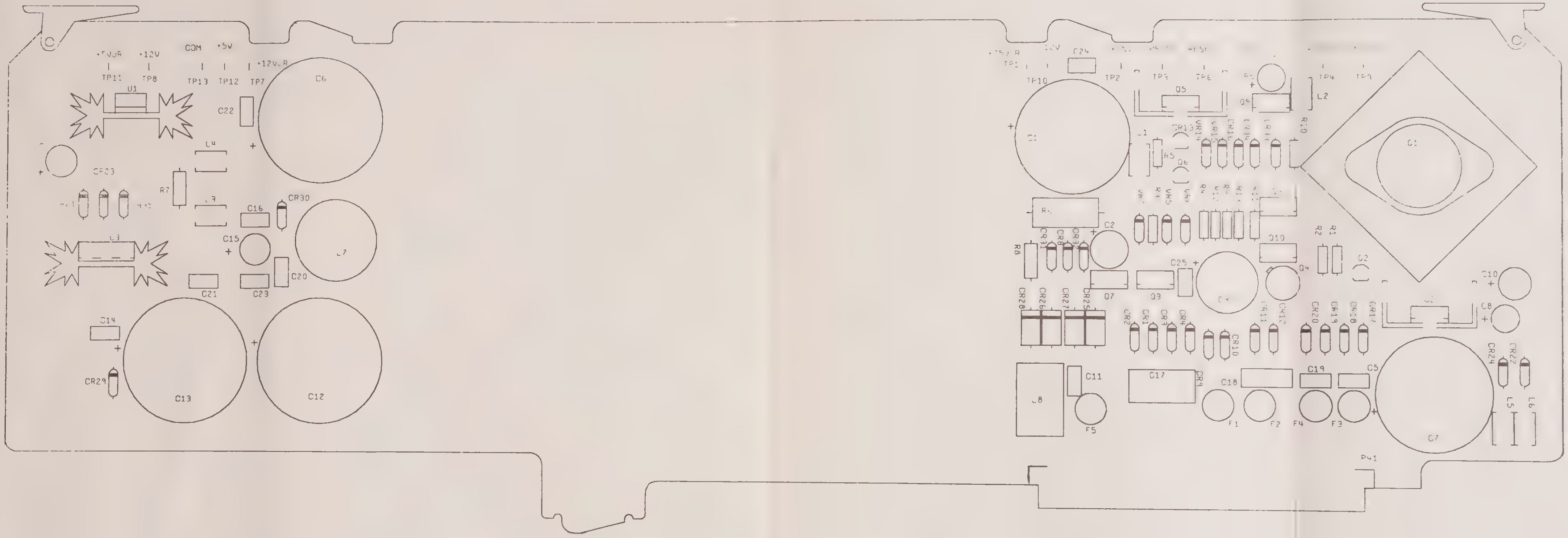

+12V
COM
+5V
TP11
TP8
TP13
TP12
TP7
U1
C6
C22
CR23
R7
CR30
C16
C15
C20
C21
C23
C14
CR29
C13
C12
C24
TP10
TP2
TP4
TP9
Q5
L2
R10
R5
Q6
C1
R8
CR31
CR8
C2
Q10
R2
R1
C25
Q4
Q7
Q3
C10
C8
CR28
CR26
CR27
CR25
CR2
CR1
CR3
CR4
CR10
CR11
CR12
CR20
CR19
CR18
CR17
CR24
CR22
C11
C17
CR9
C18
C19
C5
F5
F1
F2
F4
F3
C7
L5
L6
P41

Figure 7-23. A19 Digital Power Supply PCA

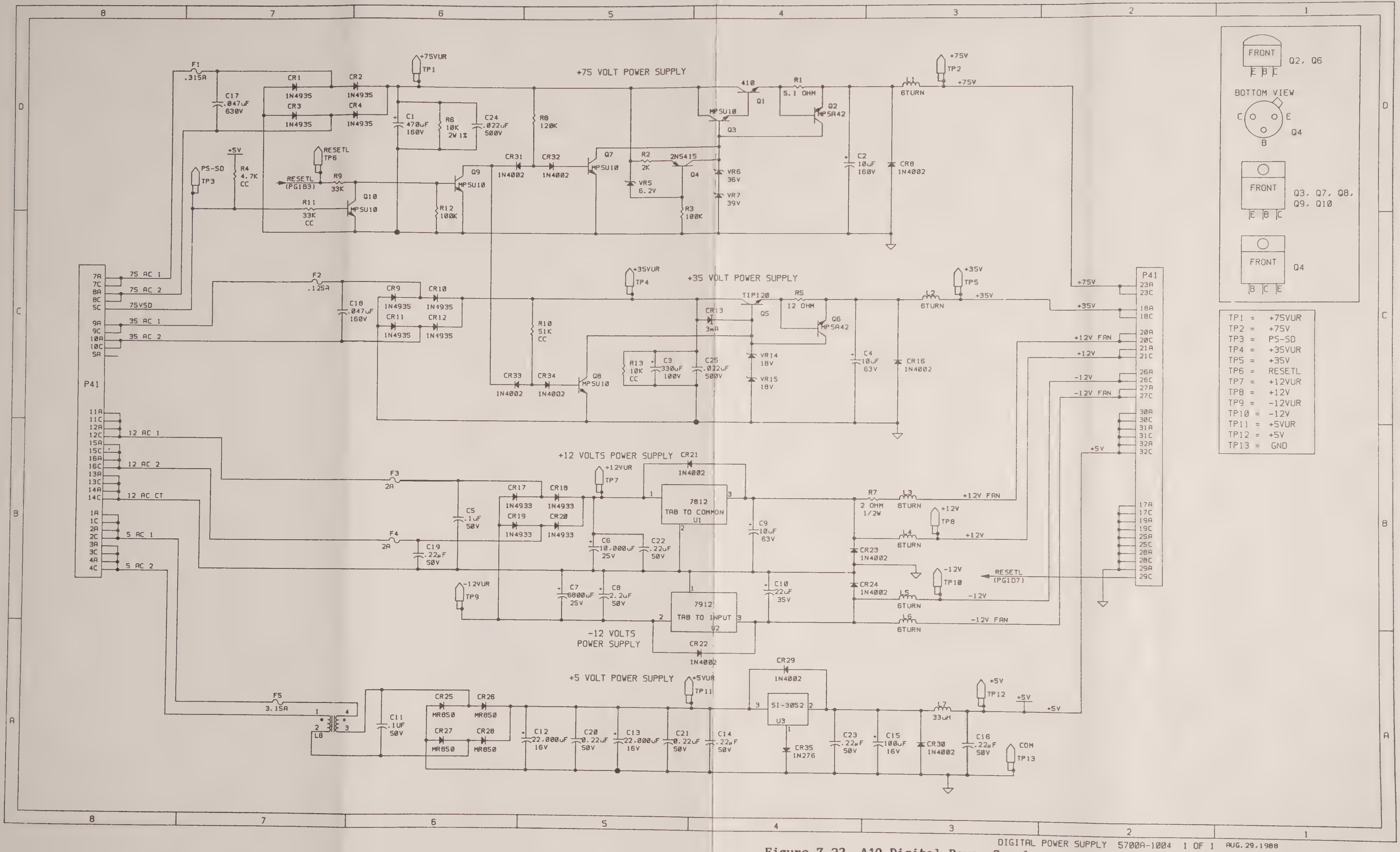

+75 VOLT POWER SUPPLY
+35 VOLT POWER SUPPLY
+12 VOLTS POWER SUPPLY
-12 VOLTS POWER SUPPLY
+5 VOLT POWER SUPPLY
P41
75 AC 1
75 AC 2
75VSD
35 AC 1
35 AC 2
12 AC 1
12 AC 2
12 AC CT
5 AC 1
5 AC 2
F1 .315A
F2 .125A
F3 2A
F4 2A
F5 3.15A
C17 .047uF 630V
C18 .047uF 160V
CR1 1N4935
CR2 1N4935
CR3 1N4935
CR4 1N4935
CR9 1N4935
CR10 1N4935
CR11 1N4935
CR12 1N4935
C1 470uF 160V
R6 10K 2W 1%
C24 .022uF 500V
R8 120K
+75VUR TP1
+75V TP2
+75V
L1 6TURN
R1 5.1 OHM
Q1 410
Q2 MPSA42
Q3 MPSU10
Q7 MPSU10
Q9 MPSU10
Q10 MPSU10
Q4 2N5415
R2 2K
VR5 6.2V
VR6 36V
VR7 39V
R3 100K
C2 10uF 160V
CR8 1N4002
CR31 1N4002
CR32 1N4002
R12 100K
+5V
R4 4.7K CC
PS-SD TP3
RESETL TP6
RESETL (PG183)
R9 33K
R11 33K CC
+35VUR TP4
+35V TP5
+35V
TIP120 Q5
R5 12 OHM
Q6 MPSA42
L2 6TURN
CR13 3mA
R10 51K CC
R13 10K CC
C3 330uF 100V
C25 .022uF 500V
VR14 18V
VR15 18V
C4 10uF 63V
CR16 1N4002
CR33 1N4002
CR34 1N4002
Q8 MPSU10
C5 .1uF 50V
C19 .22uF 50V
CR17 1N4933
CR18 1N4933
CR19 1N4933
CR20 1N4933
+12VUR TP7
CR21 1N4002
7812 TAB TO COMMON U1
C6 10,000uF 25V
C22 .22uF 50V
C9 10uF 63V
R7 2 OHM 1/2W
L3 6TURN
L4 6TURN
+12V FAN
+12V TP8
+12V
CR23 1N4002
CR24 1N4002
-12V TP10
-12V
RESETL (PG1D7)
L5 6TURN
L6 6TURN
-12V FAN
-12VUR TP9
C7 6800uF 25V
C8 2.2uF 50V
7912 TAB TO INPUT U2
C10 22uF 35V
CR22 1N4002
+5VUR TP11
L8
C11 .1UF 50V
CR25 MR850
CR26 MR850
CR27 MR850
CR28 MR850
C12 22,000uF 16V
C20 0.22uF 50V
C13 22,000uF 16V
C21 0.22uF 50V
C14 .22uF 50V
CR29 1N4002
SI-3052 U3
CR35 1N276
C23 .22uF 50V
C15 100uF 16V
CR30 1N4002
L7 33uH
+5V TP12
C16 .22uF 50V
COM TP13
+5V
7A 7C 8A 8C 5C 9A 9C 10A 10C 5A
11A 11C 12A 12C 15A 15C 16A 16C 13A 13C 14A 14C
1A 1C 2A 2C 3A 3C 4A 4C
23A 23C 18A 18C 20A 20C 21A 21C 26A 26C 27A 27C
30A 30C 31A 31C 32A 32C
17A 17C 19A 19C 25A 25C 28A 28C 29A 29C
FRONT Q2, Q6 E B C
BOTTOM VIEW C E B Q4
FRONT Q3, Q7, Q8, Q9, Q10 E B C
FRONT Q4 B C E
TP1 = +75VUR
TP2 = +75V
TP3 = PS-SD
TP4 = +35VUR
TP5 = +35V
TP6 = RESETL
TP7 = +12VUR
TP8 = +12V
TP9 = -12VUR
TP10 = -12V
TP11 = +5VUR
TP12 = +5V
TP13 = GND
8 7 6 5 4 3 2 1
D C B A
DIGITAL POWER SUPPLY 5700A-1004 1 OF 1 AUG.29,1988

Figure 7-23. A19 Digital Power Supply PCA (cont)

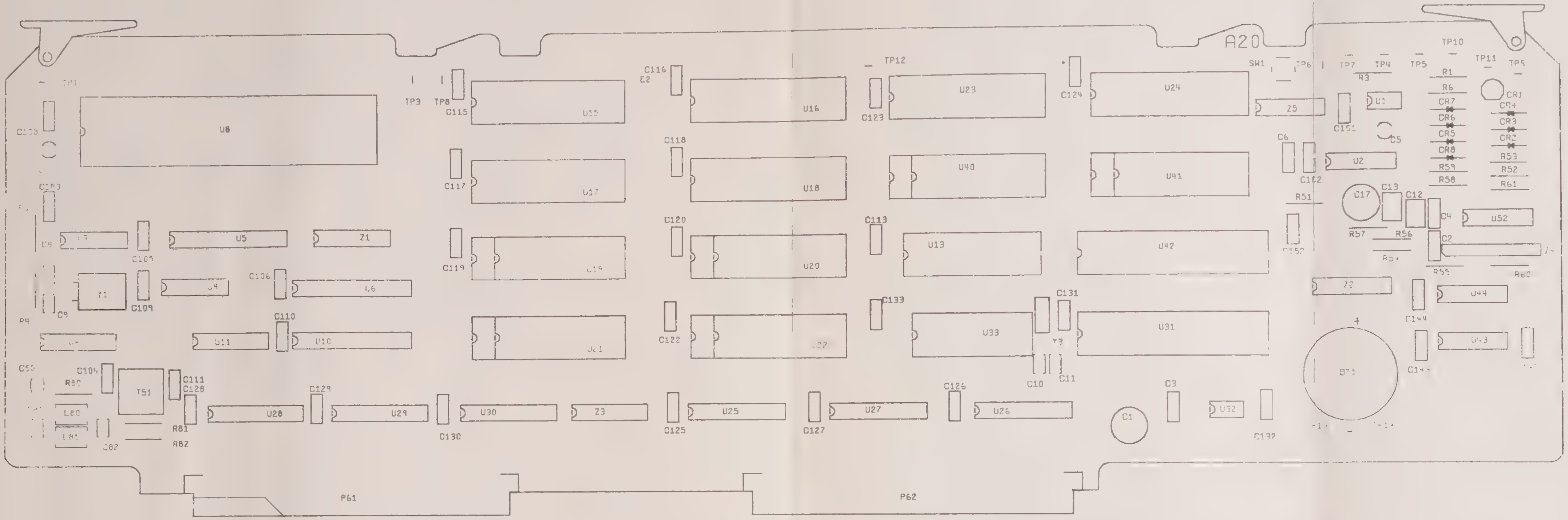
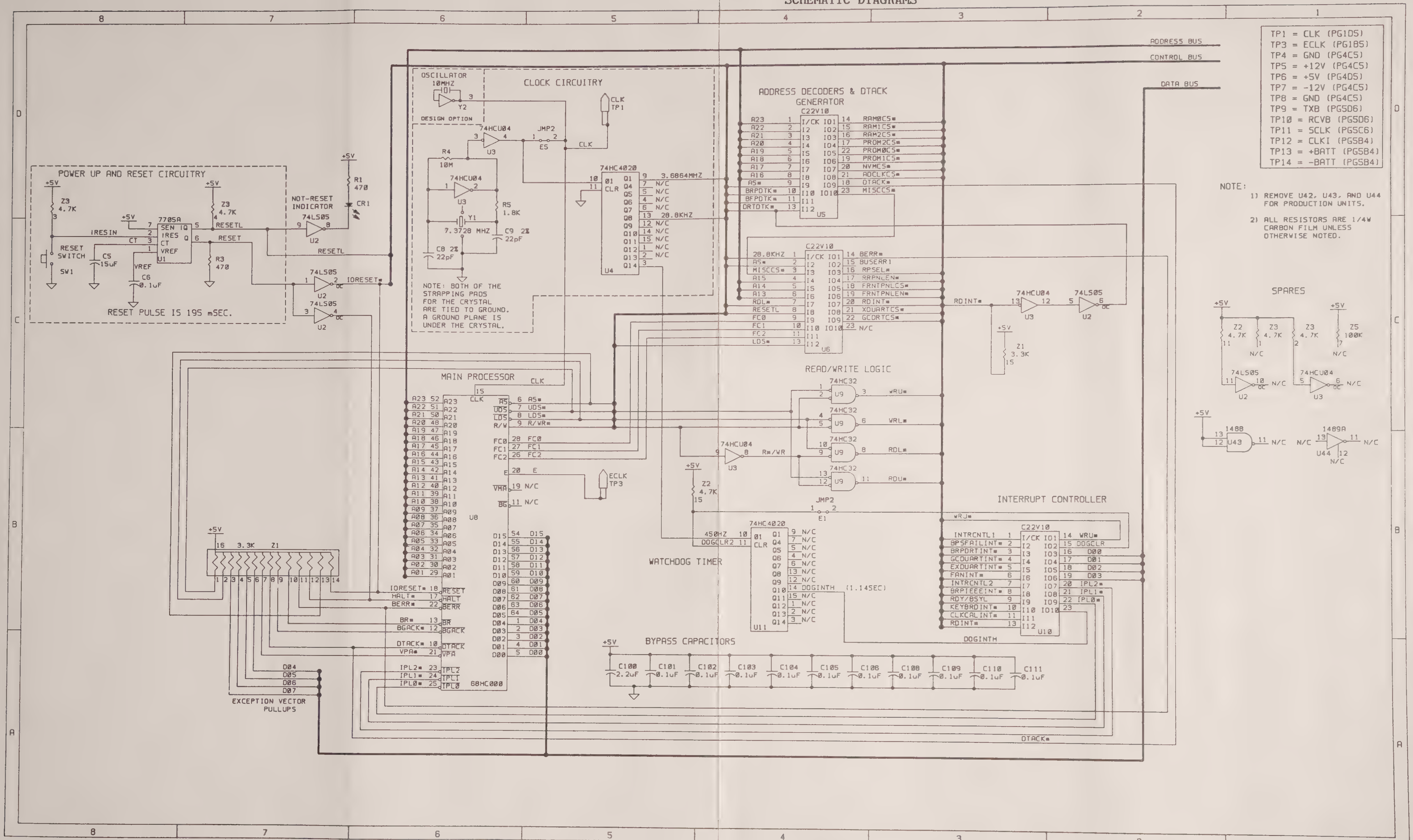

A20
TP3
TP8
TP12
TP10
TP11
TP7
TP4
TP5
TP6
SW1
E2
U8
C115
U15
C116
U16
C123
U23
C124
U24
Z5
C151
U1
R3
R1
R6
CR7
CR6
CR5
CR8
R59
R58
CR1
CR4
CR3
CR2
R53
R52
R61
C117
U17
C118
U18
U40
U41
C6
C152
U2
C5
C103
C105
U5
Z1
C119
U19
C120
U20
C113
U13
U42
R51
C17
C13
C12
C4
U52
R57
R56
C2
R55
R62
T1
C109
U9
C106
U6
C110
U11
U10
U21
C122
U22
C133
U33
C131
Y3
U31
Z2
U44
C144
U43
P4
C9
C10
C11
C53
C104
R80
T51
C111
C128
L80
R81
R82
C87
C129
U28
U29
C130
U30
Z3
C125
U25
C127
U27
C126
U26
C3
C1
U32
C132
BT1
+
P61
P62

Figure 7-24. A20 CPU PCA


POWER UP AND RESET CIRCUITRY
RESET SWITCH
SW1
RESET PULSE IS 195 mSEC.
NOT-RESET INDICATOR
OSCILLATOR 10MHZ
DESIGN OPTION
CLOCK CIRCUITRY
CLK TP1
7.3728 MHZ
NOTE: BOTH OF THE STRAPPING PADS FOR THE CRYSTAL ARE TIED TO GROUND. A GROUND PLANE IS UNDER THE CRYSTAL.
ADDRESS DECODERS & DTACK GENERATOR
ADDRESS BUS
CONTROL BUS
DATA BUS
TP1 = CLK (PG1D5)
TP3 = ECLK (PG1B5)
TP4 = GND (PG4C5)
TP5 = +12V (PG4C5)
TP6 = +5V (PG4D5)
TP7 = -12V (PG4C5)
TP8 = GND (PG4C5)
TP9 = TXB (PG5D6)
TP10 = RCVB (PG5D6)
TP11 = SCLK (PG5C6)
TP12 = CLKI (PG5B4)
TP13 = +BATT (PG5B4)
TP14 = -BATT (PG5B4)
NOTE:
1) REMOVE U42, U43, AND U44 FOR PRODUCTION UNITS.
2) ALL RESISTORS ARE 1/4W CARBON FILM UNLESS OTHERWISE NOTED.
SPARES
MAIN PROCESSOR
68HC000
READ/WRITE LOGIC
ECLK TP3
WATCHDOG TIMER
INTERRUPT CONTROLLER
BYPASS CAPACITORS
EXCEPTION VECTOR PULLUPS

CPU 5700A-1006 1 OF 5 AUG.8.1988

Figure 7-24. A20 CPU PCA (cont)

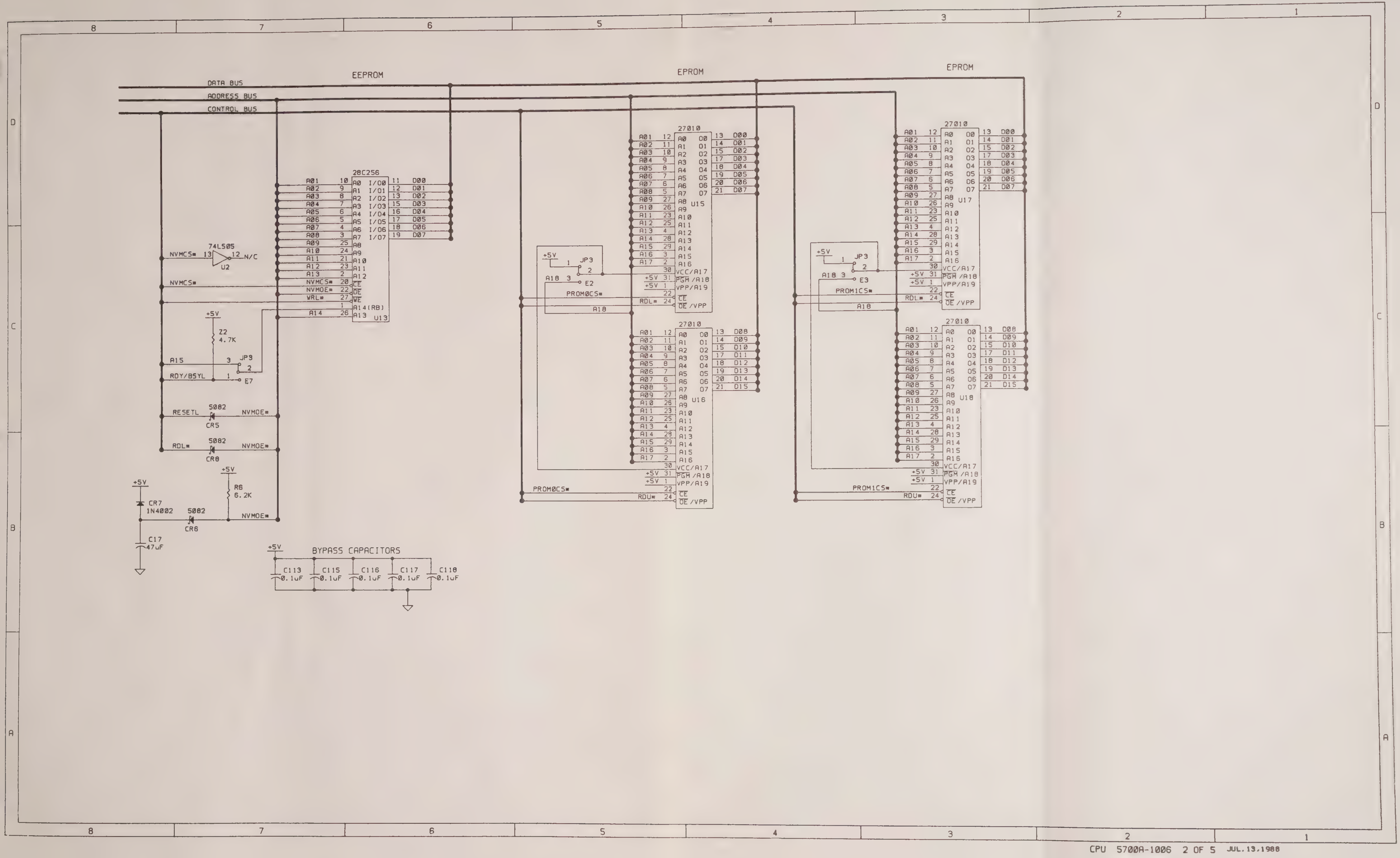

DATA BUS
ADDRESS BUS
CONTROL BUS
EEPROM
EPROM
EPROM
28C256
U13
27010
U15
U16
U17
U18
74LS05
U2
NVMCS*
N/C
NVMOE*
WRL*
A14
A14(A8)
A15
RDY/BSYL
JP9
E7
+5V
Z2
4.7K
RESETL
5082
CR5
RDL*
CR8
CR7
1N4002
CR6
R6
6.2K
C17
47uF
BYPASS CAPACITORS
C113
C115
C116
C117
C118
0.1uF
JP3
E2
E3
A18
PROM0CS*
PROM1CS*
RDU*
VCC/A17
PGM/A18
VPP/A19
CE
OE/VPP
8
7
6
5
4
3
2
1
A
B
C
D
CPU 5700A-1006 2 OF 5 JUL.13.1988

Figure 7-24. A20 CPU PCA (cont)

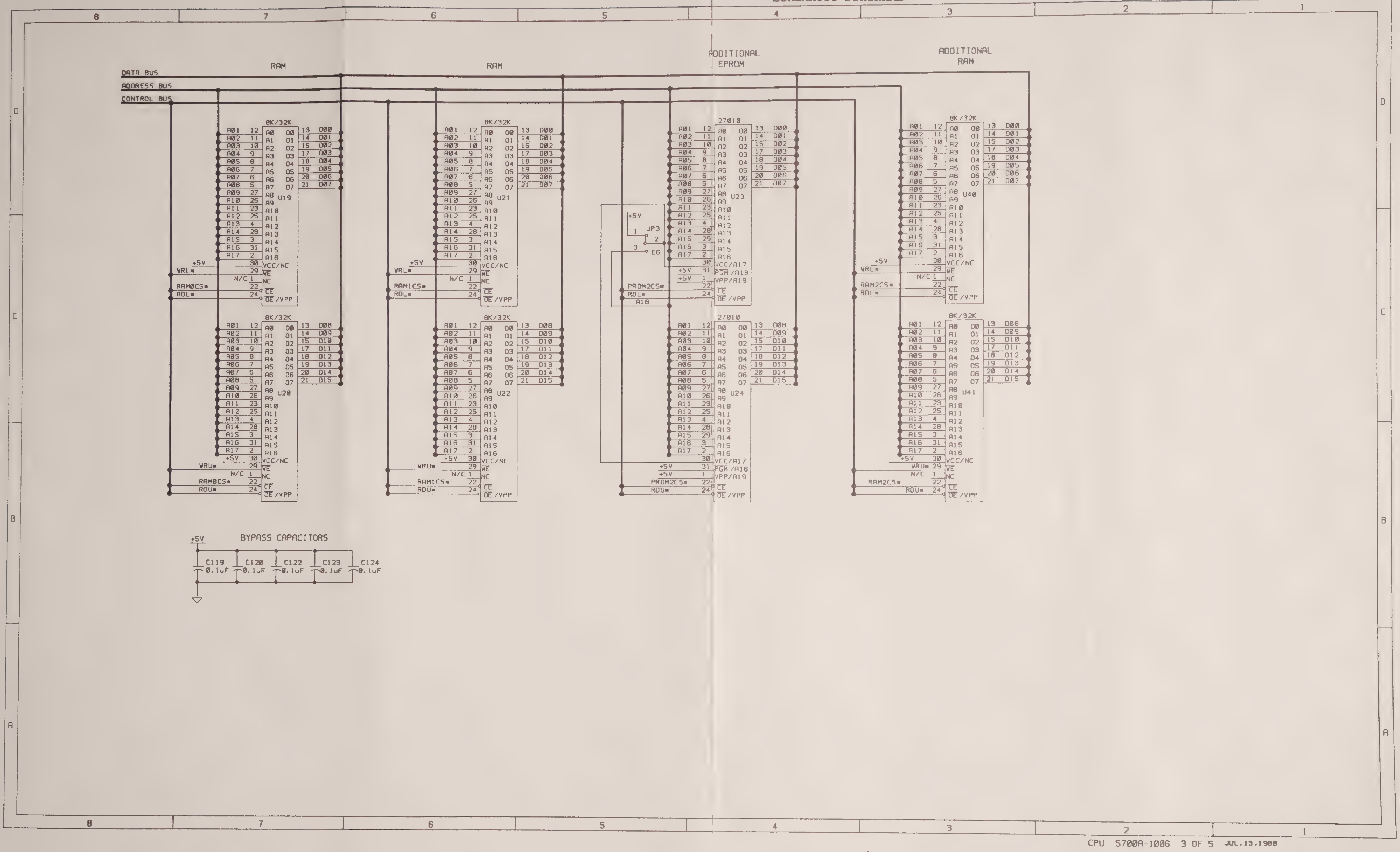
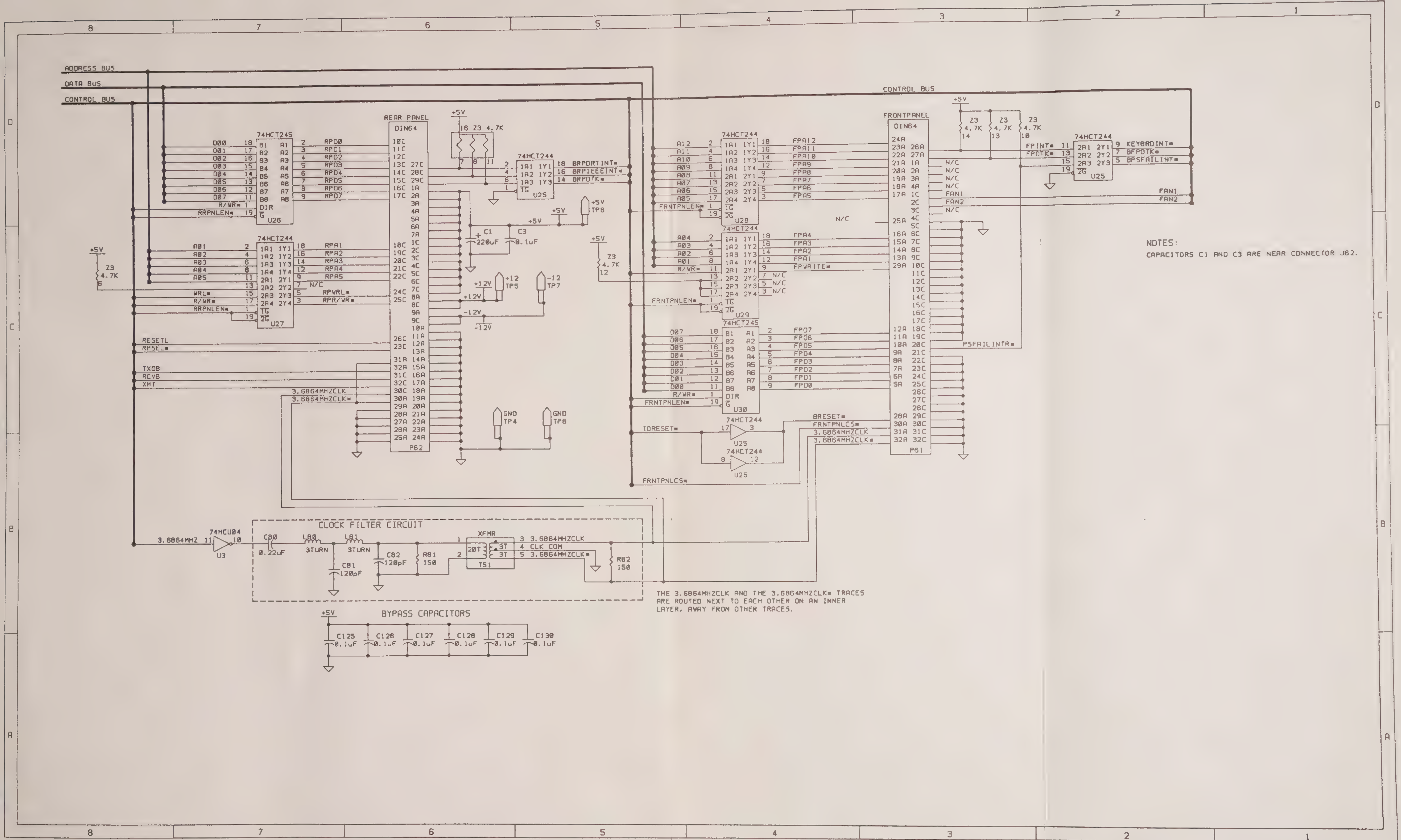

DATA BUS
ADDRESS BUS
CONTROL BUS
RAM
RAM
ADDITIONAL EPROM
ADDITIONAL RAM
8K/32K
U19
U20
U21
U22
U40
U41
27010
U23
U24
A0 … A16
O0 … O7
D00 … D15
A01 … A17
VCC/NC
WE
NC
CE
OE/VPP
VCC/A17
PGM/A18
VPP/A19
+5V
WRL=
WRU=
RDL=
RDU=
RAM0CS=
RAM1CS=
RAM2CS=
PROM2CS=
N/C
A18
JP3
E6
BYPASS CAPACITORS
C119 0.1uF
C120 0.1uF
C122 0.1uF
C123 0.1uF
C124 0.1uF
CPU 5700A-1006 3 OF 5 JUL.13.1988

Figure 7-24. A20 CPU PCA (cont)


ADDRESS BUS
DATA BUS
CONTROL BUS
74HCT245
U26
74HCT244
U27
REAR PANEL
DIN64
P62
74HCT244
U25
BRPORTINT=
BRPIEEEINT=
BRPDTK=
Z3 4.7K
+5V
TP6
C1 220uF
C3 0.1uF
+12V TP5
-12V TP7
GND TP4
GND TP8
RPD0
RPD1
RPD2
RPD3
RPD4
RPD5
RPD6
RPD7
RPA1
RPA2
RPA3
RPA4
RPA5
RPWRL=
RPR/WR=
WRL=
R/WR=
RRPNLEN=
RESETL
RPSEL=
TXDB
RCVB
XMT
3.6864MHZCLK
3.6864MHZCLK=
CONTROL BUS
FRONTPANEL
DIN64
P61
74HCT244
U28
U29
74HCT245
U30
FPA12
FPA11
FPA10
FPA9
FPA8
FPA7
FPA6
FPA5
FPA4
FPA3
FPA2
FPA1
FPWRITE=
FPD7
FPD6
FPD5
FPD4
FPD3
FPD2
FPD1
FPD0
FRNTPNLEN=
N/C
FPINT=
FPDTK=
KEYBRDINT=
BFPDTK=
BPSFAILINT=
FAN1
FAN2
PSFAILINTR=
BRESET=
FRNTPNLCS=
IORESET=
CLOCK FILTER CIRCUIT
74HCU04
U3
3.6864MHZ
C80 0.22uF
L80 3TURN
L81 3TURN
C81 120pF
C82 120pF
R81 150
XFMR
20T
3T
T51
3 3.6864MHZCLK
4 CLK COM
5 3.6864MHZCLK=
R82 150
BYPASS CAPACITORS
C125 0.1uF
C126 0.1uF
C127 0.1uF
C128 0.1uF
C129 0.1uF
C130 0.1uF
THE 3.6864MHZCLK AND THE 3.6864MHZCLK= TRACES ARE ROUTED NEXT TO EACH OTHER ON AN INNER LAYER, AWAY FROM OTHER TRACES.
NOTES:
CAPACITORS C1 AND C3 ARE NEAR CONNECTOR J62.

CPU 5700A-1006 4 OF 5 AUG.8,1988

Figure 7-24. A20 CPU PCA (cont)

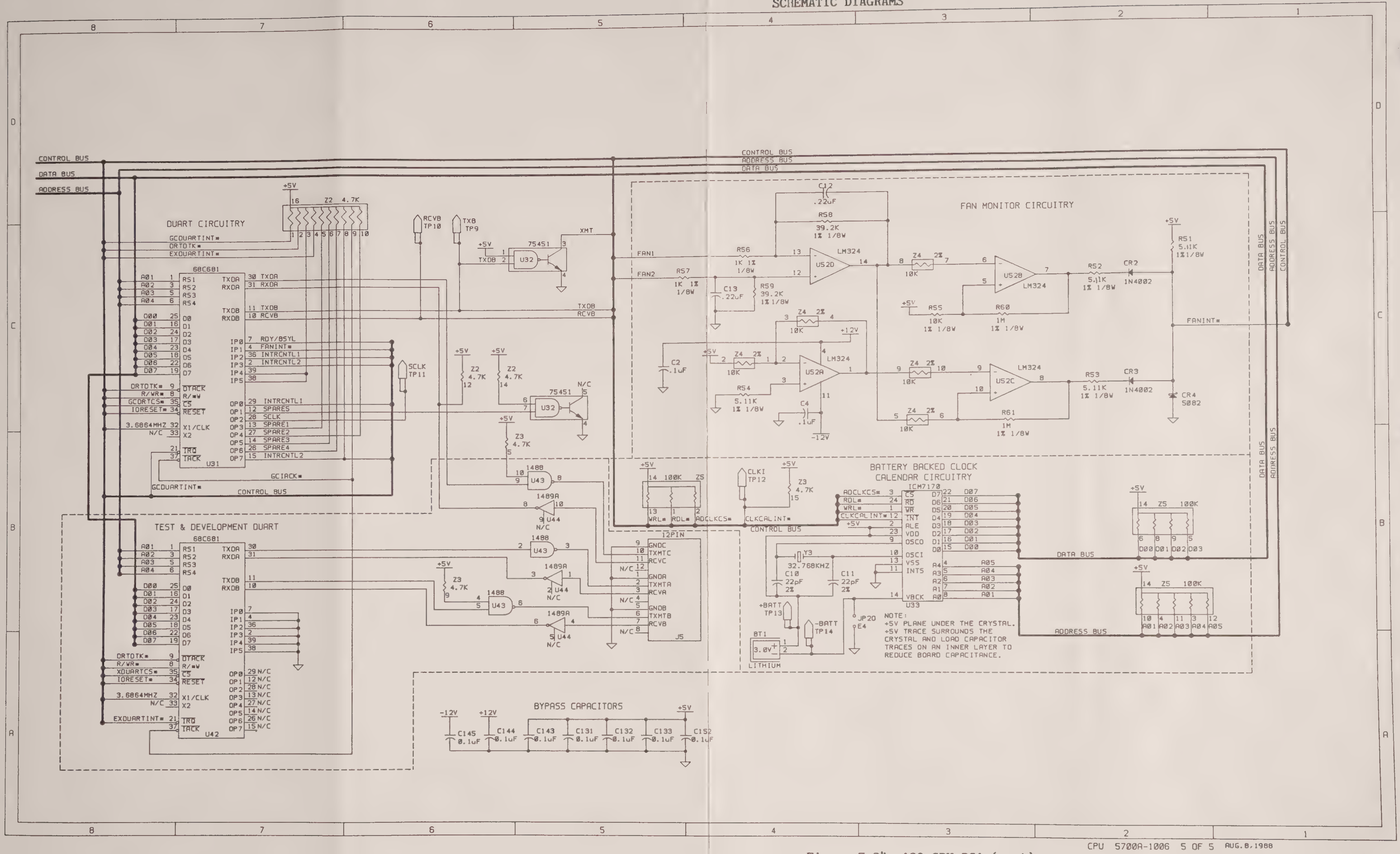

CONTROL BUS
DATA BUS
ADDRESS BUS
DUART CIRCUITRY
+5V
Z2 4.7K
GCDUARTINT*
DRTDTK*
EXDUARTINT*
68C681
RS1 RS2 RS3 RS4
A01 A02 A03 A04
D00 D01 D02 D03 D04 D05 D06 D07
TXDA RXDA TXDB RXDB
30 TXDA
31 RXDA
11 TXDB
10 RCVB
IP0 IP1 IP2 IP3 IP4 IP5
7 RDY/BSYL
4 FANINT*
36 INTRCNTL1
2 INTRCNTL2
DTACK R/*W CS RESET
DRTDTK* R/WR* GCDRTCS* IORESET*
3.6864MHZ X1/CLK
N/C X2
IRQ IACK
U31
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7
29 INTRCNTL1
12 SPARE5
28 SCLK
13 SPARE1
27 SPARE2
14 SPARE3
26 SPARE4
15 INTRCNTL2
GCIACK*
GCDUARTINT*
CONTROL BUS
RCVB TP10
TXB TP9
75451
U32
XMT
TXDB
RCVB
SCLK TP11
Z2 4.7K
Z3 4.7K
1488
U43
1489A
U44
N/C
TEST & DEVELOPMENT DUART
68C681
XDUARTCS*
EXDUARTINT*
U42
29 N/C
12 N/C
28 N/C
13 N/C
27 N/C
14 N/C
26 N/C
15 N/C
12PIN
GNDC TXMTC RCVC
GNDA TXMTA RCVA
GNDB TXMTB RCVB
J5
BYPASS CAPACITORS
-12V +12V +5V
C145 0.1uF
C144 0.1uF
C143 0.1uF
C131 0.1uF
C132 0.1uF
C133 0.1uF
C152 0.1uF
CONTROL BUS
ADDRESS BUS
DATA BUS
FAN MONITOR CIRCUITRY
C12 .22uF
R58 39.2K 1% 1/8W
FAN1
FAN2
R56 1K 1% 1/8W
R57 1K 1% 1/8W
C13 .22uF
R59 39.2K 1% 1/8W
LM324
U52D
U52B
U52A
U52C
Z4 2% 10K
+12V
C2 .1uF
R54 5.11K 1% 1/8W
C4 .1uF
-12V
R55 10K 1% 1/8W
R60 1M 1% 1/8W
R61 1M 1% 1/8W
R52 5.11K 1% 1/8W
R53 5.11K 1% 1/8W
CR2 1N4002
CR3 1N4002
CR4 5082
R51 5.11K 1% 1/8W
FANINT*
BATTERY BACKED CLOCK CALENDAR CIRCUITRY
14 100K Z5
WRL* RDL* ADCLKCS*
CLKI TP12
Z3 4.7K
CLKCALINT*
CONTROL BUS
ICM7170
ADCLKCS* RDL* WRL* CLKCALINT*
CS RD WR INT ALE VDD OSCO OSCI VSS INTS VBCK
D07 D06 D05 D04 D03 D02 D01 D00
A4 A3 A2 A1 A0
A05 A04 A03 A02 A01
U33
Y3 32.768KHZ
C10 22pF 2%
C11 22pF 2%
+BATT TP13
-BATT TP14
BT1 3.0V LITHIUM
JP20 E4
NOTE:
+5V PLANE UNDER THE CRYSTAL.
+5V TRACE SURROUNDS THE CRYSTAL AND LOAD CAPACITOR TRACES ON AN INNER LAYER TO REDUCE BOARD CAPACITANCE.
14 Z5 100K
D00 D01 D02 D03
A01 A02 A03 A04 A05
DATA BUS
ADDRESS BUS
CONTROL BUS
8 7 6 5 4 3 2 1
D C B A
CPU 5700A-1006 5 OF 5 AUG.8,1988

Figure 7-24. A20 CPU PCA (cont)

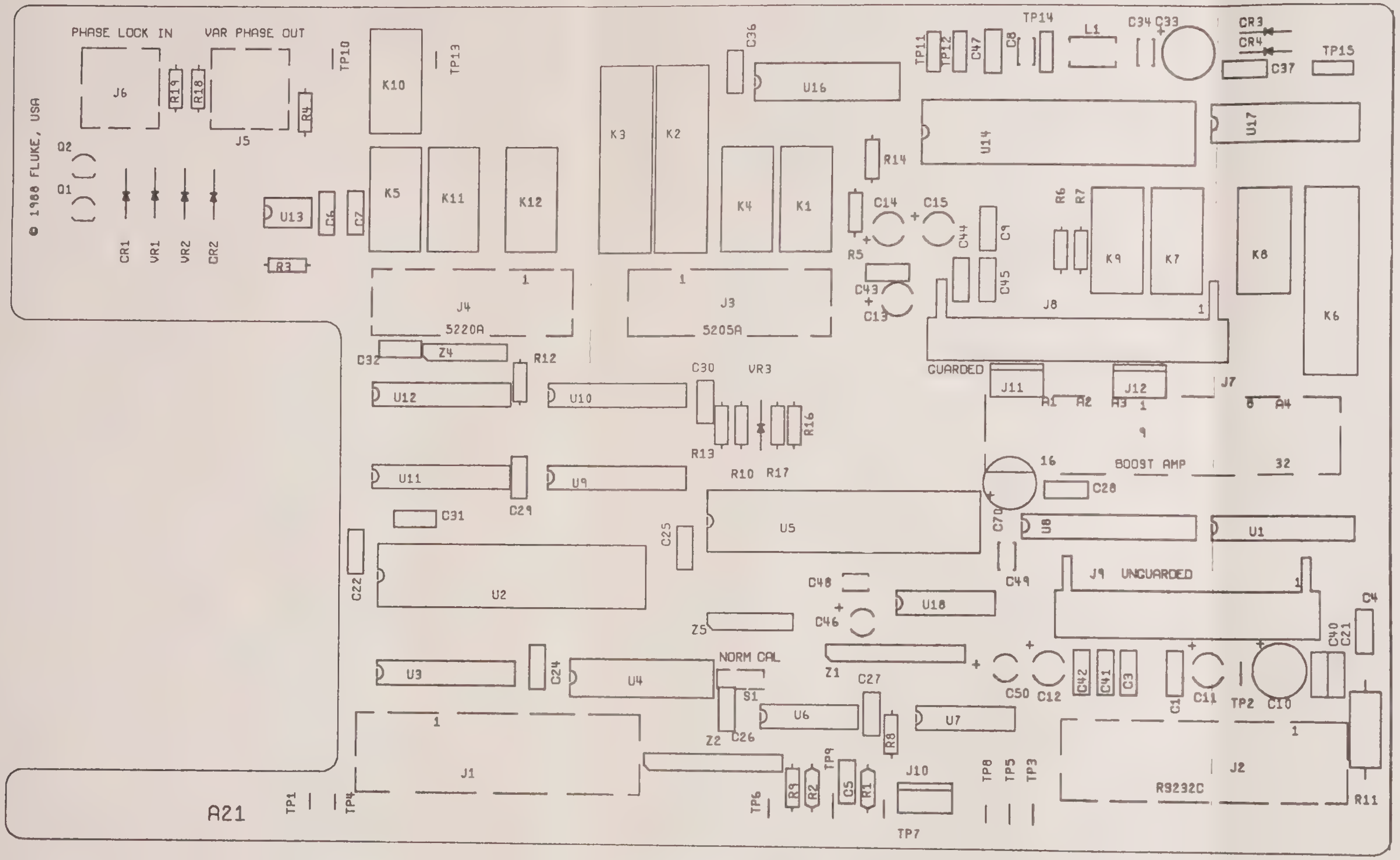
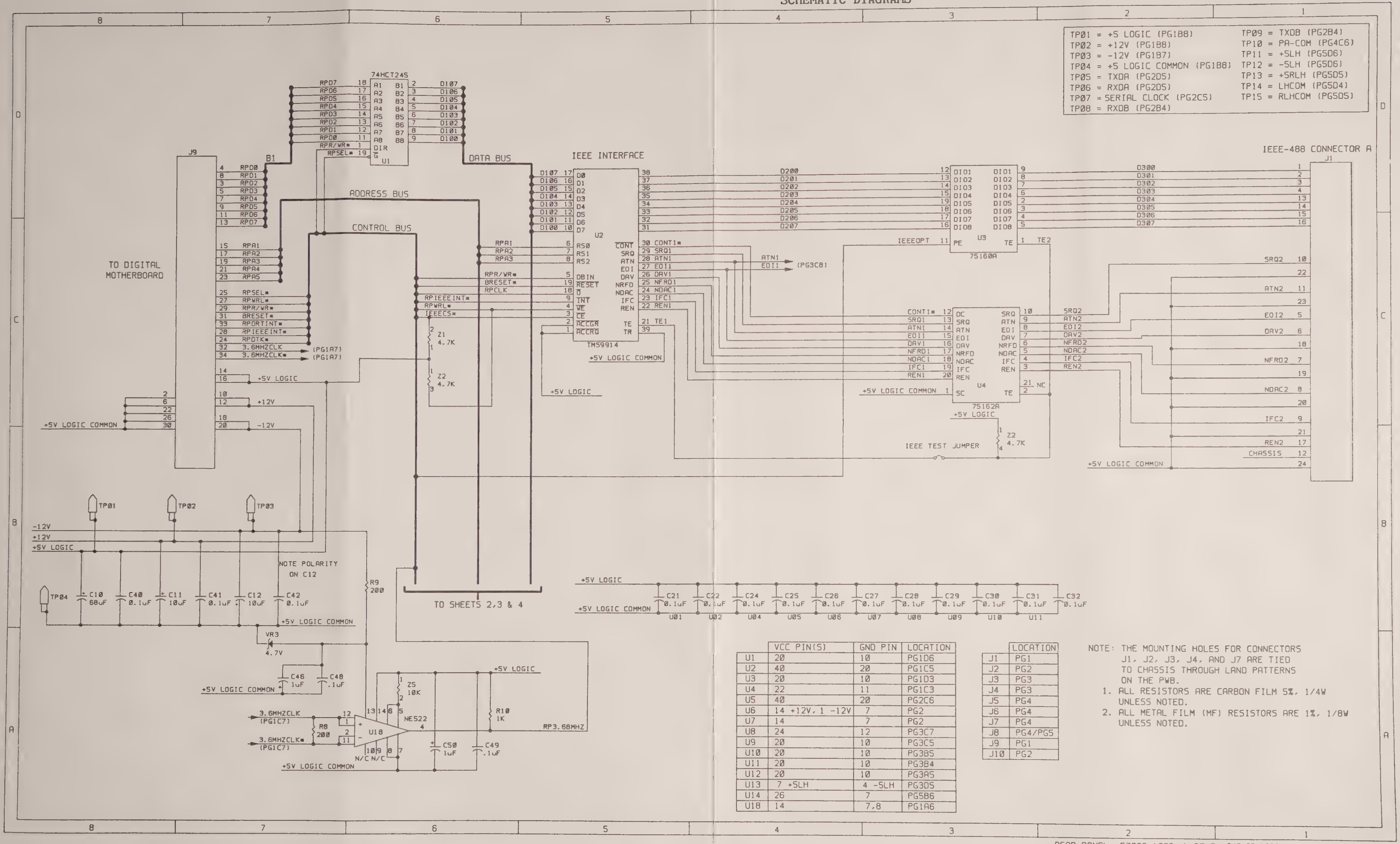

PHASE LOCK IN
VAR PHASE OUT
J6
R19
R18
J5
R4
TP10
K10
TP13
K3
K2
C36
U16
TP11
TP12
C47
C8
TP14
L1
C34
C33
CR3
CR4
C37
TP15
U14
U17
© 1988 FLUKE, USA
Q2
Q1
CR1
VR1
VR2
CR2
U13
C6
C7
R3
K5
K11
K12
K4
K1
R14
C14
C15
R5
C44
C9
R6
R7
K9
K7
K8
K6
C43
C13
C45
J8
J4
5220A
J3
5205A
1
C32
Z4
R12
U12
U10
C30
VR3
R13
R16
R10
R17
GUARDED
J11
J12
J7
A1
A2
A3
A4
BOOST AMP
16
32
9
U11
C29
U9
C31
C28
U5
C70
U8
U1
C25
C22
U2
C48
C49
J9 UNGUARDED
U18
C46
Z5
C4
C40
C21
NORM CAL
Z1
C27
C50
C12
C42
C41
C3
C1
C11
TP2
C10
U3
C24
U4
S1
U6
U7
R8
Z2
C26
J1
J10
TP9
TP8
TP5
TP3
J2
RS232C
R11
A21
TP1
TP4
TP6
R9
R2
C5
R1
TP7

Figure 7-25. A21 Rear Panel PCA


74HCT245
U1
J9
B1
TO DIGITAL MOTHERBOARD
DATA BUS
ADDRESS BUS
CONTROL BUS
IEEE INTERFACE
U2
TMS9914
U3
75160A
U4
75162A
IEEE-488 CONNECTOR A
J1
IEEE TEST JUMPER
TO SHEETS 2,3 & 4
NOTE POLARITY ON C12
VR3 4.7V
U18
NE522
RP3.68MHZ
3.6MHZCLK (PG1C7)
ATN1 EOI1 (PG3C8)
+5V LOGIC
+5V LOGIC COMMON
+12V
-12V
TP01
TP02
TP03
TP04

TP01 = +5 LOGIC (PG1B8)
TP02 = +12V (PG1B8)
TP03 = -12V (PG1B7)
TP04 = +5 LOGIC COMMON (PG1B8)
TP05 = TXDA (PG2D5)
TP06 = RXDA (PG2D5)
TP07 = SERIAL CLOCK (PG2C5)
TP08 = RXDB (PG2B4)
TP09 = TXDB (PG2B4)
TP10 = PA-COM (PG4C6)
TP11 = +5LH (PG5D6)
TP12 = -5LH (PG5D6)
TP13 = +5RLH (PG5D5)
TP14 = LHCOM (PG5D4)
TP15 = RLHCOM (PG5D5)

	VCC PIN(S)	GND PIN	LOCATION
U1	20	10	PG1D6
U2	40	20	PG1C5
U3	20	10	PG1D3
U4	22	11	PG1C3
U5	40	20	PG2C6
U6	14 +12V, 1 -12V	7	PG2
U7	14	7	PG2
U8	24	12	PG3C7
U9	20	10	PG3C5
U10	20	10	PG3B5
U11	20	10	PG3B4
U12	20	10	PG3A5
U13	7 +5LH	4 -5LH	PG3D5
U14	26	7	PG5B6
U18	14	7,8	PG1A6

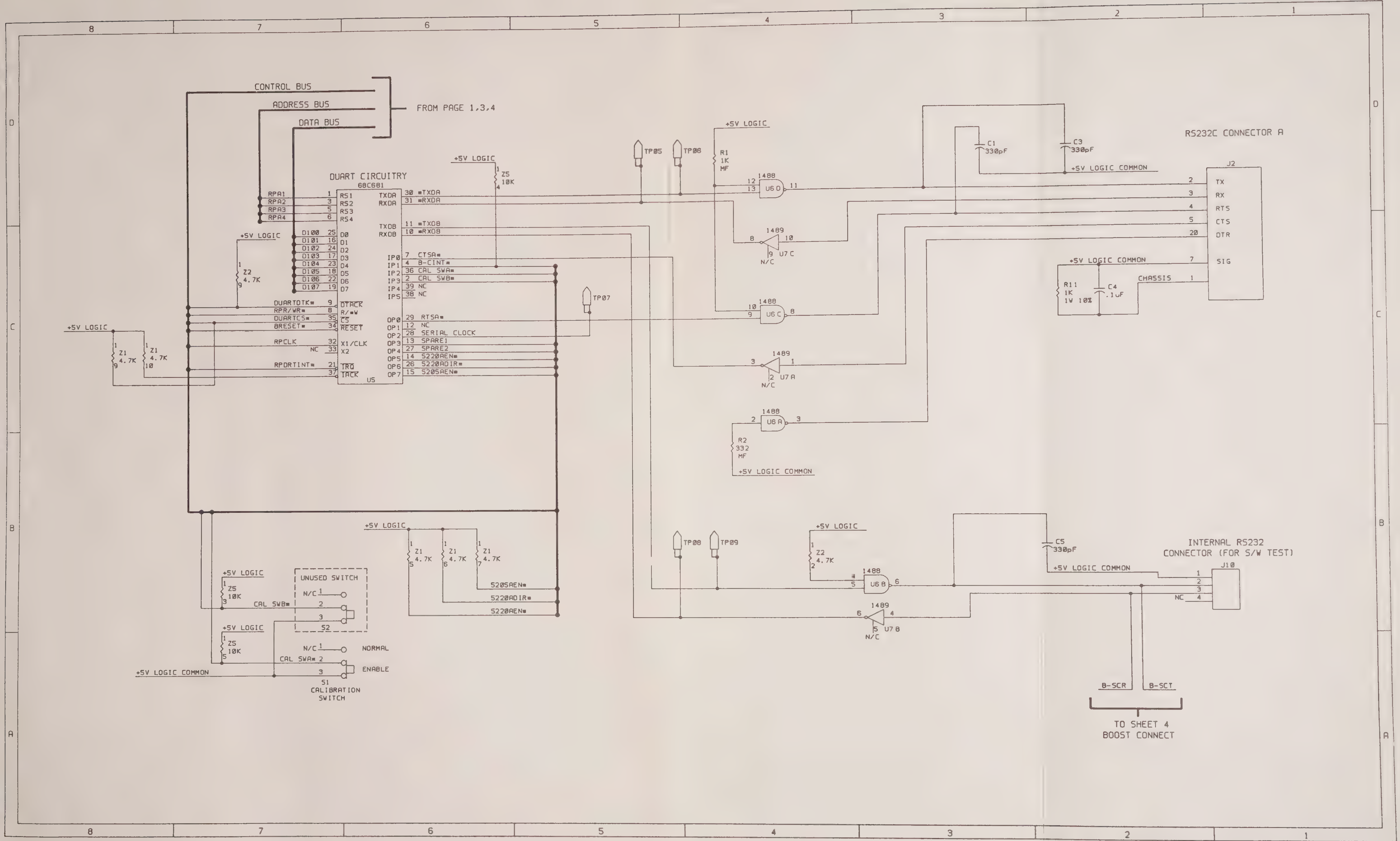
	LOCATION
J1	PG1
J2	PG2
J3	PG3
J4	PG3
J5	PG4
J6	PG4
J7	PG4
J8	PG4/PG5
J9	PG1
J10	PG2

NOTE: THE MOUNTING HOLES FOR CONNECTORS J1, J2, J3, J4, AND J7 ARE TIED TO CHASSIS THROUGH LAND PATTERNS ON THE PWB.

1. ALL RESISTORS ARE CARBON FILM 5%, 1/4W UNLESS NOTED.
2. ALL METAL FILM (MF) RESISTORS ARE 1%, 1/8W UNLESS NOTED.

REAR PANEL 5700A-1009 1 OF 5 AUG.29,1988

Figure 7-25. A21 Rear Panel PCA (cont)


CONTROL BUS
ADDRESS BUS
DATA BUS
FROM PAGE 1,3,4
DUART CIRCUITRY
68C681
U5
RPA1
RPA2
RPA3
RPA4
RS1
RS2
RS3
RS4
TXDA
RXDA
TXDB
RXDB
30 =TXDA
31 =RXDA
11 =TXDB
10 =RXDB
DI00
DI01
DI02
DI03
DI04
DI05
DI06
DI07
D0
D1
D2
D3
D4
D5
D6
D7
DUARTDTK=
RPR/WR=
DUARTCS=
BRESET=
RPCLK
NC
RPORTINT=
DTACK
R/=W
CS
RESET
X1/CLK
X2
IRQ
IACK
IP0
IP1
IP2
IP3
IP4
IP5
7 CTSA=
4 B-CINT=
36 CAL SWA=
2 CAL SWB=
39 NC
38 NC
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
29 RTSA=
12 NC
28 SERIAL CLOCK
13 SPARE1
27 SPARE2
14 5220AEN=
26 5220ADIR=
15 5205AEN=
+5V LOGIC
Z5
10K
Z2
4.7K
Z1
4.7K
TP05
TP06
TP07
TP08
TP09
R1
1K
MF
1488
U6 D
U6 C
U6 A
U6 B
1489
U7 C
U7 A
U7 B
N/C
R2
332
MF
+5V LOGIC COMMON
C1
330pF
C3
330pF
C5
330pF
R11
1K
1W 10%
C4
.1uF
CHASSIS
RS232C CONNECTOR A
J2
TX
RX
RTS
CTS
DTR
SIG
5205AEN=
5220ADIR=
5220AEN=
UNUSED SWITCH
N/C
CAL SWB=
S2
CAL SWA=
NORMAL
ENABLE
S1
CALIBRATION
SWITCH
INTERNAL RS232
CONNECTOR (FOR S/W TEST)
J10
NC
B-SCR
B-SCT
TO SHEET 4
BOOST CONNECT
8
7
6
5
4
3
2
1
D
C
B
A

REAR PANEL 5700A-1009 2 OF 5 AUG.29,1988

Figure 7-25. A21 Rear Panel PCA (cont)

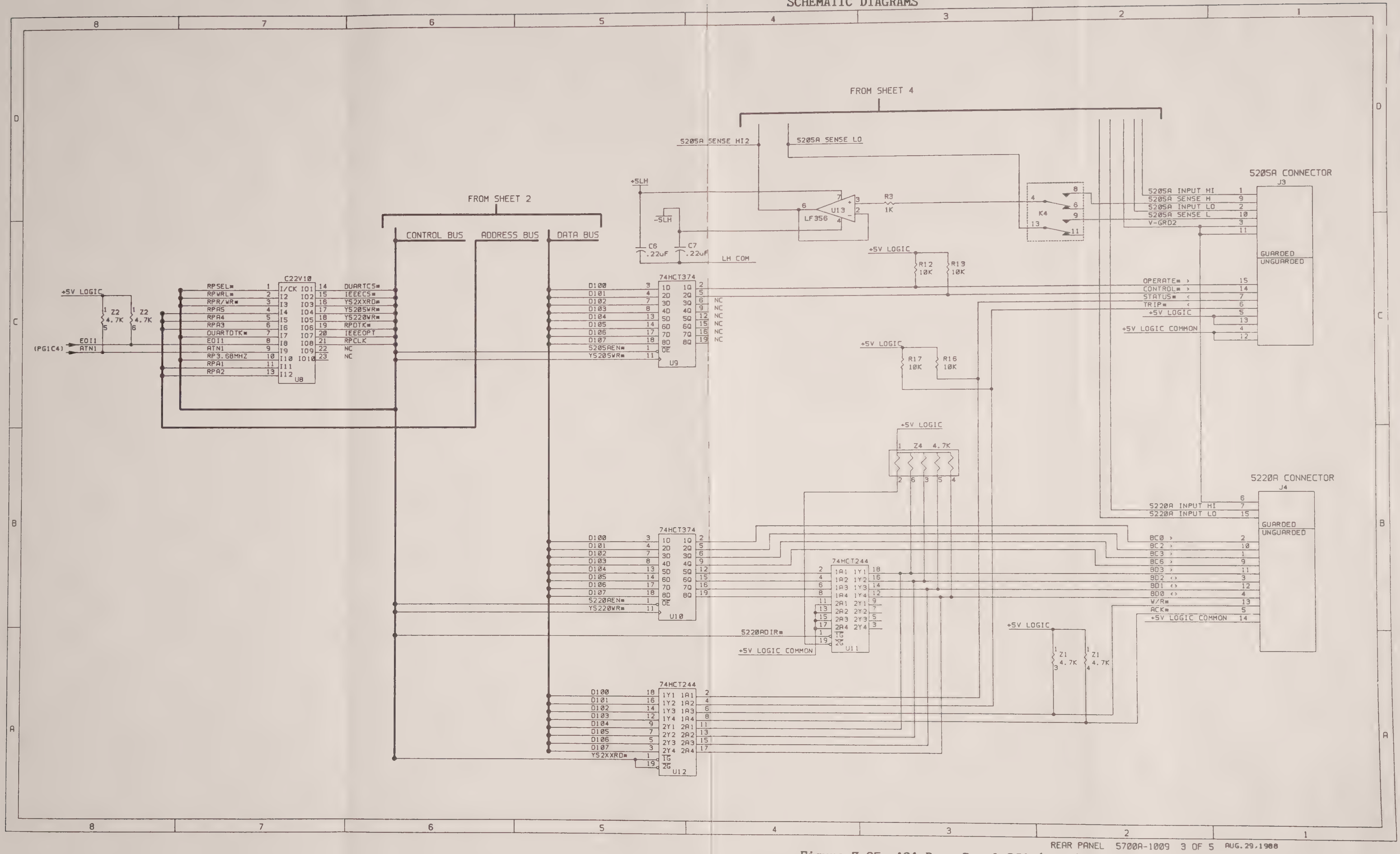
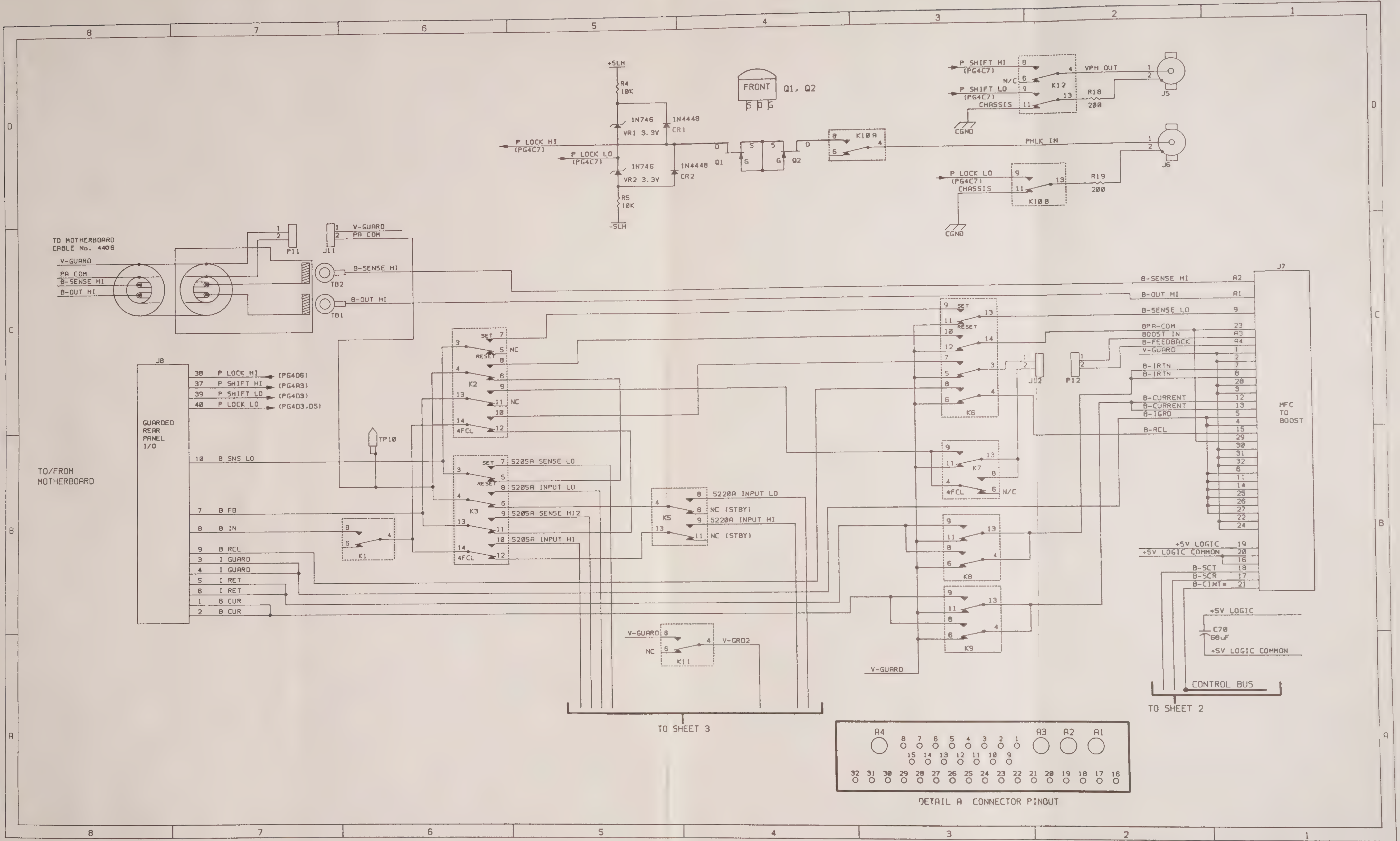
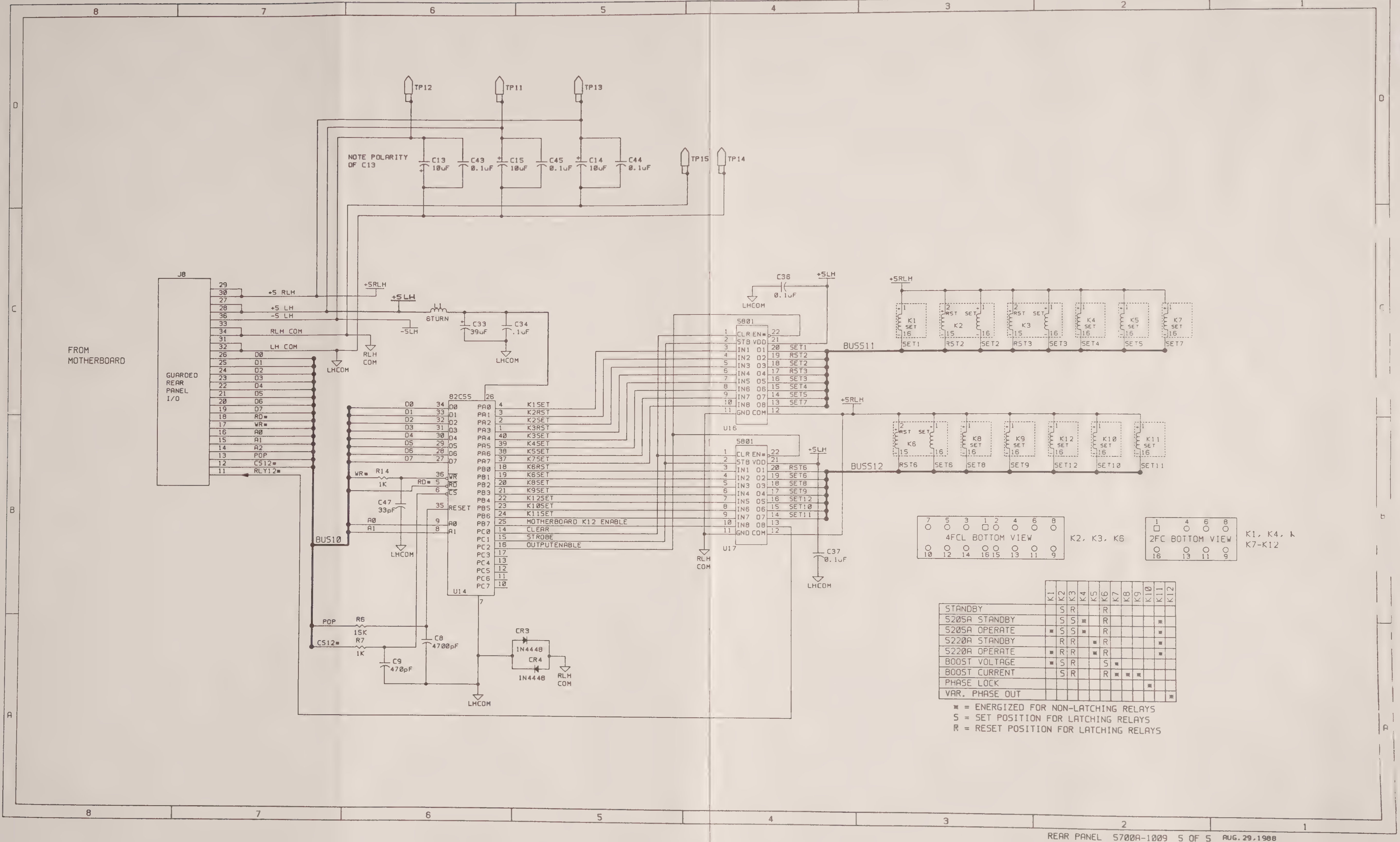

FROM SHEET 4
FROM SHEET 2
CONTROL BUS
ADDRESS BUS
DATA BUS
5205A SENSE HI2
5205A SENSE LO
+5LH
-5LH
C6 .22uF
C7 .22uF
LH COM
U13 LF356
R3 1K
K4
5205A CONNECTOR
J3
5205A INPUT HI
5205A SENSE H
5205A INPUT LO
5205A SENSE L
V-GRD2
GUARDED
UNGUARDED
+5V LOGIC
R12 10K
R13 10K
OPERATE=
CONTROL=
STATUS=
TRIP=
+5V LOGIC COMMON
R17 10K
R16 10K
Z2 4.7K
EOI1
ATN1
(PG1C4)
C22V10
U8
RPSEL=
RPWRL=
RPR/WR=
RPA5
RPA4
RPA3
DUARTDTK=
RP3.68MHZ
RPA1
RPA2
DUARTCS=
IEEECS=
YS2XXRD=
YS205WR=
YS220WR=
RPDTK=
IEEEOPT
RPCLK
NC
74HCT374
U9
D100
D101
D102
D103
D104
D105
D106
D107
5205AEN=
YS205WR=
Z4 4.7K
5220A CONNECTOR
J4
5220A INPUT HI
5220A INPUT LO
BC0
BC2
BC3
BC6
BD3
BD2
BD1
BD0
W/R=
ACK=
74HCT374
U10
5220AEN=
YS220WR=
74HCT244
U11
5220ADIR=
Z1 4.7K
74HCT244
U12
YS2XXRD=
REAR PANEL 5700A-1009 3 OF 5 AUG.29.1988

Figure 7-25. A21 Rear Panel PCA (cont)


+5LH
R4
10K
1N746
VR1 3.3V
1N4448
CR1
1N746
VR2 3.3V
1N4448
CR2
R5
10K
-5LH
P LOCK HI
(PG4C7)
P LOCK LO
(PG4C7)
Q1
Q2
FRONT
Q1, Q2
K10A
P SHIFT HI
(PG4C7)
N/C
P SHIFT LO
(PG4C7)
CHASSIS
K12
VPH OUT
R18
200
J5
CGND
PHLK IN
J6
P LOCK LO
(PG4C7)
CHASSIS
R19
200
K10B
CGND
TO MOTHERBOARD
CABLE No. 4406
V-GUARD
PA COM
B-SENSE HI
B-OUT HI
P11
J11
V-GUARD
PA COM
B-SENSE HI
TB2
B-OUT HI
TB1
J8
38 P LOCK HI (PG4D6)
37 P SHIFT HI (PG4A3)
39 P SHIFT LO (PG4D3)
40 P LOCK LO (PG4D3,D5)
GUARDED
REAR
PANEL
I/O
TO/FROM
MOTHERBOARD
10 B SNS LO
7 B FB
8 B IN
9 B RCL
3 I GUARD
4 I GUARD
5 I RET
6 I RET
1 B CUR
2 B CUR
TP10
K1
SET
RESET
NC
K2
4FCL
K3
5205A SENSE LO
5205A INPUT LO
5205A SENSE HI2
5205A INPUT HI
K5
5220A INPUT LO
NC (STBY)
5220A INPUT HI
NC (STBY)
V-GUARD
NC
K11
V-GRD2
TO SHEET 3
K6
J12
P12
K7
N/C
K8
K9
V-GUARD
J7
B-SENSE HI A2
B-OUT HI A1
B-SENSE LO 9
BPA-COM 23
BOOST IN A3
B-FEEDBACK A4
V-GUARD 1
B-IRTN
B-IRTN
B-CURRENT
B-CURRENT
B-IGRD
B-RCL
MFC
TO
BOOST
+5V LOGIC 19
+5V LOGIC COMMON 20
B-SCT 18
B-SCR 17
B-CINT* 21
+5V LOGIC
C70
68uF
+5V LOGIC COMMON
CONTROL BUS
TO SHEET 2
A4 8 7 6 5 4 3 2 1 A3 A2 A1
15 14 13 12 11 10 9
32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
DETAIL A CONNECTOR PINOUT

REAR PANEL 5700A-1009 4 OF 5 AUG.29.1988

Figure 7-25. A21 Rear Panel PCA (cont)


TP12
TP11
TP13
TP15
TP14
NOTE POLARITY OF C13
C13 10uF
C43 0.1uF
C15 10uF
C45 0.1uF
C14 10uF
C44 0.1uF
J8
FROM MOTHERBOARD
GUARDED REAR PANEL I/O
+5 RLH
+5 LH
-5 LH
RLH COM
LH COM
+5RLH
+5LH
6TURN
-5LH
C33 39uF
C34 .1uF
LHCOM
RLH COM
D0
D1
D2
D3
D4
D5
D6
D7
RD*
WR*
A0
A1
A2
POP
CS12*
RLY12*
82C55
U14
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
RESET
K1SET
K2RST
K2SET
K3RST
K3SET
K4SET
K5SET
K7SET
K6RST
K6SET
K8SET
K9SET
K12SET
K10SET
K11SET
MOTHERBOARD K12 ENABLE
CLEAR
STROBE
OUTPUTENABLE
R14 1K
C47 33pF
BUS10
R6 15K
R7 1K
C8 4700pF
C9 470pF
CR3 1N4448
CR4 1N4448
C36 0.1uF
5801
U16
U17
CLR EN*
STB VDD
IN1 O1
IN2 O2
IN3 O3
IN4 O4
IN5 O5
IN6 O6
IN7 O7
IN8 O8
GND COM
SET1
RST2
SET2
RST3
SET3
SET4
SET5
SET7
RST6
SET6
SET8
SET9
SET12
SET10
SET11
BUSS11
BUSS12
C37 0.1uF
K1
K2
K3
K4
K5
K7
K6
K8
K9
K12
K10
K11
RST
SET
4FCL BOTTOM VIEW
K2, K3, K6
2FC BOTTOM VIEW
K1, K4, K
K7-K12
REAR PANEL 5700A-1009 5 OF 5 AUG.29.1988

	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12
STANDBY		S	R			R						
5205A STANDBY		S	S	■		R					■	
5205A OPERATE	■	S	S	■		R					■	
5220A STANDBY		R	R		■	R					■	
5220A OPERATE	■	R	R		■	R					■	
BOOST VOLTAGE	■	S	R			S	■					
BOOST CURRENT		S	R			R	■	■	■			
PHASE LOCK										■		
VAR. PHASE OUT												■

■ = ENERGIZED FOR NON-LATCHING RELAYS
S = SET POSITION FOR LATCHING RELAYS
R = RESET POSITION FOR LATCHING RELAYS

Figure 7-25. A21 Rear Panel PCA (cont)

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